CMOS-compatible method for doping of buried vertical polysilicon structures by solid phase diffusion

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Polysilicon receives attention nowadays as a means to incorporate 3D-structured photonic devices into silicon processes. However, doping of buried layers of a typical 3D structure has been a challenge. We present a method for doping of buried polysilicon layers by solid phase diffusion. Using an underlying silicon oxide layer as a dopant source facilitates diffusion of dopants into the bottom side of the polysilicon layer. The polysilicon is grown on top of the oxide layer, after the latter has been doped by ion implantation. Post-growth heat treatment drives in the dopant from the oxide into the polysilicon. To model the process, we studied the diffusion of the two most common silicon dopants, boron (B) and phosphorus (P), using secondary ion mass spectroscopy profiles. Our results show that shallow concentration profiles can be achieved in a buried polysilicon layer using the proposed technique. We present a quantitative 3D model for the diffusion of B and P in polysilicon, which turns the proposed method into an engineerable technique. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4944778]

Polysilicon is a versatile and simple to integrate material, which is in common use for manufacturing of complicated layers and structures in the microelectronics industry.[1] The ability to deposit polysilicon on a wide variety of substrates along with standard CMOS techniques enables manufacturing of complex 3D structures,[2,3] which offer an advantage in various applications such as thin-film transistors,[4] microelectromechanical systems (MEMS),[5] and solar cells,[6] and has recently shown great promise in silicon photonics.[7–9]

Vertical structures have been employed in the design of semiconductor devices as a means to minimize device area. However, they require a complex fabrication process that renders their manufacturing a challenge.[10] One of the main challenges is the doping of deep buried layers during the formation of a P-N junction.[11] Ion implantation of such layers causes severe damage to all up-lying layers and makes impossible the formation of a shallow concentration profiles.[12] *In-situ* doping avoids this problem and produces ultra-shallow concentration profile.[13] However, it is not suitable when different dopant types or concentrations are required across the wafer. Recent developments, such as molecular monolayer doping and microwave annealing, provide a promising method for ultra-shallow, highly activated junctions by low-temperature process, using new techniques that are not part of the standard CMOS process.[14,15] In contrast, solid phase diffusion proposes the benefit of shallow concentration profiles and selective doping using a common CMOS process.[16] In its common use, a heavily doped temporary layer is formed *above* the target layer and serves as the dopant source. An annealing step is employed to drive the dopants by diffusion into the target layer. The temporary layer is then removed, leaving a doped active layer.

The use of solid phase diffusion for doping of *top* layers has been thoroughly studied.[17] However, doping of the *bottom* side of the buried layer in vertical structures is still a challenge. The heavily doped source layer cannot be removed at the end of the process and, therefore, is required to be electrically inactive. The challenge is even greater, when the bottom side of the desired layer is non-planar, in which case, the dopant-source layer is required to have the same non-planar shape, but, at the same time, should be uniformly doped.

A buried silicon oxide layer, heavily doped by ion implantation, may be an ideal candidate for this challenging task. Integration of silicon oxide as a dopant-source layer in standard CMOS process was thoroughly studied.[18–20] The effect of high scattering of the implanted ions in the oxide prevents channeling, and thus, a thin heavily doped layer can be created near the top surface. An almost uniform concentration profile is achieved this way even on non-planar oxide layer using angle implantation. However, most of the oxide thickness remains undoped and serves as an insulator. In combination with photolithography, different 3D structures can be fabricated using the proposed technique. For example, a high efficiency 3-D photodiode is shown in Fig. 1. The lens-like device shape, reminiscent of honeycomb structures used in photovoltaics,[21] is beneficial due to internal reflections that improve light absorption.

In this study, we investigated doping of polysilicon buried layers using solid phase diffusion. A polysilicon layer was deposited over a heavily doped silicon oxide layer followed by drive-in anneal to dope the *bottom side* of a polysilicon layer with boron (B) or phosphorus (P).

Polysilicon is composed of grains (G) separated by grain boundaries (GB). Diffusion takes place both at GB and inside the grains. Depth profiling methods typically integrate over areas much greater than the cross-section of a grain and, therefore, are usually incapable of separating the *intra-grain* from the *inter-grain* concentrations. The diffusivity at

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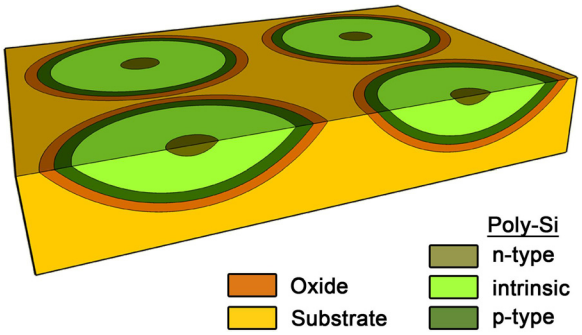

FIG. 1. An example of a 3D-structured photonic device application of polysilicon: High efficiency hemispheric polysilicon P-I-N photodiode array that can be fabricated using our method. High responsivity may be achieved due to the spherical shape that optimizes the surface-to-volume ratio. The lens-like shape is beneficial from the optical point of view.

GB is significantly greater than that inside grains producing a non-uniform profile distribution. Each data point in the resulting depth profile is therefore an average between the concentrations at the boundaries and inside the grains.

The case studied here is of column-structured grains. A schematic of four columnar grains separated by GB's on top of a doped oxide layer is shown in Fig. 2 along with the possible diffusion paths indicated by arrows and their typical concentration profiles. Vertical diffusion from the underlying oxide progresses in parallel into the grain and the GB. The diffusion in GB is much faster than that inside the grain. The resulting GB concentration serves as a secondary source for horizontal diffusion from the boundaries into the grains.

To fit measured depth profiles, we constructed a 3D diffusion model that simulates each of the diffusion mechanisms in a single grain and its boundaries, and then calculates the concentration average for the entire cross-section from this result, thus simulating a data point in a real depth profile.

In the method we propose, the oxide layer is heavily doped. However, the total dose traversing the oxide/polysilicon interface is more than two orders of magnitude lower than the implanted dose due to redistribution of the dopant during the diffusion across the interface. It is therefore safe to assume that the oxide is an infinite dopant source and that

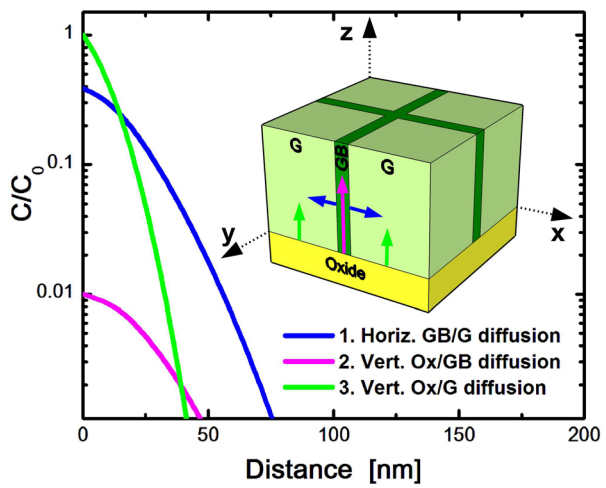

FIG. 2. Schematic of four grains with possible diffusion paths, and the typical diffusion profile as a function of the distance from oxide interface contributed by each diffusion mechanism to the total depth profile.

the effective concentration at the polysilicon side near the interface remains constant for the short rapid thermal anneal (RTA) durations. Therefore, the concentration profiles for vertical diffusion may be described by a solution of the diffusion equation for a constant concentration source. In the case of vertical diffusion from the oxide directly into the grain the solution is of the form

$$C_g(z,t) = C_0 erfc\left(\frac{z}{2\sqrt{D_g t}}\right)\ \text{cm}^{-3}, \tag{1}$$

where C_0 is the concentration at the oxide/poly interface, z is the displacement from the interface, D_g is the diffusivity of dopant in the grain, and t is the duration of diffusion.

For diffusion from the boundaries into the grain, the source becomes the concentration in the boundary at a certain depth. This source is *not constant*, but rather grows with time. When no segregation at the grain boundary occurs, the solutions of the diffusion equation for both vertical diffusion within the GB and the resulting horizontal diffusion into the grain are described by the following equations:[22]

$$C_{gb}(z,t) = C_0 \sum_{n=0}^{\infty} \alpha^n \left(erfc\left(\frac{2nz_0 + z}{2\sqrt{D_{gb}t}}\right) - \alpha erfc\left(\frac{2(n+1)z_0 - z}{2\sqrt{D_{gb}t}}\right)\right)\ \text{cm}^{-3}, \tag{2}$$

$$C_g(x,t) = \frac{2kC_0}{k+1} \sum_{n=0}^{\infty} \alpha^n erfc\left(\frac{(2n+1-k)z_0 + kx}{2\sqrt{D_{gb}t}}\right)\ \text{cm}^{-3}, \tag{3}$$

$$\text{where } k = \sqrt{\frac{D_{gb}}{D_g}}, \quad \alpha = \frac{1-k}{1+k}, \tag{4}$$

and x is the displacement from the GB for the horizontal diffusion profile inside the grain and z is the displacement from the interface within the GB (the source for this diffusion is a point within the GB displaced by z_0 from the oxide interface).

For n-type impurities (As and P), which tend to segregate at GBs, the initial concentration for the horizontal diffusion will also be affected by this segregation. Kamins suggested that the ratio between the number of dopants segregated at the GB, N_{gb}, to that in the grain, N_g, may be described by[23]

$$\ln\left(\frac{N_{gb}}{N_g}\right) = \ln\left(\frac{AN_s}{N_{si}}\right) + \frac{Q_0}{kT}, \tag{5}$$

where N_s is the total number of sites per unit volume at the GB, N_{si} is the total number of sites per unit volume in the system, A is the entropy factor, and Q_0 is the heat of segregation, which is defined as a difference in enthalpy between an impurity atom in the grain and one in the GB. The concentration ratio at the GB/G interface in equilibrium obtained from (5) will be of the form

$$\frac{C_g}{C_{gb}} \approx \frac{1}{A}\exp\left(-\frac{Q_0}{kT}\right). \tag{6}$$

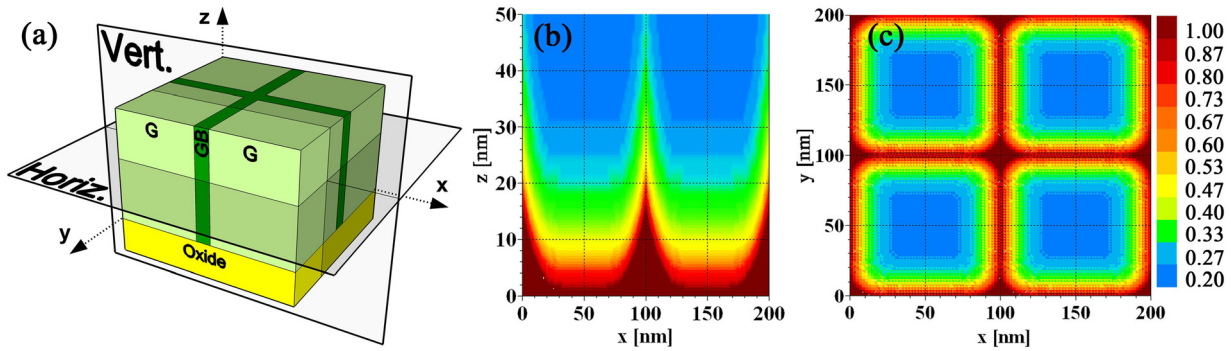

FIG. 3. (a) Grain schematics, (b) normalized concentration (C/C_0) map of the vertical x-z plain, and (c) of the horizontal x-y plain.

Figure 3(a) shows a schematic of the four-grain cell and two cross-sections in perpendicular plains. 2D maps of normalized concentrations in these two cross-sections are shown in Figs. 3(b) and 3(c).

The fitting parameters are the initial concentration, grain diffusivity, GB diffusivity, and GB segregation coefficient.

Standard p-type Si (100) wafers were thermally oxidized to oxide thickness of 600 nm. Either B or P was ion implanted into the oxide at several doses and energies. Following the implantation, the wafers were cleaned using the standard RCA process.[24] A 300 nm-thick polysilicon layer was then grown on top of the oxide using low-pressure chemical vapor deposition (LPCVD), introducing silane gas (SiH_4) at a temperature of 610 °C and pressure of 15 Pa. The polysilicon layer was followed by an additional, encapsulating layer of 50-nm-thick SiO_2 grown by plasma-enhanced chemical vapor deposition (PECVD) for the prevention of out-diffusion of dopants during heat treatments. Annealing was carried out at a temperature of 950 °C for various durations from 0.5 s up to 2.5 s, using RTA, or for 1 h using furnace anneal. Actual RTA time was monitored in real time, in an automated process that also takes into account the energy provided at ramp-up and ramp-down. After annealing, the SiO_2 encapsulation layer was wet-etched using hydrofluoric acid (HF) solution. The main process steps are shown in Fig. 4, and a summary of doping and annealing conditions for the various samples is given in Table I. Post-anneal dopant distributions were measured using secondary ion mass spectrometry (SIMS). Size and morphology of the polysilicon grains were studied using cross-sectional transmission electron microscopy (TEM).

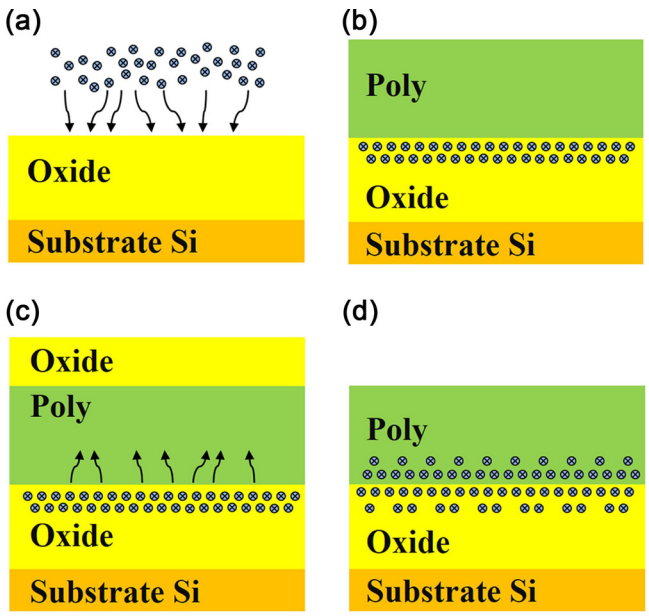

FIG. 4. Process flow: (a) ion implantation of oxide (B or P), (b) polysilicon deposition, (c) drive-in anneal, (d) final structure.

A columnar structure of the grains along the growth direction is observed in the cross-sectional TEM image (Fig. 5). The average grain width is 90 ± 10 nm.

Fig. 6 shows SIMS dopant concentration profiles (plus symbols) in wafers implanted with B and P after various annealing durations along with fit curves obtained using the proposed model (full lines).

For B, the peak concentration observed at the oxide/poly interface appears greater for longer anneal times, with the largest value of $7.4 \times 10^{18}\,cm^{-3}$ observed after 1-h anneal. For P, this peak concentration remained constant for different anneal times and increased only with the implant dose. For a dose of $2 \times 10^{15}\,cm^{-2}$, the maximum concentration of P is $1 \times 10^{19}\,cm^{-3}$ but increases to $1.1 \times 10^{20}\,cm^{-3}$ with a dose of $1 \times 10^{16}\,cm^{-2}$. The reason for the difference in the initial concentration of B is probably the "RCA clean" procedures performed after ion implantation. Exposure of the doped silicon oxide to the diluted HF solution between SC-1 and SC-2 steps in RCA clean procedure etches a thin layer from the oxide surface. HF is known to attack B more readily than it attacks the silicon oxide, thereby reducing the etch rate of the doped oxide. For P doped silicon oxide, the effect is the opposite. By this way, a certain depletion of B is caused by the RCA clean at the very surface of the oxide.

TABLE I. Doping and annealing conditions used in this study.

	Implant			Anneal	
#	Dopant	Dose (cm^{-2})	Energy (keV)	Temp (°C)	Time (s)
1	B	1×10^{16}	4	950	0.5
2	B	1×10^{16}	4	950	1
3	B	1×10^{16}	4	950	2.5
4	B	1×10^{16}	15	950	3600
5	P	2×10^{15}	10	950	1
6	P	2×10^{15}	10	950	2
7	P	1×10^{16}	10	950	2
8	P	1×10^{16}	15	950	3600

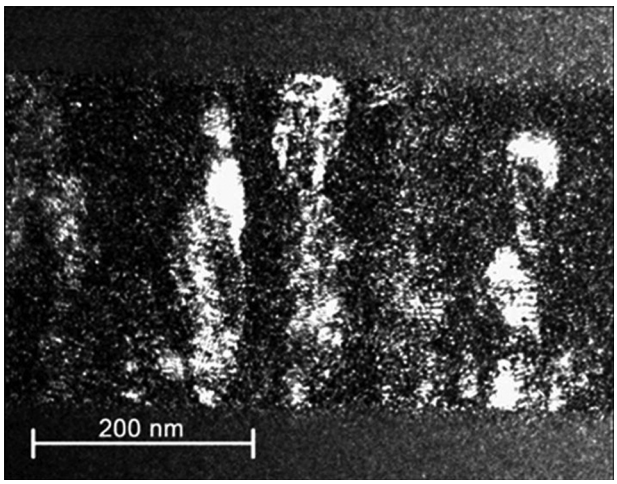

FIG. 5. Cross-sectional TEM of our polysilicon layer after RTA.

Nonetheless, this loss is replenished rapidly at the onset of diffusion, restoring B concentration at the interface to its previous level, as observed in SIMS results.[25]

As there is no segregation in the case of B, the resulting profile is a combination of all the three mechanisms described in Fig. 2. The contribution of the horizontal GB/G diffusion is manifested as a kink in the total concentration profile.

In case of P, which is known to segregate at GB, the ratio of dopants entering from GB into the grain can be calculated by Eq. (6). For phosphorus, the entropy factor, A, is in the range 2–3, and Q_0 is ~0.41–0.44 eV.[23] Substituting these parameters in Eq. (6) yields that the initial concentration of P at the grain is over two orders of magnitude lower than the source concentration at the GB. This suggests that horizontal diffusion of P into the grains is negligible. Thus, the resulting total profile is a combination of the vertical diffusion mechanisms only. Hence, the tail observed in the P profiles is due to high inactive concentration at the GB.

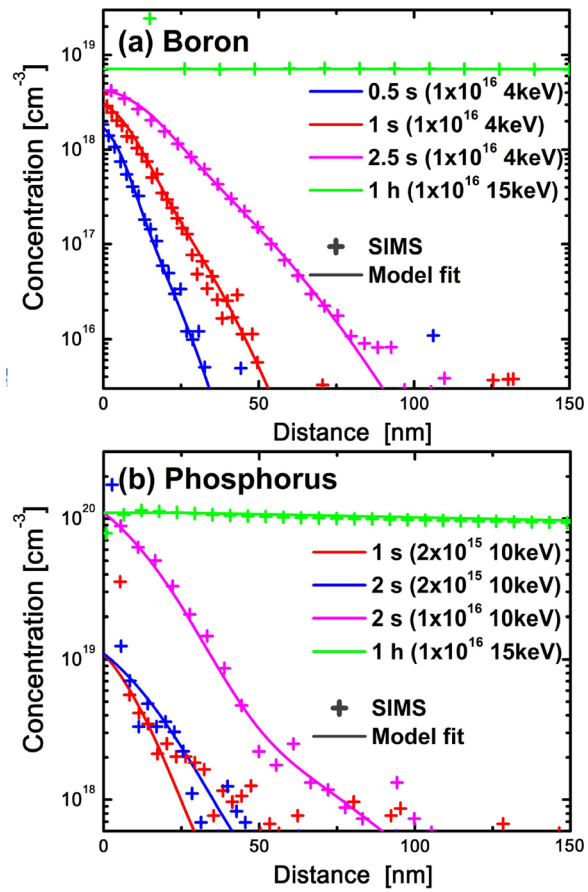

FIG. 6. SIMS depth profiles (pluses) and calculated doping profiles (full lines) as a function of distance from the oxide interface of (a) B and (b) P diffusion into polysilicon for different heat treatments duration and implant conditions.

Based on the TEM measurements (Fig. 5), a grain width of 100 nm was used in the model, while the GB width was assumed to be 1 nm.[26] Fitting the SIMS data with the model, we obtained a B diffusivity of 4×10^{-13} cm^2/s in grain and 1.8×10^{-12} cm^2/s in GB. For P, grain diffusivity was found to be 9×10^{-13} cm^2/s and GB diffusivity of -7×10^{-12} cm^2/s. Our results match the reported values for B and P diffusivity in polysilicon (though diffusion in these studies was achieved using other techniques).[27–30]

The method we present removes the main obstacle on the way to achieving shallow 3D doping profiles. It provides a CMOS-compatible technique for solid phase diffusion doping for the bottom side of a polysilicon layer, along with a quantitative model for the diffusion of B and P. This makes our technique engineerable and enables the design and manufacturing of vertical polysilicon P-N junctions and the incorporation of 3-D photonic device structures in a planar CMOS process.

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[1]M. F. Hung, Y. C. Wu, and Z. Y. Tang, Appl. Phys. Lett. **98**, 162108 (2011).
[2]C. Y. Ho, Y. J. Chang, and Y. L. Chiou, J. Appl. Phys. **114**, 054503 (2013).
[3]M. S. Seo, B. H. Lee, S. K. Park, and T. Endoh, IEEE Trans. Electron Devices **59**, 2078 (2012).
[4]Y. C. Cheng, Y. C. Wu, H. B. Chen, M. H. Han, N. H. Lu, J. J. Su, and C. Y. Chang, Appl. Phys. Lett. **103**, 123510 (2013).
[5]G. A. Myers, S. S. Hazra, M. P. de Boer, C. A. Michaels, S. J. Stranick, R. P. Koseski, R. F. Cook, and F. W. DelRio, Appl. Phys. Lett. **104**, 191908 (2014).
[6]A. Kumar, H. Hidayat, C. Ke, S. Chakraborty, G. K. Dalapati, P. I. Widenborg, C. C. Tan, S. Dolmanan, and A. G. Aberle, J. Appl. Phys. **114**, 134505 (2013).
[7]K. Preston, B. Schmidt, and M. Lipson, Opt. Express **15**, 17283 (2007).
[8]K. Preston, P. Dong, B. Schmidt, and M. Lipson, Appl. Phys. Lett. **92**, 151104 (2008).
[9]L. Lagonigro, N. Healy, J. R. Sparks, N. F. Baril, P. J. A. Sazio, J. V. Badding, and A. C. Peacock, Appl. Phys. Lett. **96**, 041105 (2010).
[10]P. G. Emma and E. Kursun, IBM J. Res. Dev. **52**, 541 (2008).
[11]C. S. Tan, R. J. Gutmann, and L. R. Reif, *Wafer Level 3-D ICs Process Technology* (Springer, New York, 2008), p. 35.
[12]M. I. Current and D. Pramanik, Solid State Technol. **27**, 211 (1984).
[13]C. M. Polley, W. R. Clarke, J. A. Miwa, G. Scappucci, J. W. Wells, D. L. Jaeger, M. R. Bischof, R. F. Reidy, B. P. Gorman, and M. Simmons, ACS Nano **7**, 5499 (2013).
[14]Y.-J. Lee, T.-C. Cho, K.-H. Kao, P.-J. Sung, F.-K. Hsueh, P.-C. Huang, C.-T. Wu, S.-H. Hsu, W.-H. Huang, H.-C. Chen, Y. Li, M. I. Current, B. Hengstebeck, J. Marino, T. Buyuklimanli, J.-M. Shieh, T.-S. Chao, W.-F. Wu, and W.-K. Yeh, IEEE Int. Electron Devices Meet. **2014**, 32.7.1–4.
[15]Y.-J. Lee, T.-C. Cho, S.-S. Chuang, F.-K. Hsueh, Y.-L. Lu, P.-J. Sung, H.-C. Chen, M. I. Current, T.-Y. Tseng, T.-S. Chao, C. Hu, and F.-L. Yang, IEEE Trans. Electron Devices **61**, 651 (2014).

[16]K. Ehinger, H. Kabza, J. Weng, M. Miura-Mattausch, I. Maier, H. Schaber, and J. Bieger, J. Phys. Colloq. **49**, C4-109 (1988).
[17]K. A. Jackson, *Silicon Devices: Structures and Processing* (Wiley-VCH, Veinheim, Federal Republic of Germany, 1998), p. 149.
[18]A. Fallisch, D. Wagenmann, R. Keding, D. Trogus, M. Hofmann, J. Rentsch, H. Reinecke, and D. Biro, IEEE J. Photovoltaics **2**, 450 (2012).
[19]B. Kalkofen, A. Amusan, M. Lisker, and E. P. Burte, Microelectoron. Eng. **109**, 113 (2013).
[20]M. L. Barry and P. Olofsen, J. Electrochem. Soc. **116**, 854 (1969).
[21]H. Sai, K. Saito, and M. Kondo, IEEE J. Photovoltaics **3**, 5 (2013).
[22]J. Crank, *The Mathematics of Diffusion*, 2nd ed. (Oxford University Press, London, Great Britain, 1975), p. 41.
[23]T. Kamins, *Polycrystalline Silicon for Integrated Circuits and Displays*, 2nd ed. (Springer, New York, 1998), p. 156.
[24]W. Kern and D. A. Puotinen, RCA Rev. **31**, 187 (1970).
[25]X. G. Zhang, *Electrochemistry of Silicon and Its Oxide* (Kluwer Academic Publishers, New York, 2001), p. 164.
[26]N. K. Upreti and S. Singh, Bull. Mater. Sci. **14**, 1331 (1991).
[27]S. Horiuchi and R. Blanchard, Solid-State Electron. **18**, 529 (1975).
[28]A. Merabet and C. Gontrand, Phys. Status Solidi A **145**, 77 (1994).
[29]C. Hill and S. K. Jones, *Polysilicon Thin Films and Interfaces*, edited by T. Kamins, B. Raicu, and C. V. Thompson (Mater. Res. Soc. Symp. Proc., 1990), Vol. 182, pp. 129–140.
[30]M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed. (CRC Press, Boca Raton, FL, 2002), p. 297.