Design of Ternary Schmitt Triggers Based on Its Sequential Characteristics

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Abstract

By analyzing the working characteristics of binary Schmitt circuits we find their sequential characteristics, which makes us follow the method of sequential circuits to design Schmitt circuits. The sequential design technique is extended to the study of ternary Schmitt circuits in this paper. The designed ternary Schmitt trigger has a similar structure with a ternary flip-flop. PSPICE simulation with TTL technology shows that the circuit has correct Schmitt characteristics.

1. Sequential characteristic analysis of Schmitt circuits

In the traditional binary digital circuits, Schmitt circuit is a useful device. One of its important characteristics is that it has different thresholds for the positive-going and negative-going direct current (DC) transmission characteristics, and the difference between them is called hysteresis. Such a trigger scheme makes it capable of receiving slowly varying input signals and effectively suppressing the interference imposed on the input signal. In digital circuits, Schmitt circuit is used as an effective device to reshape input signals. Obviously, in the multiple-valued logic, multiple-valued Schmitt trigger should hold its corresponding position and usage as its binary counterpart. Studying multiple-valued Schmitt circuits is helpful for the completeness of the multiple valued logic study.

In recent years, some research progress has been made on the design of multiple-valued Schmitt circuits based on TTL, CMOS, ECL, etc.[1-3] However, it is still lack of the study of their design principle. Therefore, the research should start from the binary Schmitt circuits. Traditionally, Schmitt circuit is thought of as a special gate, which has threshold-skipping effect. Taking a binary Schmitt circuit for example, it is different from a general gate, which has only one threshold (V_{TH}) to detect the input signal. Schmitt circuit shows that there are two thresholds, V_{T+} and V_{T-} Figures 1(a) and (b) show the different responses to a triangular wave input signal for a general inverter and a Schmitt inverter, respectively.

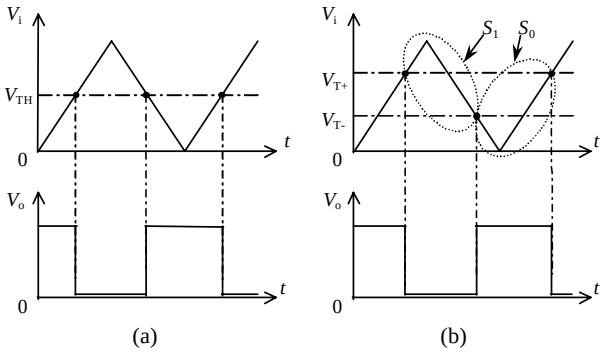

Fig. 1 (a) General ternary reshaping circuit

(b) Ternary Schmitt reshaping circuit

From Fig.1 (b), it is noted that when the input signal increases, the threshold of the circuit is V_{T+}, however, when the input signal exceeds V_{T+} and enters the high level region S_1, the threshold immediately skips from V_{T+} to V_{T-}; vice versa, when the input signal decreases to V_{T-} and enters low level region S_0, the detecting threshold of the circuit skips from V_{T-} to V_{T+} again. Traditionally, Schmitt circuit is classified as a special combinational gate. However, we believe that Schmitt circuits are of an obvious sequential characteristic, because when the input signal V_i is between V_{T+} and V_{T-}, the circuit level completely depends on whether the circuit is in high level or low level before entering the region, i.e., it is related to "the input history". Therefore, the sequential characteristic

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is obviously shown. In fact, the working process of the circuit has shown that it has two states, S_0 and S_1. According to the analysis method of the sequential circuits, its state transition graph (STG) can be obtained from Fig. 1(b), as shown in Fig. 2(a), where the arrows of state transition are labeled with the state transition conditions. In order to specify the STG using specific variables, state variable Q is introduced and each state Q = 0, 1 is named S_0 and S_1, respectively. In addition, it is noted that the circuit has two thresholds: When threshold is V_{T+}, variable x_+ is used to represent the logic value of the input and $x_+ = 0,1$ corresponds to $V_i < V_{T+}$ and $V_i > V_{T+}$, respectively. Similarly, variable x_- is introduced when threshold is V_{T-} and $x_- = 0,1$ corresponds to $V_i < V_{T-}$ and $V_i > V_{T-}$, respectively. Obviously, when the input in Fig.1(b) increases from low level to high level and decreases from high level to low level three regions will be passed by, while $x_+x_- = 00,01,11$. However, $x_+x_- = 10$ never appears. Having been introduced variables Q, x_+, x_-, STG and state transition table (STT) in Figs. 2(b) and (c) can be derived from Fig. 2(a). From the STT, the following next state equation is easily deduced:

$$Q' = x_+ + x_- \cdot Q = \overline{\overline{x_-} \cdot \overline{x_- \cdot Q}}$$

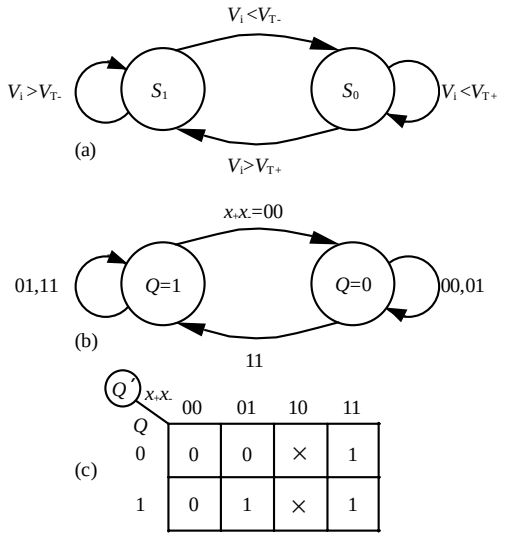

Fig. 2 State transition graph (STG) and state transition table (STT) of Schmitt trigger

The above equation describes the detailed structure using "NAND" gates to implement Schmitt circuits, which is shown in Fig. 3(a). In the circuit, if the input threshold of the inverter G_3 is taken as V_{T+} and one of input thresholds in NAND gate G_1 is taken as V_{T-} ($V_{T-} < V_{T+}$), Schmitt circuit can be implemented by using x instead of x_+ and x_- as inputs. However, if the circuit in Fig.3 is implemented using general gates rather than those having special thresholds, two following solutions can be employed as follows.

Solution 1: Set $V_{T+} = V_{TH}$. As long as we can manage to lower one of input thresholds in gate G_1, V_{T-} can be obtained. If TTL circuits are used, it can be easily implemented by serially connecting a diode as shown in Fig. 3 (b).

Solution 2: Set $V_{T-} = V_{TH}$. In this case, we need to increase the input threshold of the inverter G_3. If TTL circuits are used, it can be implemented by connecting a diode at the grounded terminal as shown in Fig. 3 (c).

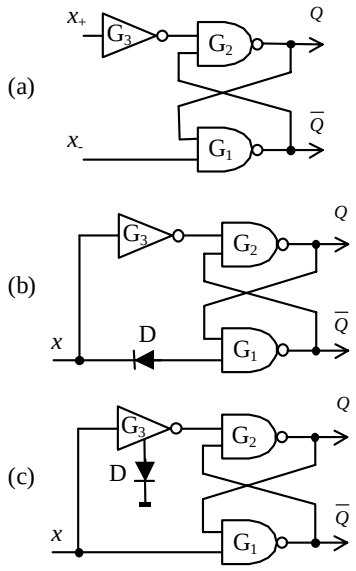

Fig. 3 NANA gate based design of Schmitt circuits

It is noted that there is a cross-coupled structure and complementary dual-rail outputs in Fig. 3, which is similar to flip-flops in structure. This characteristic of the structure testifies that Schmitt trigger is of the sequential characteristic. The difference between a general flip-flop and the Schmitt trigger is that the former stores signal (0 or 1) while the latter stores the threshold, V_{T-} or V_{T+}, to detect input signals.

According to the above discussion, ternary and higher radix Schmitt triggers can be developed in a similar way.

2. NAND gate based design of ternary Schmitt circuits

Differently from a general ternary gate with two thresholds, $V_{(0.5)}$, $V_{(1.5)}$, a ternary Schmitt circuit has four thresholds, $V_{(0.5)+}$, $V_{(1.5)+}$, $V_{(0.5)-}$, $V_{(1.5)-}$, to detect input signals. To illustrate it, Figs.4(a) and (b) show the different responses to the triangle wave input signals for a general ternary reshaper and a ternary Schmitt reshaper. From Fig.4(b), it can be seen that when the input signal V_i increases from low level to high level, the detecting threshold of the circuit is $V_{(0.5)+}$ and $V_{(1.5)+}$ while the input goes in the reverse direction it is $V_{(1.5)-}$ and $V_{(0.5)-}$, respectively. Hence, the input signal V_i can be divided into five regions according to its function to the circuit, as shown in Table 1.

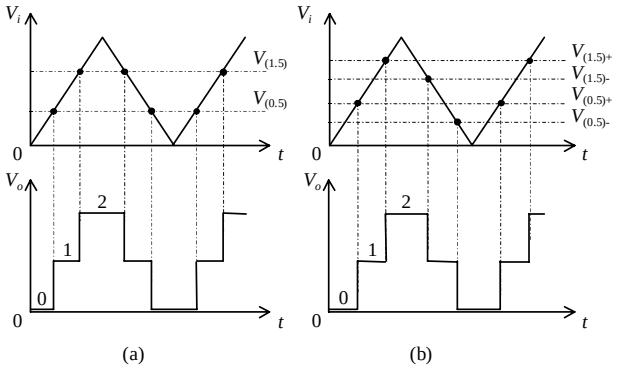

Fig. 4 (a) General inverter (b) Schmitt inverter

Range of input signal		x_+	x_-
Region A_2	$V_{(1.5)+} < V_i$	2	2
Region A_{12}	$V_{(1.5)-} < V_i < V_{(1.5)+}$	1	2
Region A_1	$V_{(0.5)+} < V_i < V_{(1.5)-}$	1	1
Region A_{01}	$V_{(0.5)-} < V_i < V_{(0.5)+}$	0	1
Region A_0	$V_i < V_{(0.5)-}$	0	0

Table 1 Regional table of input signal

In Table 1, x_+ represents the logic value when the detecting threshold is $V_{(0.5)+}$ or $V_{(1.5)+}$ while x_- represents the logic value when the detecting threshold is $V_{(0.5)-}$ or $V_{(1.5)-}$. It is noted that in regions A_{12} and A_{01} there are two different logic values corresponding to the same input voltage level. Which logic value the input signal will take completely depends on whether the input signal is positive going into the region or negative going into the region. From the discussion in the previous section, it has been shown that the ternary Schmitt circuits have the working characteristics of sequential circuits.

The ternary Schmitt circuit has three output states, 0, 1 and 2, which are named S_0, S_1, S_2. From Fig.4(b), its STG can be obtained as shown in Fig. 5(a). If a ternary state variable Q is used to represent three states and if x_+ and x_- in Table 1 are used to represent input conditions on state transition arrows, a specific variable state graph and next state Karnaugh Map can be derived, as shown in Figs.5(b) and (c), respectively. In Fig. 5(c), "×" is used to represent that the input condition cannot happen under this state. From Fig. 2(c), the following simplified next state function can easily be obtained:

$$Q' = x_+ + x_- \cdot Q = \overline{\overline{x_+} \cdot \overline{x_-} \cdot Q},$$

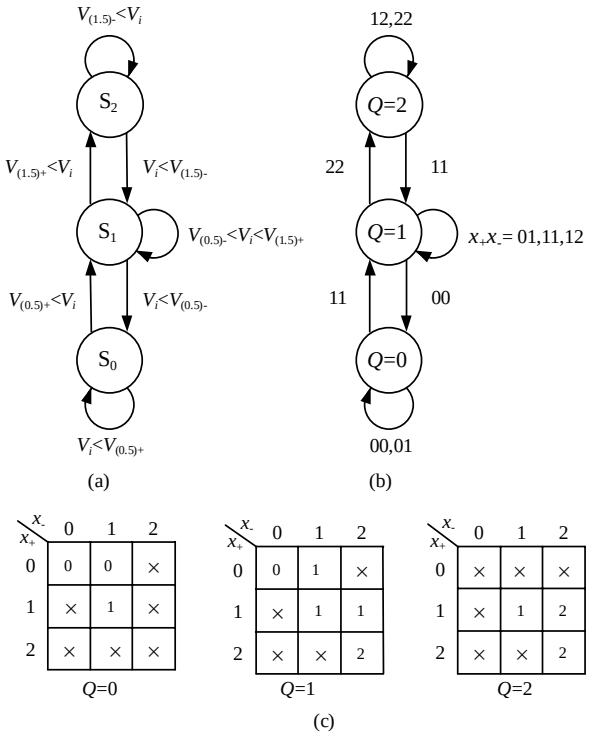

Fig. 5 Ternary Schmitt circuit
(a) State transition graph
(b) Specific variable state transition graph
(c) Next state Karnaugh Map

The logic structure is shown in Fig. 3(a). The difference between binary Schmitt circuit and ternary Schmitt circuit is only that all gates are ternary ones in the latter. Figure 3(a) shows that if the input threshold of the ternary inverter G_3 takes $V_{(0.5)+}$, $V_{(1.5)+}$ and one of the input

thresholds of the ternary NAND gate G_1 takes $V_{(0.5)-}$, $V_{(1.5)-}$ (Note: $V_{(0.5)-} < V_{(0.5)} < V_{(0.5)+}$, $V_{(1.5)-} < V_{(1.5)} < V_{(1.5)+}$), then ternary Schmitt circuit can be implemented by simply using x instead of x_+ and x_- as the inputs. However, if we use ternary gates with fixed threshold rather than use special gates with two special thresholds, the structures shown in Figs.3 (b) and (c) can be employed to design ternary Schmitt circuits. It is noted that the circuit has similar couple-cross structure and sequential working characteristic to the ternary flip-flops proposed in Ref.[4]. Hence, it can be recognized as a special flip-flop. To simply testify the above theory and the correspondingly designed circuit, the ternary TTL inverter proposed in Ref.[1] is employed to test whether the circuits shown in Figs.3(b) and (c) do have Schmitt threshold-jumping characteristics. A simple design of a ternary TTL inverter is shown in Fig.6. To a ternary input signal, two detecting thresholds 0.5 and 1.5 need to be set. Beneficially from the threshold-setting experience of binary TTL gate circuits, the threshold setting is implemented by properly connecting diodes in serial as shown in Fig.6. Suppose that three levels, 0V, 2.4V, 5V, are corresponding to logic, 0, 1, 2, then the detecting levels can be set at 1.6V and 3.2V corresponding to thresholds, 0.5 and 1.5, which can be implemented by serially connecting two and four diodes. In Fig.6, only one and three diodes are used in two threshold-setting circuits, respectively. The reason is that there is one pn junction existed in the be junction of the output transistor. The dashed lines in the figure show that a ternary TTL NAND gate can be obtained by simply increasing the number of the input transistor emitters.

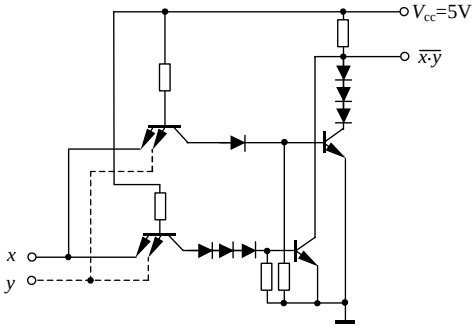

Fig. 6 A simple ternary TTL NAND gate

The ternary Schmitt circuits which have the structures shown in Figs.3 (b) and (c) have been simulated using PSpice. Both of DC transfer characteristics are shown in Figs.7 (a) and (b), respectively. From the figures, it can be seen that two circuits have good ternary Schmitt characteristics. Hence, the correctness of the above design theory is well testified.

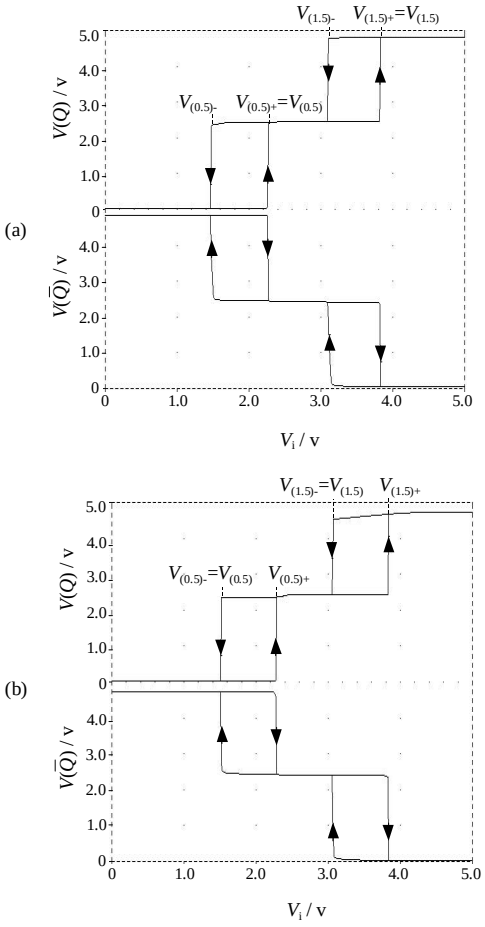

Fig.7 DC transfer characteristics of ternary Schmitt circuit in Fig.3 (b)

3. Conclusions

We think that the multiple-valued Schmitt triggers would be needed for the possible multiple-valued systems in practical application since such a trigger scheme can make it capable of receiving slowly varying multiple-valued input signals and effectively suppressing the interference imposed on the multiple-valued input signal.

By analyzing the working characteristics of binary Schmitt circuits, we find that Schmitt circuits have sequential characteristics. Hence, it is not correct that a Schmitt circuit was traditionally thought of as a special combinational gate. It, however, should be categorized as

a special flip-flop. If the design method for sequential circuits is used, the logic design of binary Schmitt circuits can be proposed.

The study for binary Schmitt circuits actually lays the foundation for the design of ternary Schmitt circuits. With a similar study procedure to the binary counterpart, it is found that the ternary Schmitt circuit has the same circuit structure as its binary counterpart. In order to testify the correctness of the design principle, we take a simply designed TTL circuit as an example. A gate level design of a ternary Schmitt circuit is proposed and PSpice simulation is conducted. The results show that the proposed ternary Schmitt circuit has correct logic functions.

As a matter of fact, based on the logic structure from Fig.3 (a), other integrated circuit types of ternary Schmitt circuits, such as CMS and ECL, can be designed. For example, using ion implants technology to control threshold to detect inputs, various ternary CMOS gates with two kinds of threshold had been designed in Ref.[5], by which the ternary CMOS Schmitt circuits can be obtained. Finally, it should be pointed out that the research on the sequential characteristics of Schmitt circuits in this paper could be applied to design multiple-valued Schmitt circuits with a higher radix.

4. Acknowledgments

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5. References

[1] G.Hang, X. Wu. Research on ternary TTL Schmitt trigger. J.of Electronics, Vol.15, No.1, pp.35-42, 1998.

[2] J. Shen, P.D.Tougaw. Design of symmetric ternary current-mode CMOS Schmitt inverter, Int. J. Electronics, Vol.85, No.4. pp.477-482, 1998.

[3] G.Hang, X. Wu. Switch-signal theory based threshold-control techniques and ternary ECL Schmitt circuits (in Chinese), J. of Circuits and Systems, Vol.3, No.2, pp.15-20, 1998.

[4] T. A. Irving, H. T. Nagle. An approach to multi-valued sequential logic. Conf. Rec. ISMVL, Toronto, pp.80-105, May 1973.

[5] X. Wu, F. Prosser, CMOS ternary logic circuits, IEE Proceedings, Part G, Vol.137, No.1, pp.21-27, 1990.