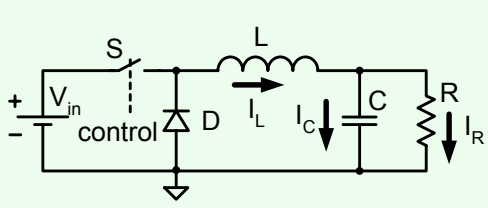
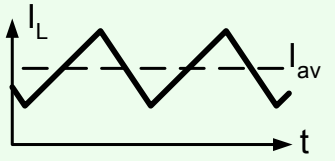
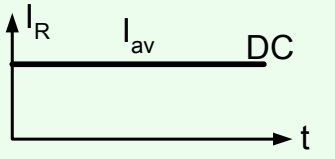
Output Voltage Ripple, Parasitic Effects

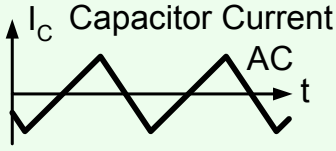
6.1 Output voltage ripple (Buck)
6.2 Parasitic effects
- 6.2.1 Diode recovery
- 6.2.2 Internal delay of switching
- 6.2.3 Stray and leakage inductances
  - Clamp
  - Diode snubber (clamp)
  - Switch snubbers

Output voltage ripple





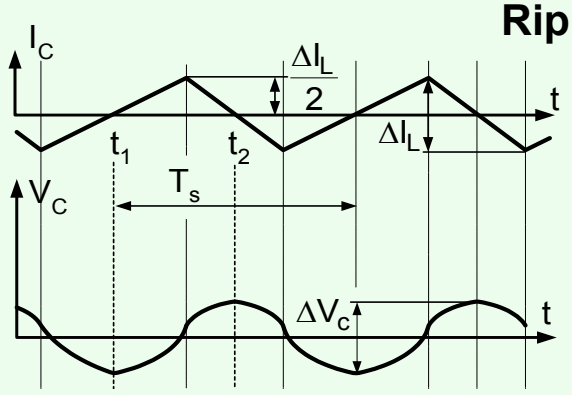




- **Assumption:**

Low output ripple voltage

Ripple



$$\Delta V_C = \frac{\Delta Q}{C};$$

$$\Delta Q = \int_{t_1}^{t_2} I_L dt;$$

$$\Delta V_C = \frac{\Delta I_L}{8C}\frac{1}{f_s}$$

$$\Delta Q = \frac{\Delta I_L}{2}\cdot\frac{T_s}{2}\cdot\frac{1}{2};$$

$$\Delta Q = \frac{\Delta I_L}{8}T_s$$

Ripple

$$\Delta I_L = V_o t_{off}/L \qquad \Delta I_L = \frac{V_o}{L}D_{off}T_s = \frac{V_o D_{off}}{Lf_s}$$

$$\Delta V_C = \frac{V_o D_{off}}{CLf_s}\frac{1}{8f_s} = \frac{V_o D_{off}}{8CLf_s^2}$$

The effect of f_s $\Delta I = \frac{V_o D_{off}}{Lf_s}$

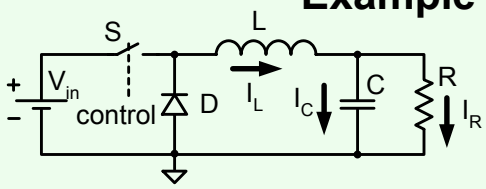
L; f_s can be traded for same ΔI $\Delta V_C = \frac{\Delta I_L}{8f_s C}$

C;f_s can be traded for same ΔI& ΔV_C

if f_s is increased for given L, C $\Delta V_C = \frac{V_o D_{off}}{8LCf_s^2}$

ΔV_C goes down -40 db/dec (second order)

Example



$\Delta I_L = 1A$

$C = 47\mu F$

$T_s = 10\mu S$

$ESR = 10m\Omega$

Find the output voltage ripple ΔV

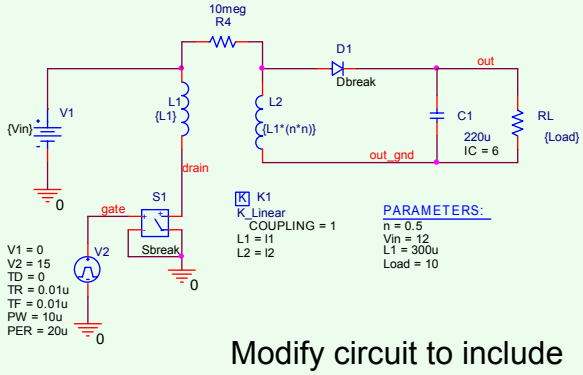
$$\Delta V_C = \frac{1A \cdot 10\mu S}{8 \cdot 47\mu F} = 25mV$$

$$\Delta V_{ESR} = 10m\Omega \cdot 1A = 10mV$$

- Approximate (upper limit) of total ripple)

$$\Delta V = \Delta V_C + \Delta V_{ESR} = 25mV + 10mV = 35mV$$

Application of Simulation

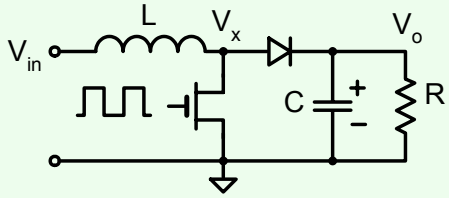


Modify circuit to include

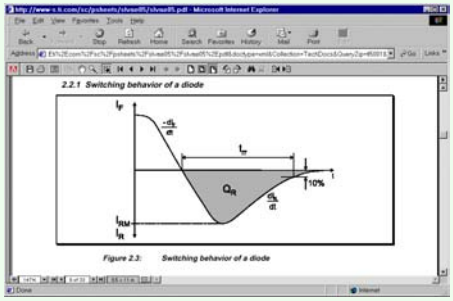
ESR=100mΩ

Find ripple at output

Diodes Recovery – Implications

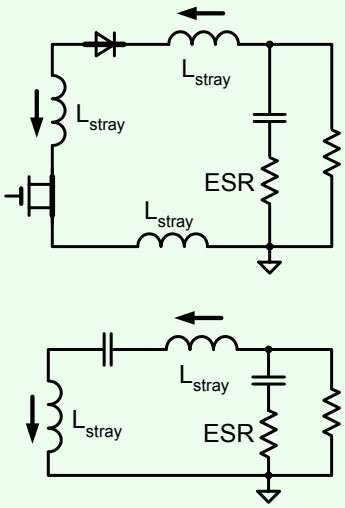


Reverse current at switch turn on

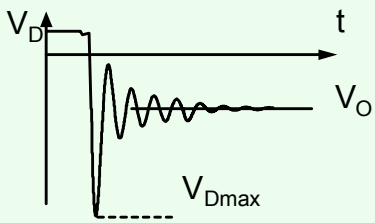


- **Soft and hard recovery**

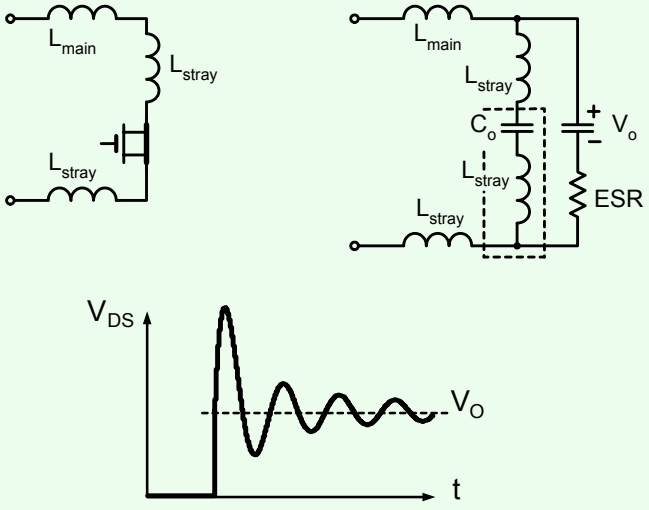
Stages in diode recovery



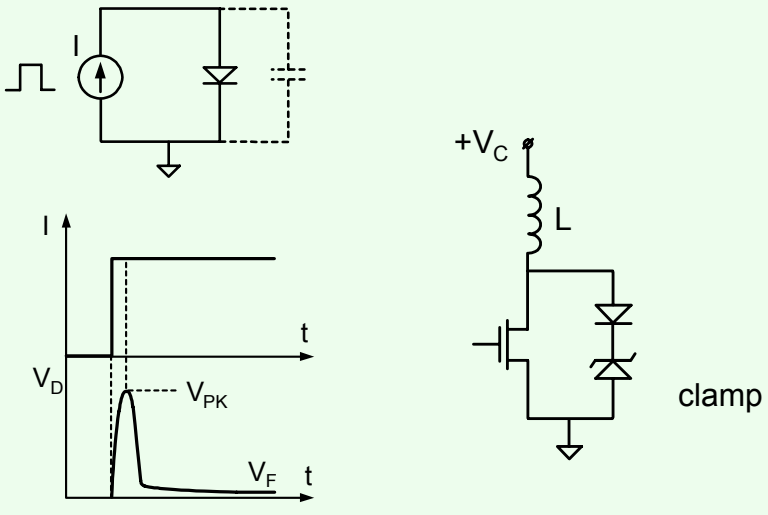
Diode voltage



Turn “off” of transistor

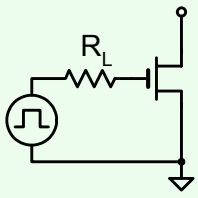


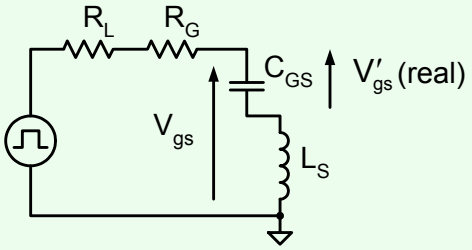
Diode forward recovery

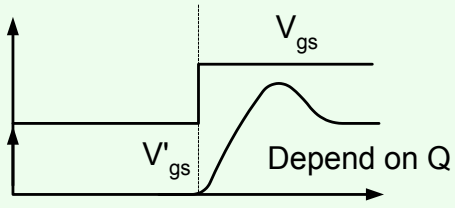


Parasitic effects: Internal delay

To turn “on”



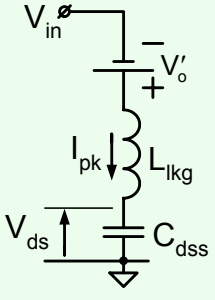


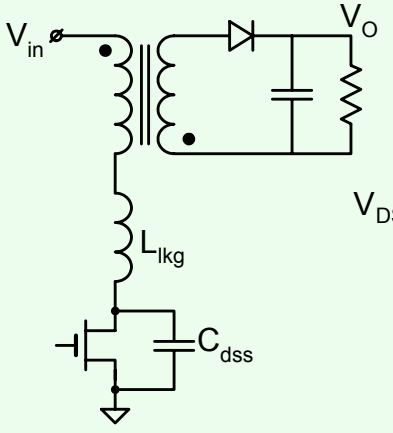


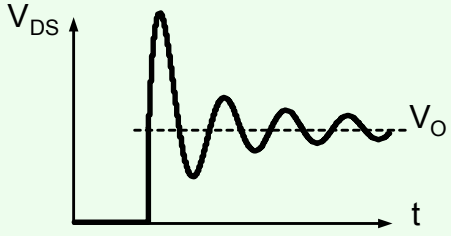
$$Q = \frac{\sqrt{\frac{L_S}{C_{gs}}}}{R_L + R_G}$$

Clamps

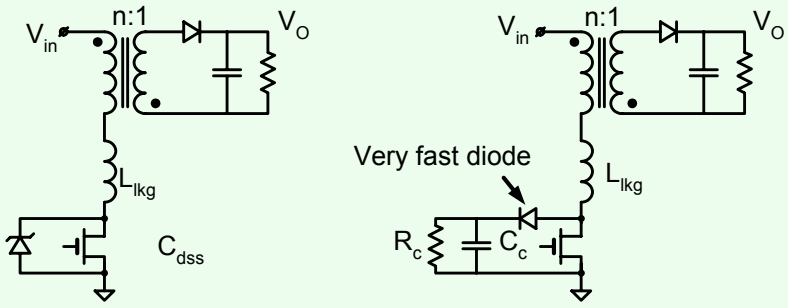
* limiting maximum voltage





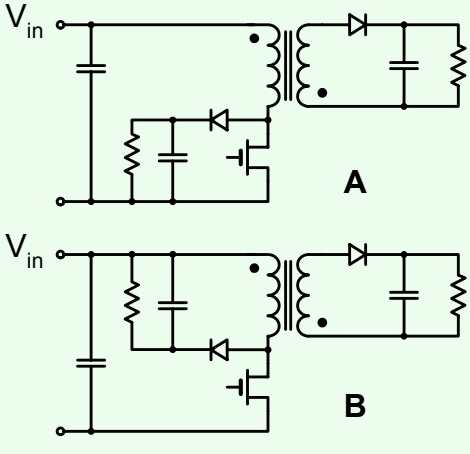


Solutions



$V_z > V_{in} + V_o' = V_{in} + nV_o$

Simple Example

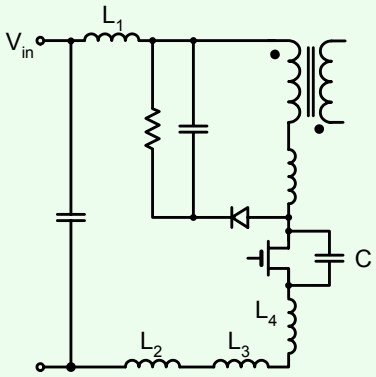


Clamp B is better from the point of view of efficiency.

$V_C(A) = V_{in} + V_o'$

But ...

Parasitic inductance

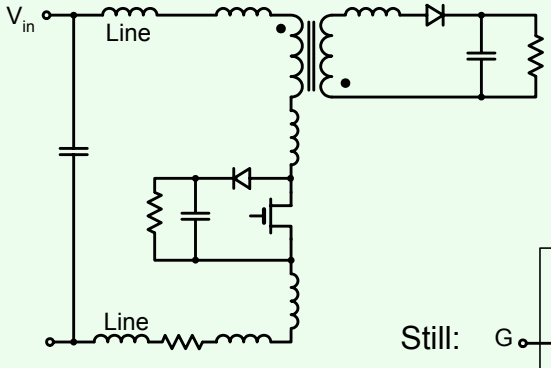


Energy of L_1 L_2 L_3 L_4 will cause high spike on C (FET). The FET is not protected!

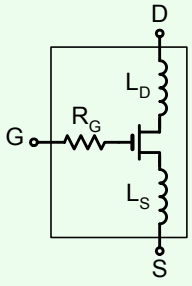
Rule:

Connect clamps and snubbers directly to the elements to be protected

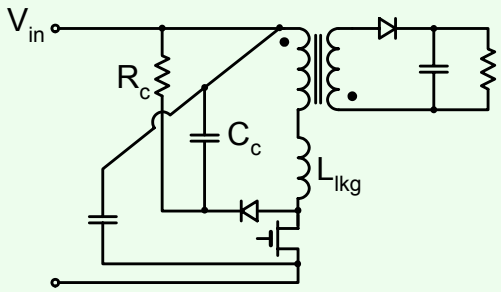
To protect FET



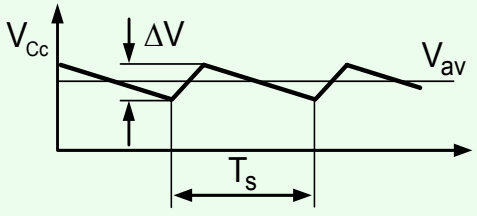
Still:

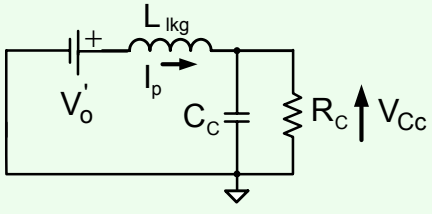


Designing the Snubber Components

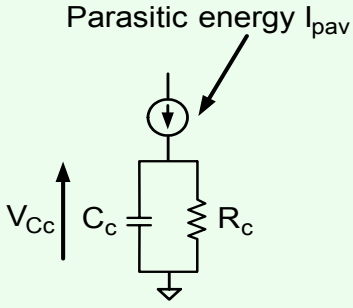


Snubber

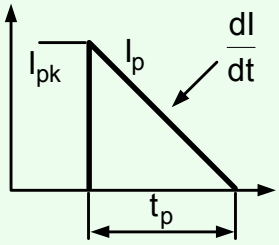




$V_{Cc} > V_o'$



Leakage discharge



$$I_{p\,av} \cdot R_c = V_{Cc\,av}$$

$$R_c \cdot C_c = T > T_s$$

$$\frac{dI_p}{dt} = \frac{V_{Cc\,av} - V_o'}{L_{lkg}}$$

$$t_p = \frac{L_{lkg} I_{pk}}{V_{Cc\,av} - V_o'}$$

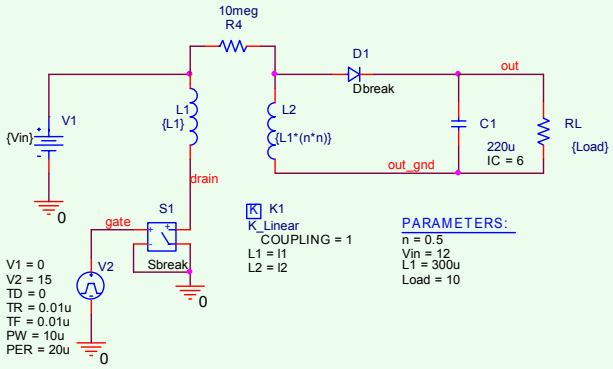
Leakage average current

$$I_{pav} = \frac{I_{pk} \cdot t_p}{2} \cdot f_s$$

Procedure

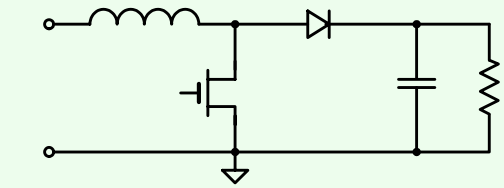
1. Select $V_{Cc\,av}$
2. Calculate $I_{p\,av}$
3. Select $R_c = \frac{V_{Cc\,av}}{I_{p\,av}}$
4. Select C_c $T > T_s$
5. Trim in-circuit

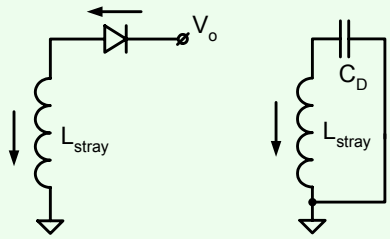
Simulation Exercise

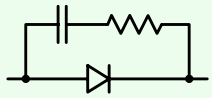


- Add 1uH leakage to Flyback converter. Design a clamp and check it by simulation.

Diode Snubber (clamp)

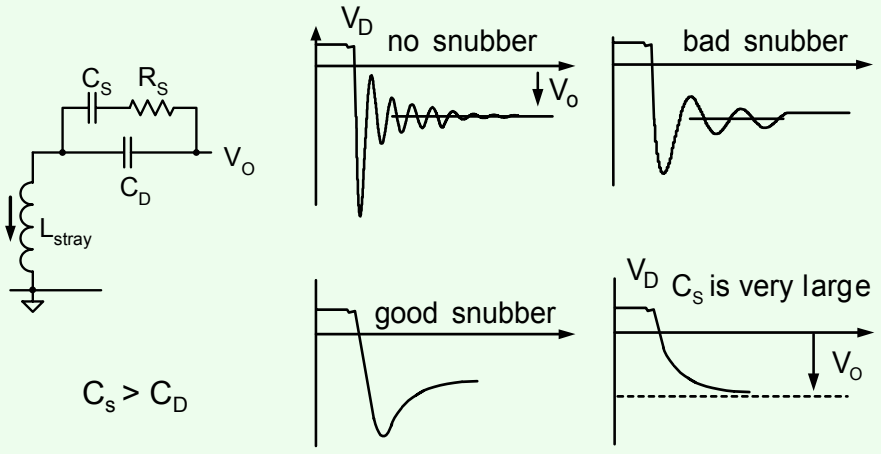






Diode Snubber

Snubber waveforms



$C_s > C_D$

Energy lost to snubber $\frac{V^2 C_S}{2}$

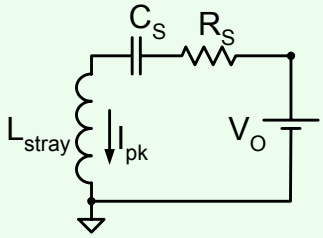
Snubber design

Design - use simulation in circuit tuning

Needed information

I_{pk} (Reverse)

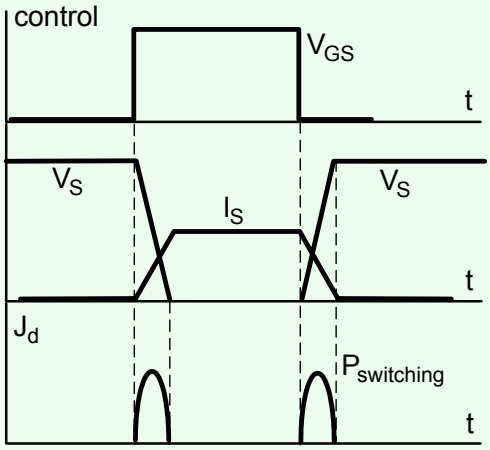
L_{stray}



$\frac{L_{stray} I_{pk}^{\ 2}}{2} \Rightarrow$ moves to $C_s \Rightarrow V_o + \Delta V$

$R_s \Rightarrow$ damping

Switch Snubbers



Switching losses due to overlap P_d linear with f_S !

Snubber types

$$\text{Snubbers} = \text{control of } \frac{dV}{dt} \text{ or } \frac{dI}{dt}$$

$\frac{dV}{dt}$ snubbers

$\frac{dI}{dt}$ snubbers

Snubber types

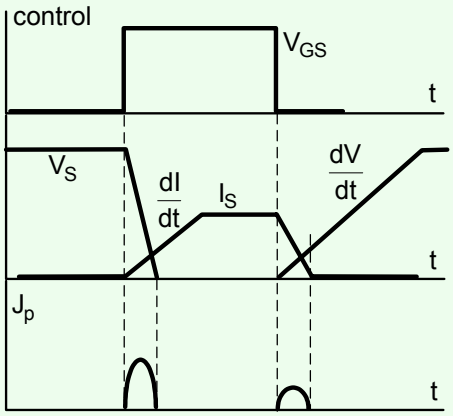
Passive (dissipative) snubber
* Energy lost to heat

Non-dissipative (lossless) snubber
* Energy recovered

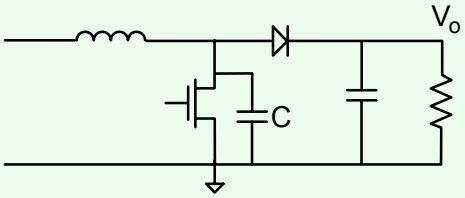
Passive Snubbers
* by passive network

Active snubbers
* by auxiliary active devices

Switching overlap

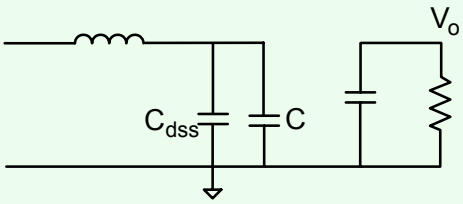


Switch Snubber



dV/dt (at turn off) can be slow down by adding external snubber capacitor C

At turn off



dV/dt

$$\frac{dV}{dt} = \frac{I}{C + C_{dss}}$$

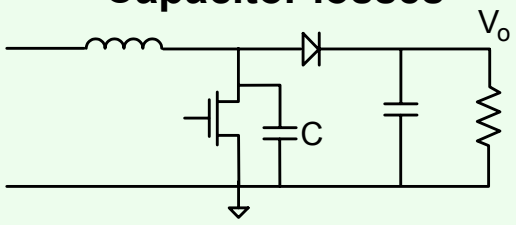
C_{dss} - output capacitance of FET

I = 1 Amp

$C + C_{dss}$= 1nF

$$\frac{dV}{dt} = \frac{1}{10^{-9}} = \frac{10^3}{10^{-6}} = 1 \ kV/\mu S$$

Capacitor losses



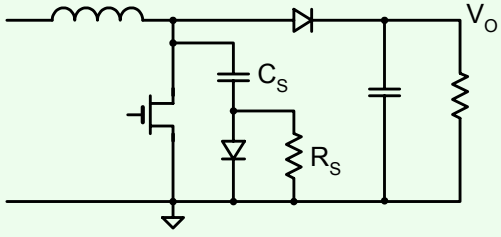
Problem at turn on ! $E_C = \frac{CV_O^2}{2}(J)$ $P_d = \frac{CV_O^2}{2} \cdot f_s$

Example : V_O = 400 V C = 1 nF

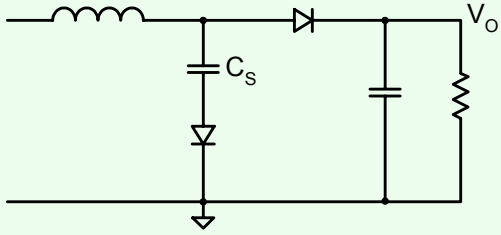
f_s = 100 kHz

$$P_d = \frac{10^{-9} \cdot 16 \cdot 10^4}{2} \cdot 10^5 = 8\,W$$

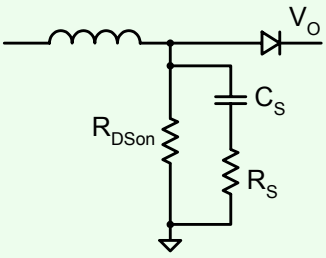
Solution



Snubbing



Reset



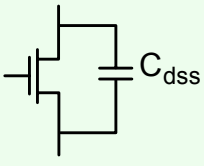
If $R_{ds\,on} < R_s$ most energy will be lost to $R_s \rightarrow$ Heat

Selection of $C_s \rightarrow$

Selection of $R_s \rightarrow$ to ensure reset

$$T = \frac{1}{R_s C_s} << t_{on} \qquad t_{on} \approx 4 R_s C_s$$

$\frac{CV^2}{2}$ Losses

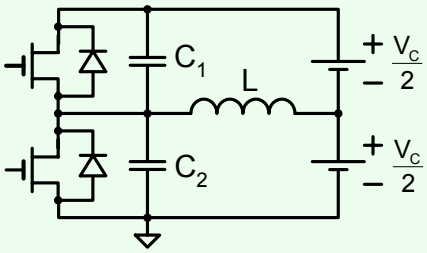


$$\left[\frac{C_{dss} V_{max}^2}{2}\right] f_s \rightarrow \text{lost to heat}$$

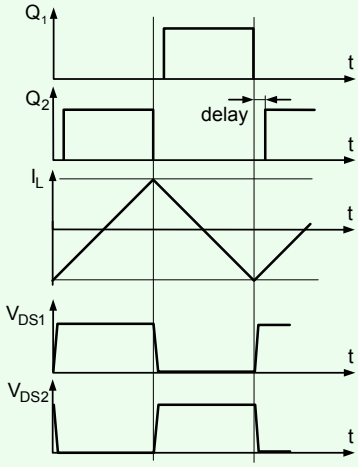
Linear with f_s !

Switching losses (overlap) also linear with f_s !

Lossless snubbing (simple example)



C_1 , C_2 of transistor plus external (if any)



Dead time requirement