

Power Converters Control Technique

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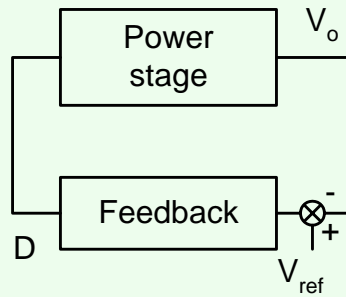
The Dynamic Problem

A closed loop converter is a feedback system

Issues:

- Stability
- Rejection of input voltage variations (audio susceptibility)
- Resistance to load changes
- Quick response to reference change - good tracking. Important for variable output voltage working in close loop.

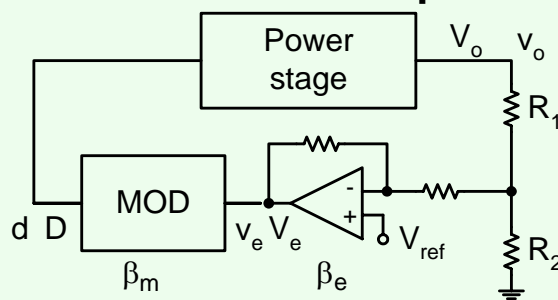
The Dynamic Problem



Power stage is a Switching system

Feedback is analog (or digital) control

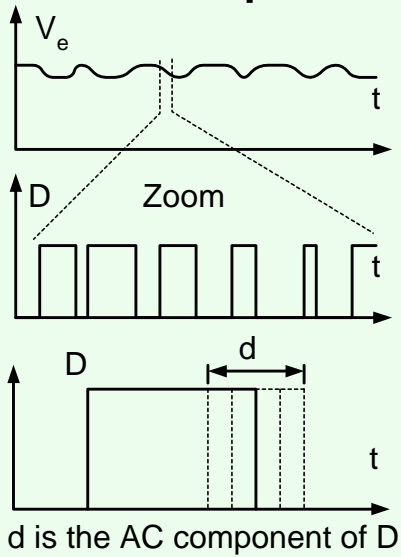
Closed Loop



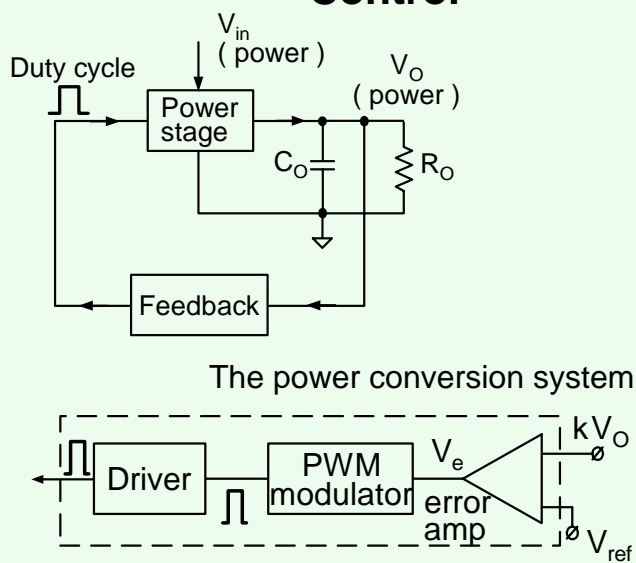
$\frac{V_o(f)}{V_e}$ – Analog Function

Feedback factor v_e (small signal) into d (small signal)

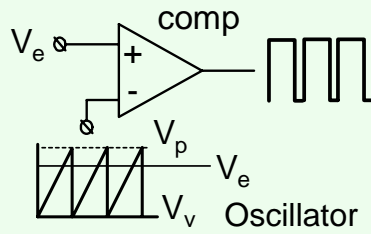
The Concept of d



Control

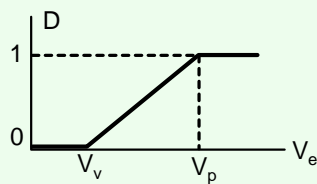


Modulator



$$V_t = \frac{(V_p - V_v)t}{T_s} + V_v$$

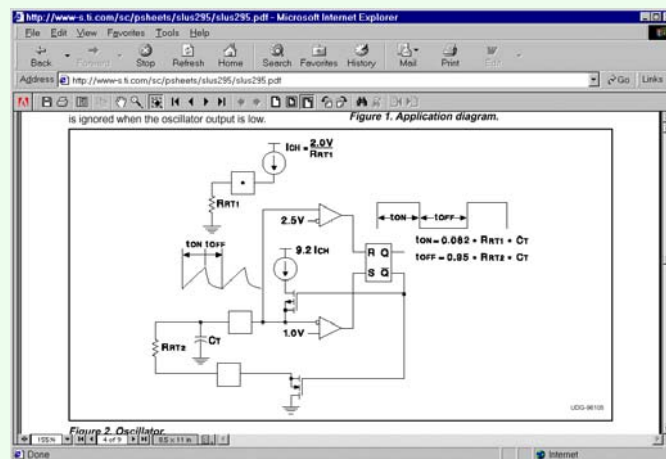
$$V_t = V_e = \frac{(V_p - V_v)t_{on}}{T_s} + V_v$$



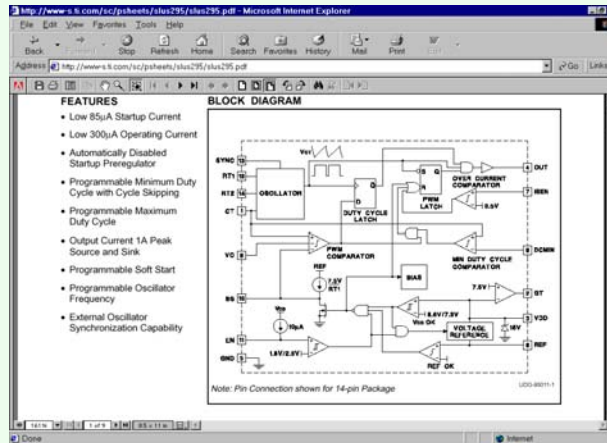
$$\frac{t_{on}}{T_s} = D_{on} = \frac{(V_e - V_v)}{V_p - V_v}$$

Practical $D_{on\ max} \approx 0.8 \div 0.9$

Oscillator



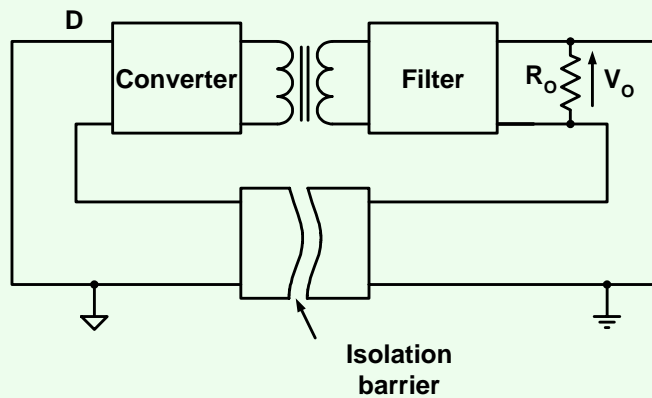
Complete controller - Voltage Mode (VM)



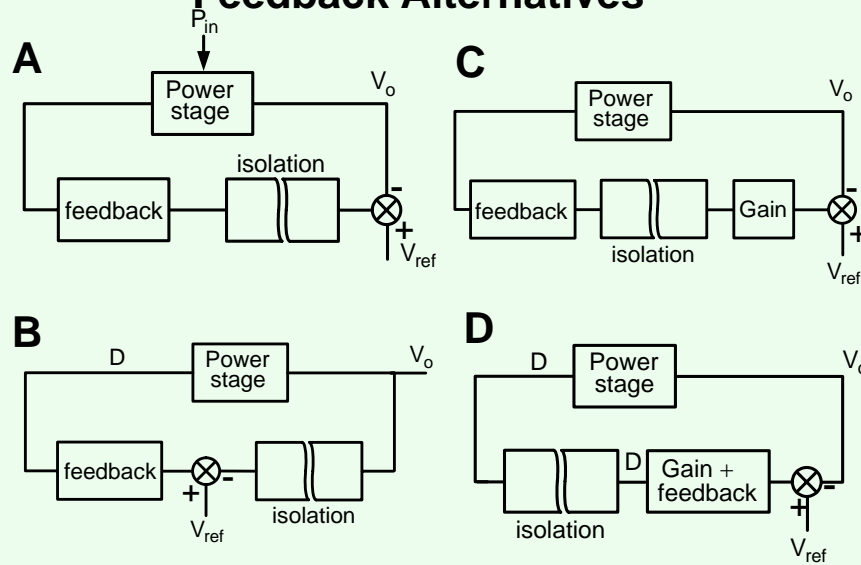
- This controller does not include an error amplifier

Primary to secondary isolation

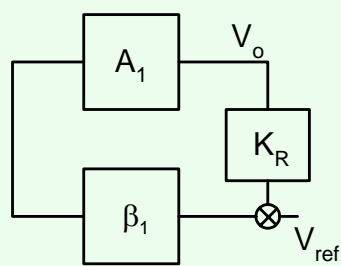
The problem :



Feedback Alternatives



Output Voltage Sampler

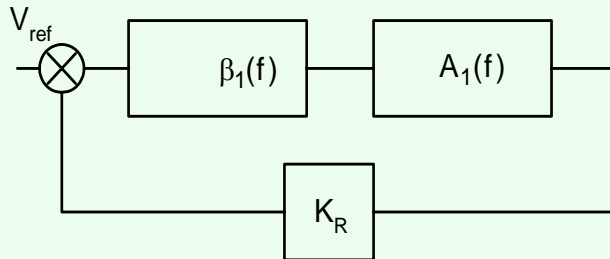


$$\left(\frac{V_o}{V_{ref}} \right) = \frac{\beta_1 A_1}{1 + \beta_1 A_1 K_R}$$

$$\beta_1 A_1 K_R > 1$$

$$\left(\frac{V_o}{V_{ref}} \right) = \frac{1}{K_R}$$

LoopGain



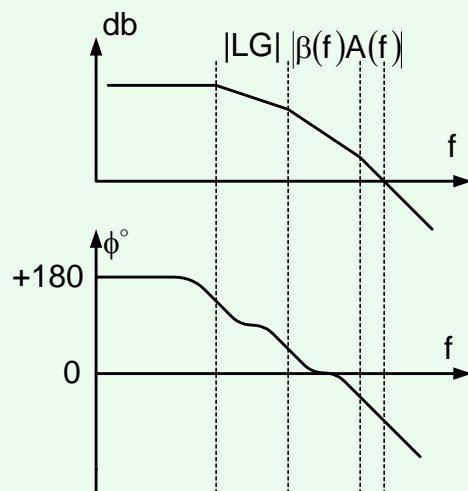
Stability and dynamic response depend on Loop Gain (LG)

$$LG = K_R \beta_1(f) A_1(f)$$

General representation

$$LG = A(f) \beta(f)$$

Bode Plot



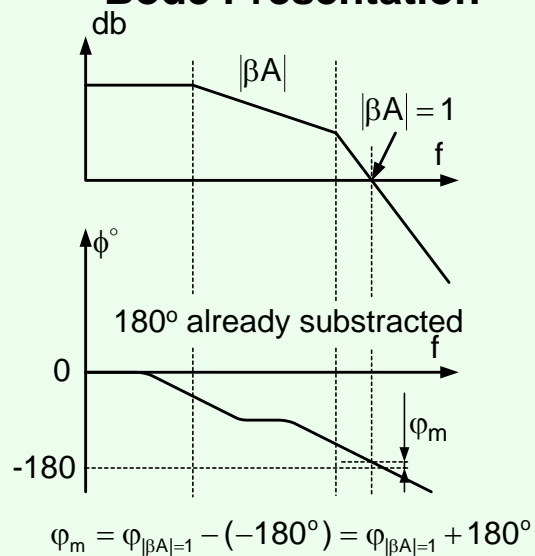
In negative feedback systems $\phi = 180^\circ (-180^\circ)$
 At $f \rightarrow 0$

Nyquist Criterion

$$A_{CL} = \frac{A(s)}{1+LG(s)}$$

- The system is unstable if $\{1+LG(s)\}$ has roots in the right half of the complex plane.
- Nyquist criterium is a test for location of $\{1+LG(s)\}$ roots.
- Nyquist criterium is normally translated into the Bode plane (frequency domain)

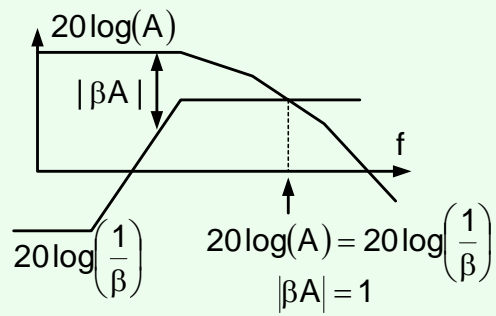
Bode Presentation



The design problem

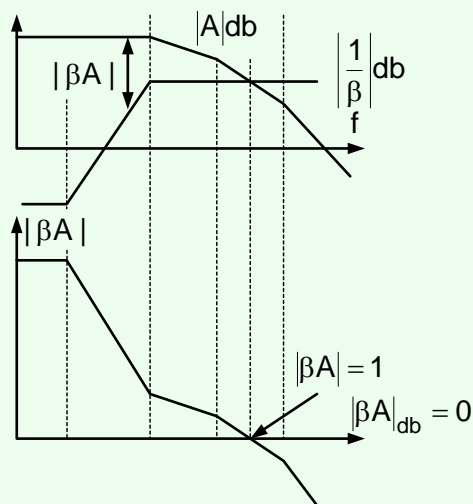
Given $A(f)$

Find $\beta(f)$

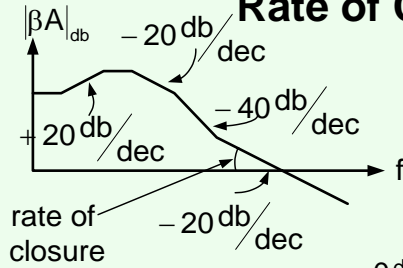


$$20\log(A) - 20\log\left(\frac{1}{\beta}\right) = 20\log(\beta A)$$

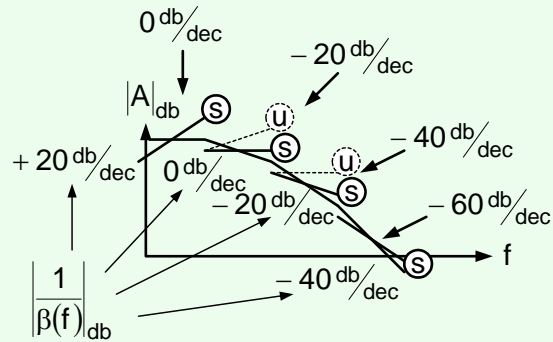
LG=1



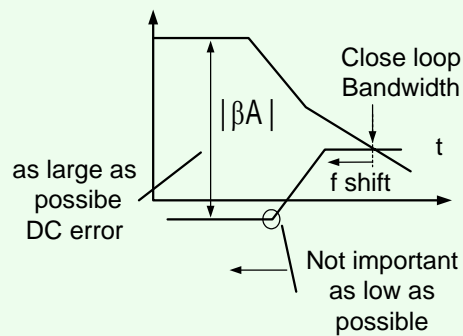
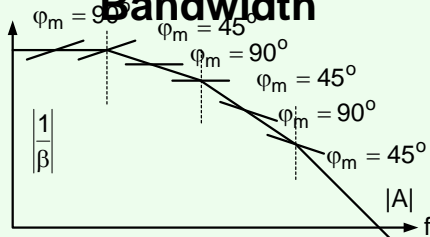
Rate of Closure



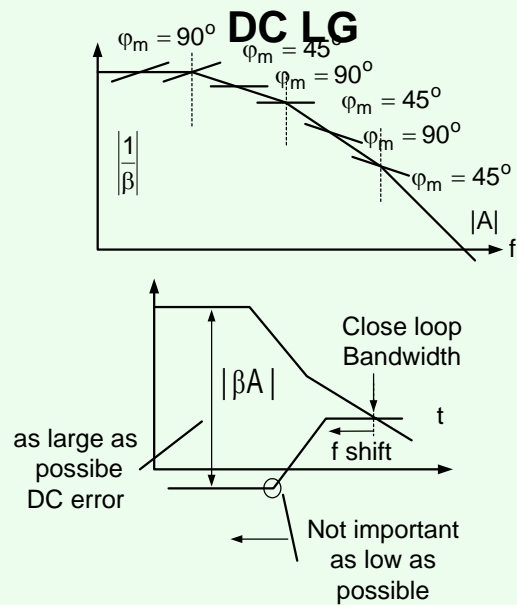
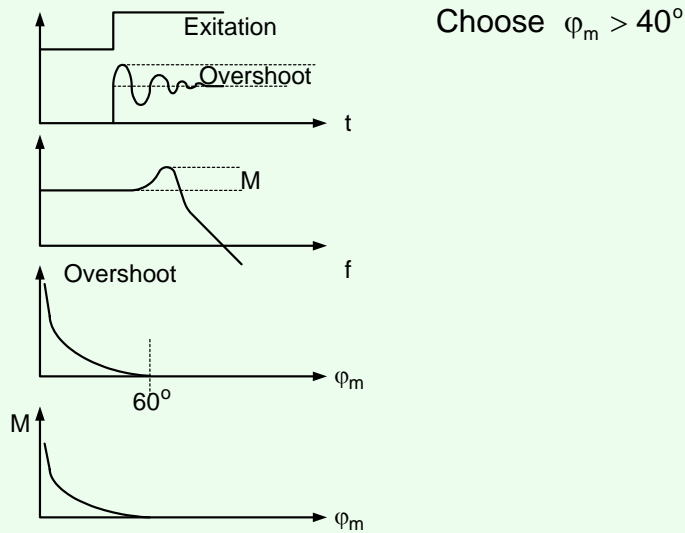
If rate of closure -20 db/dec
system is stable



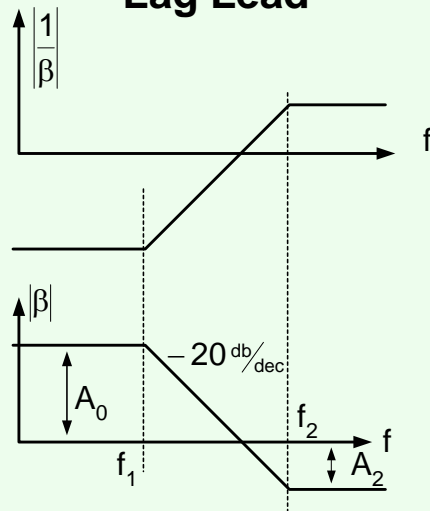
Bandwidth



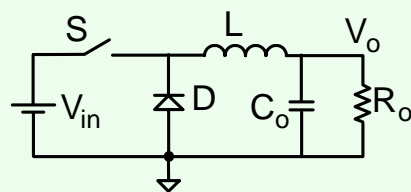
Phase Margin Effects



Lag Lead



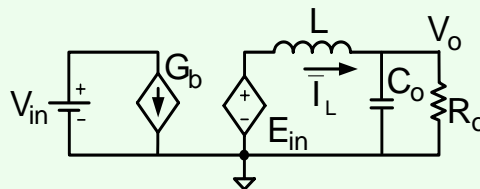
Average Model – AC Analysis



$$E_{in} = V_{in} \cdot D_{on}$$

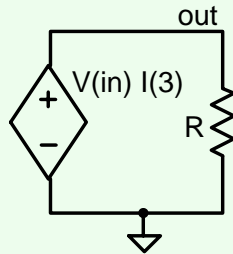
$$G_b = \bar{I}_L \cdot D_{on}$$

$$E_{in} - V_o \rightarrow \bar{V}_L$$



Polarity: (voltage and current sources) selected by inspection

Linearization

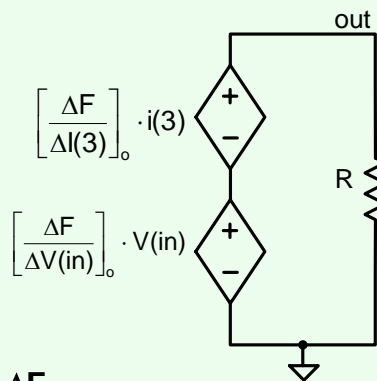
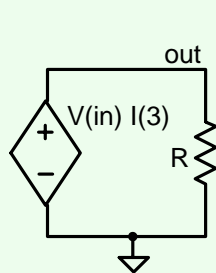


$$V(out) = V(in) * I(3)$$

$$d(V(out)) = \frac{\partial(V(out))}{\partial(V(in))} v(in) + \frac{\partial(V(out))}{\partial(I(3))} i(3)$$

$$V(out) = \frac{\Delta V(out)}{\Delta V(in)} v(in) + \frac{\Delta V(out)}{\Delta I(3)} i(3)$$

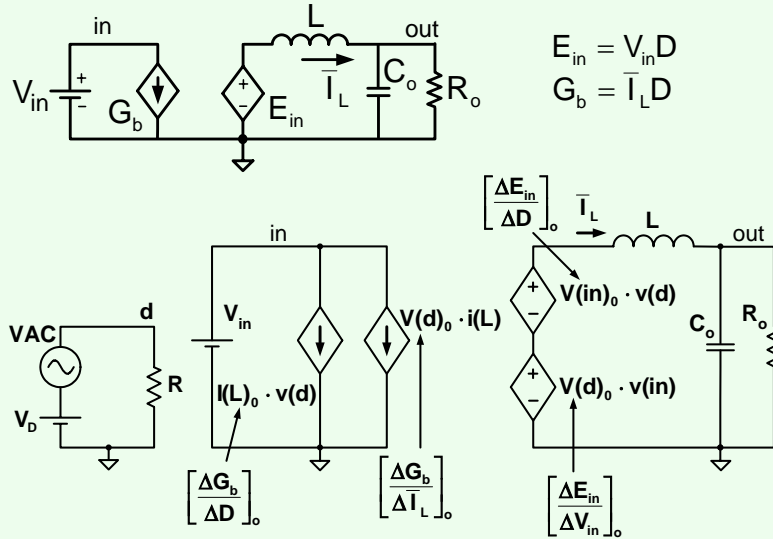
SPICE Linearization (AC Analysis)



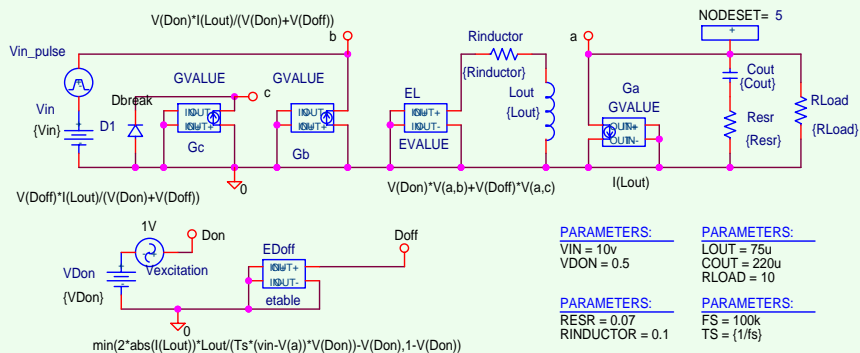
$$\frac{\Delta F}{\Delta V(in)} = I(3)_0$$

$$\frac{\Delta F}{\Delta I(3)} = V(in)_0$$

Buck linearization

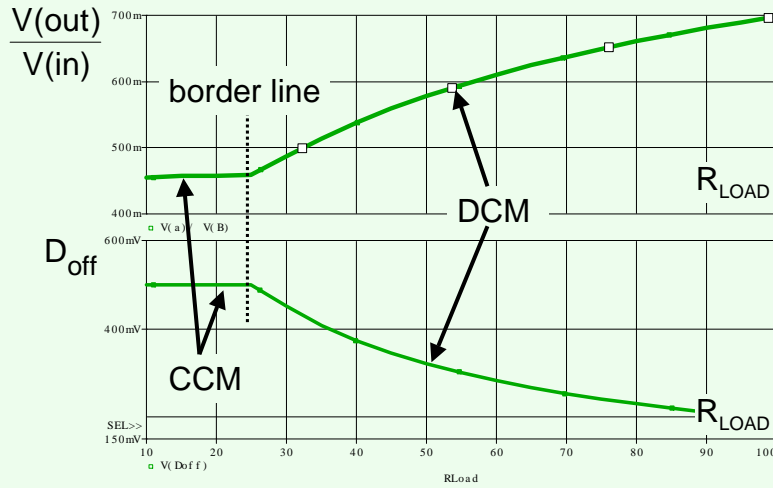


Example: Buck Average Model Simulations

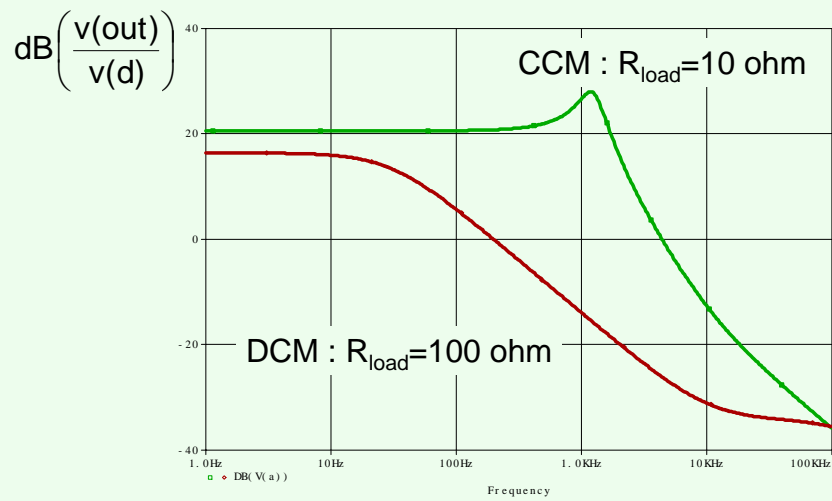


Example: Buck DC Sweep Analysis (CCM/DCM)

$$D_{on}=0.5$$



Example: Buck AC Analysis (CCM/DCM)



Buck AC Analysis (CCM/DCM) file .out

```

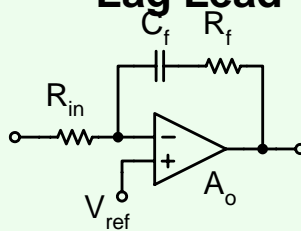
**** SMALL SIGNAL BIAS SOLUTION   TEMPERATURE = 27.000 DEG C
**** CURRENT STEP                 PARAM RLOAD = 10
*****
NODE VOLTAGE  NODE VOLTAGE  NODE VOLTAGE  NODE VOLTAGE
( a) 4.5455   ( B) 10.0000   ( C) -0.8182   ( DON) .5000
(Doff) .5000 (N00069) -0.0455 (N00141) 0.0000 (N000071) .5000 (N000230) 0.0000

VOLTAGE SOURCE CURRENTS
NAME      CURRENT
V_Vexcitation 0.000E+00
V_VDon      0.000E+00
V_Vin      -2.273E-01

**** CURRENT STEP                 PARAM RLOAD = 100
*****
NODE VOLTAGE  NODE VOLTAGE  NODE VOLTAGE  NODE VOLTAGE
( a) 6.9835   ( B) 10.0000   ( C) -0.7340   ( DON) .5000
(Doff) .1945 (N00069) -0.0070 (N00141) 0.0000 (N000071) .5000 (N000230) 0.0000

VOLTAGE SOURCE CURRENTS
NAME      CURRENT
V_Vexcitation 0.000E+00
V_VDon      0.000E+00
V_Vin      -5.028E-02
    
```

Lag Lead



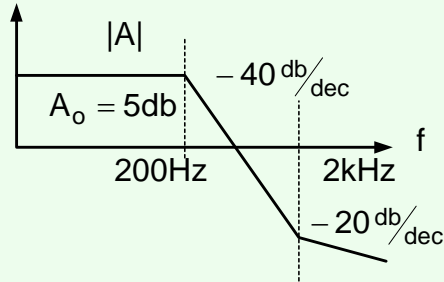
$$A_o = A_{OL} \text{ (ampl.)}$$

$$f_L = \frac{1}{2\pi C_f R_f}$$

$$A_2 = \frac{R_f}{R_{in}}$$

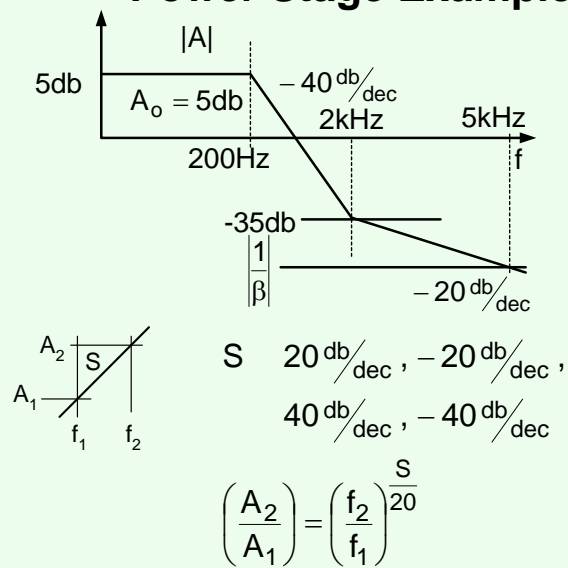
Exercise

Given



Design β and feedback circuit for $f_{el}=5\text{kHz}$

Power Stage Example



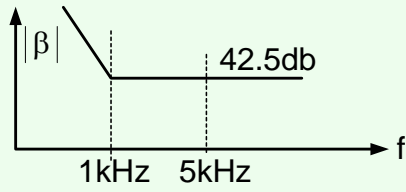
Pole Zero

$$\frac{A_1}{A_2} = \left(\frac{5}{2}\right)^{-1}$$

$$A_2 = A_1 \left(\frac{2}{5}\right)^1$$

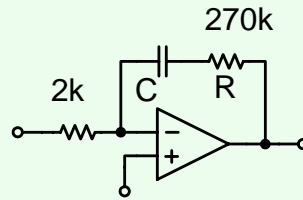
$$A_{2_{db}} = A_{1_{db}} + 20 \lg\left(\frac{2}{5}\right)$$

$$A_{2_{db}} = 35 + (-7.5) = -42.5 \text{db}$$

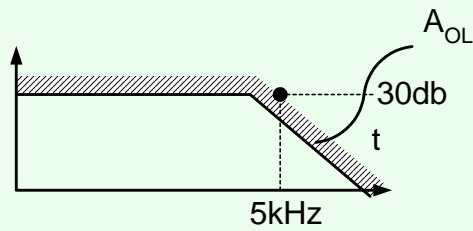


$$C = \frac{1}{2\pi R 1\text{kHz}} = 0.59 \text{nF}$$

$$\frac{1}{2\pi RC} = 1\text{kHz}$$

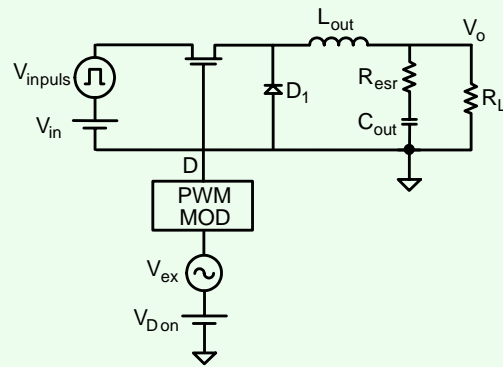


Problem?

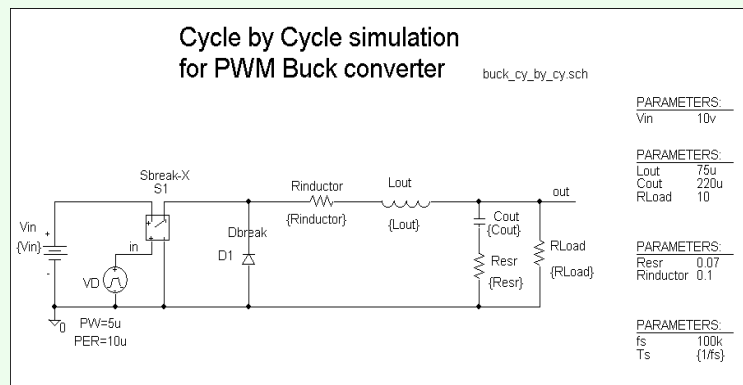


Operational amplifier limitation

Buck



File: Buck_cy_by_cy.SCH

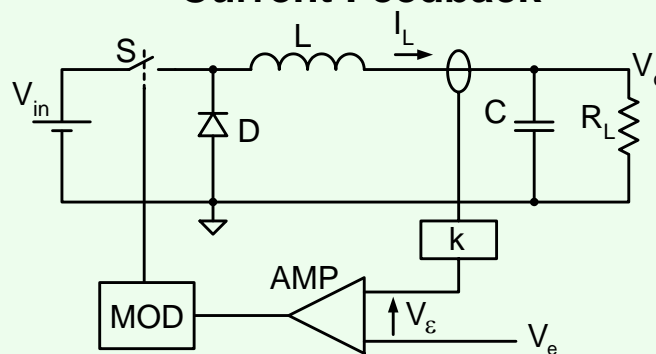


Current Feedback

- The problem: transfer function is second order
- Solution: Add current Feedback

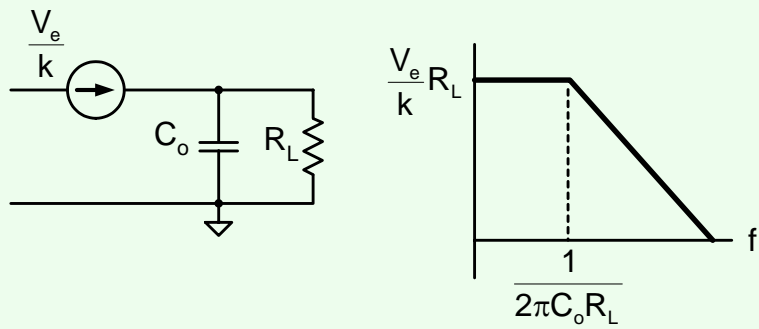
System order is reduced for each state variable feedback

Current Feedback



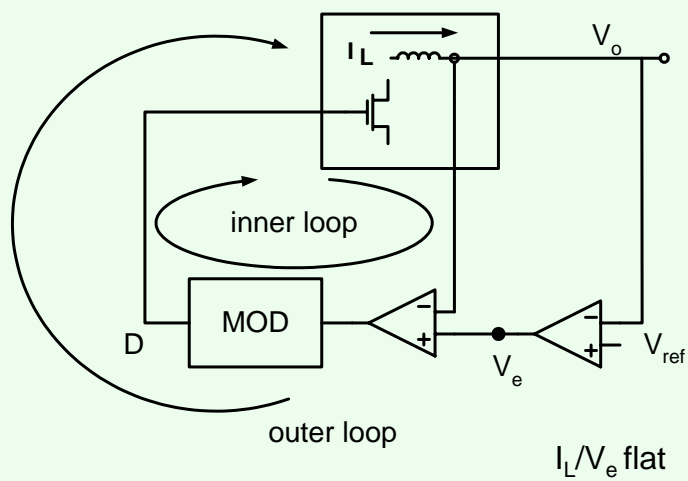
- For strong feedback ($A_{OL} \gg 1$):

$$I_L = \frac{1}{k} V_e \quad (V_\epsilon \rightarrow 0)$$

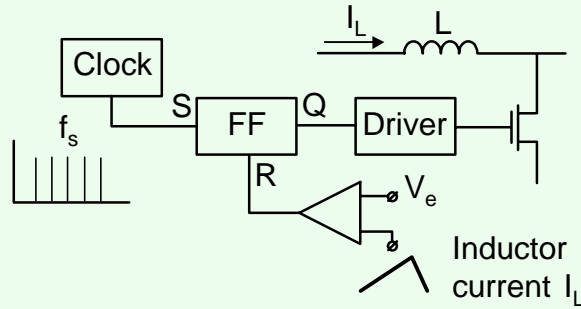


- First order system !

PCM & ACM

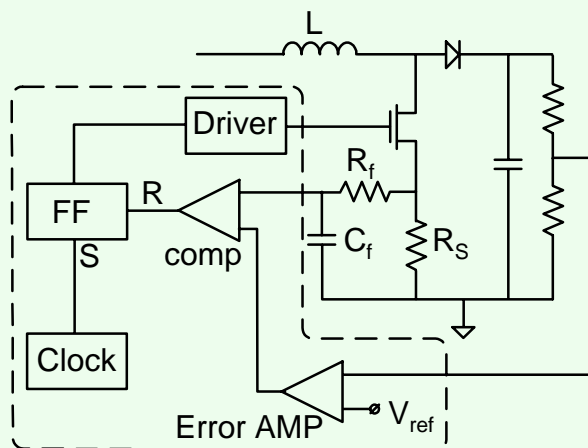


Current mode (CM) control



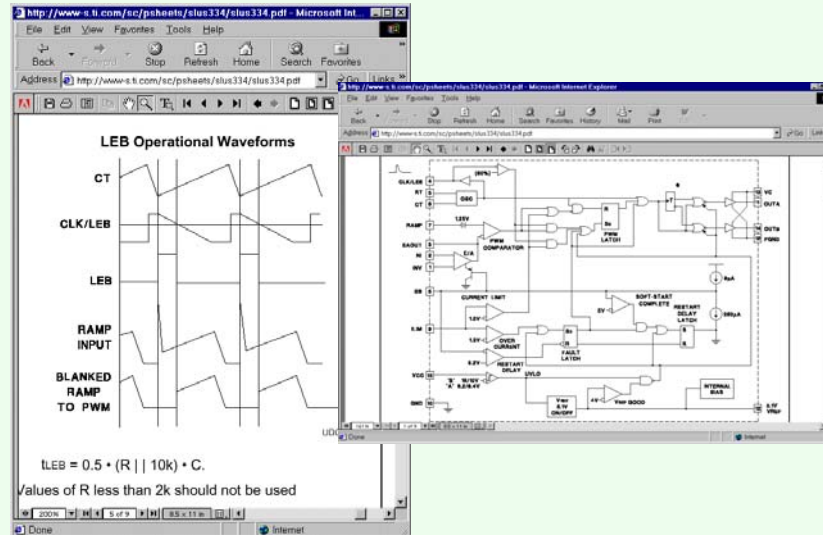
$$\frac{V_o}{V_{in}} = f(D_{on}) \text{ is the same !}$$

Implementation CM Boost



Some controllers have amplifiers for sensed current

CM Controller



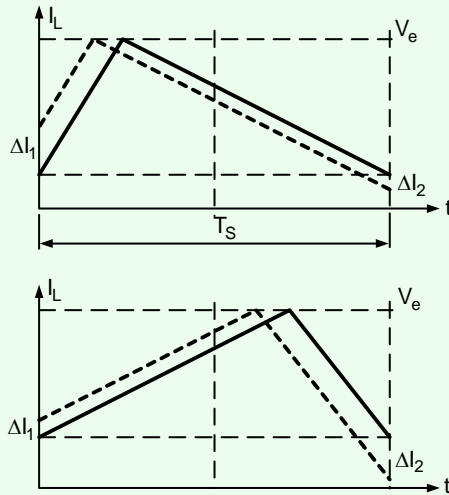
Advantages of peak CM (PCM)

- * Cycle by cycle protection
- * Better dynamics

Disadvantages

- * Loading edge spike
- * Subharmonic oscillation

The nature of Subharmonic Oscillations

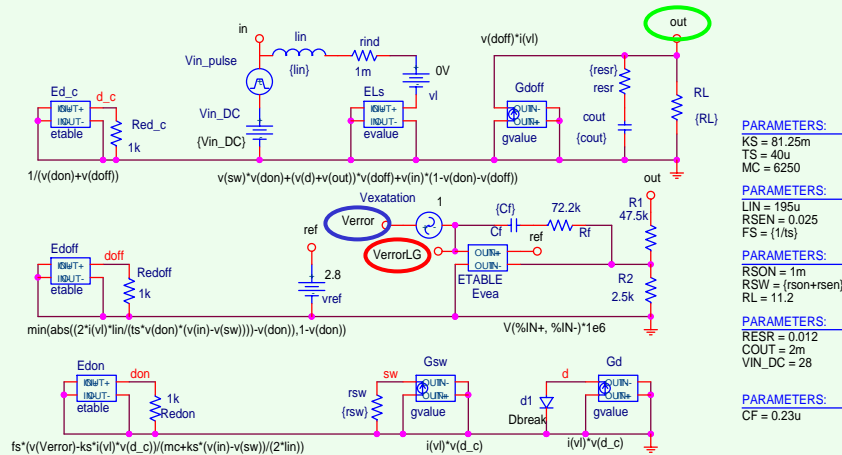


The geometric explanation

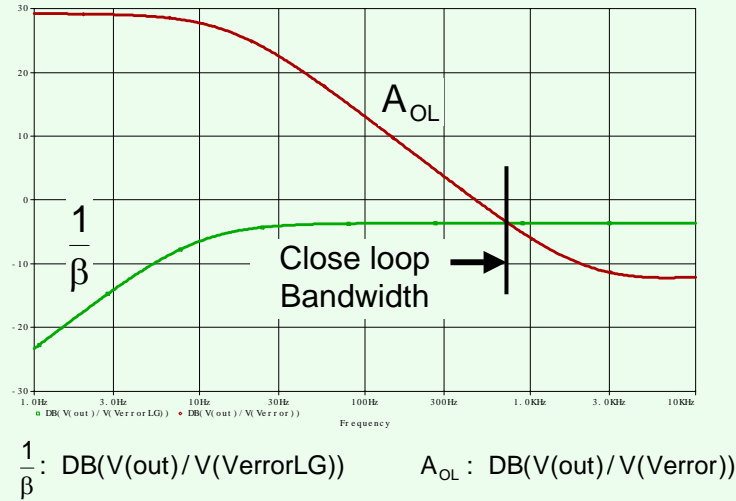
$$D < 0.5 \quad \Delta I_2 < \Delta I_1$$

$$D > 0.5 \quad \Delta I_2 > \Delta I_1$$

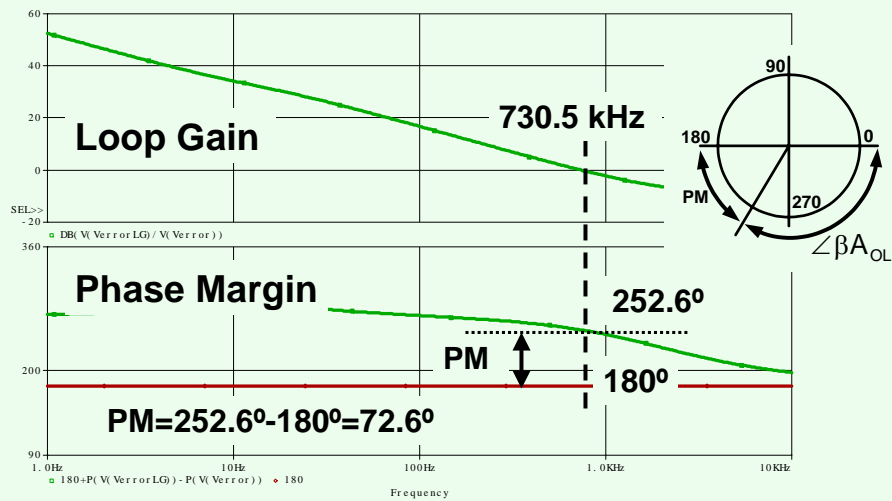
BOOST Average Model AC analysis PCM (CCM & DCM)



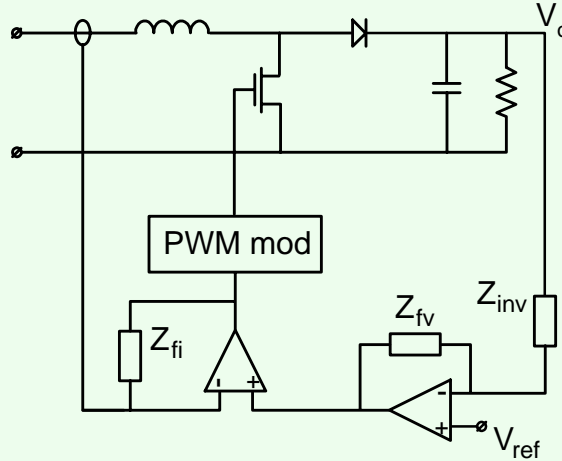
BOOST Average Model Simulation



BOOST Average Model Simulation

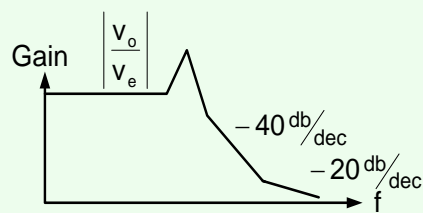


Average Current Mode (ACM) Control

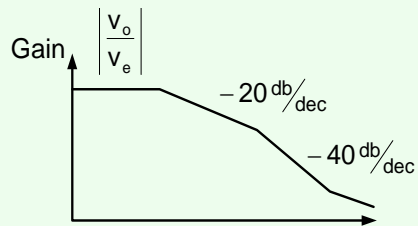


Current is filtered first to take out high frequency (f_s)

The advantages of current feedback (PCM or ACM)

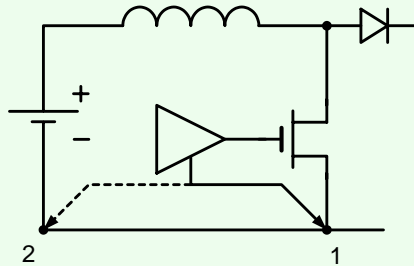


Typical power stage VM



Same power stage (outer loop) with CM

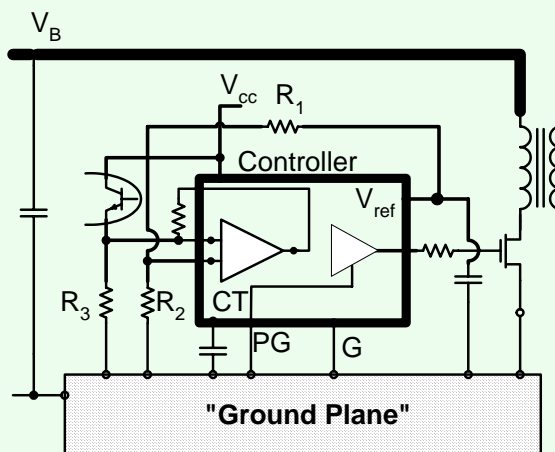
Parasitic effects: PCB trace resistance



$$V_1 \neq V_2$$

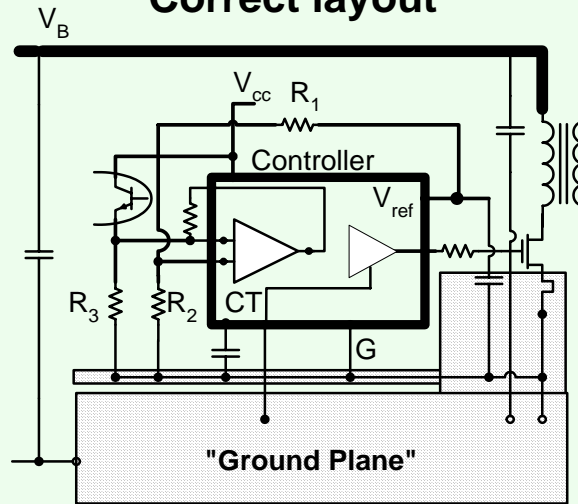
Ground Noise

Separate power ground from signal ground



This circuit will probably not work. Why ?

Correct layout

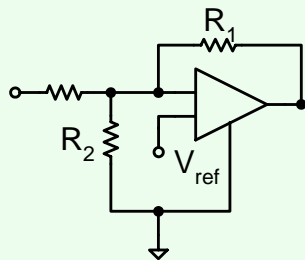


Do not rely on "Ground Plane"

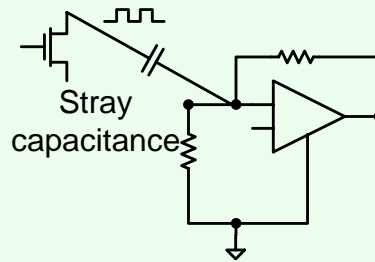
Schottky Diodes

The screenshot shows a PDF document with a circuit diagram and text. The diagram is divided into two main sections: "TO ANALOG CIRCUITRY" and "POWER STAGE". The "TO ANALOG CIRCUITRY" section shows a signal path with nodes labeled CT , $VREF$, and GND . The "POWER STAGE" section shows a power path with nodes labeled VCC , OUT , $POND$, and GND . A Schottky diode is connected between the OUT and $POND$ nodes. The diagram also shows a transformer and a capacitor labeled C_{MAX} . The text below the diagram describes an "Open Loop Test Circuit" and mentions the use of Schottky diodes for exercising functions and measuring their specifications. The text states: "This test fixture is useful for exercising many of the UC3823A,B, UC3825A,B functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should likewise be bypassed to the signal ground with a good high frequency capacitor. The use of a ground plane is highly recommended." The PDF viewer interface is visible at the top and bottom of the screenshot.

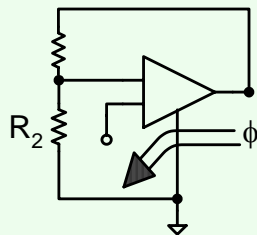
Parasitic effects: Interfering signal injection



Sensitive Part-Capacitive coupling



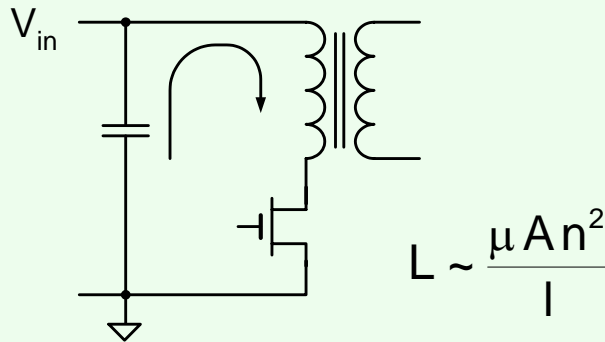
Parasitic effects: Inductive coupling



Do not put sensitive elements close to high voltage pulses or close to magnetic elements

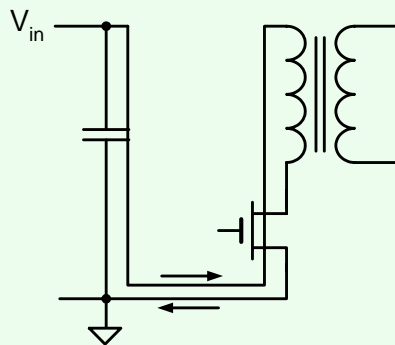
Current Loop Area

Avoid wide power line loops



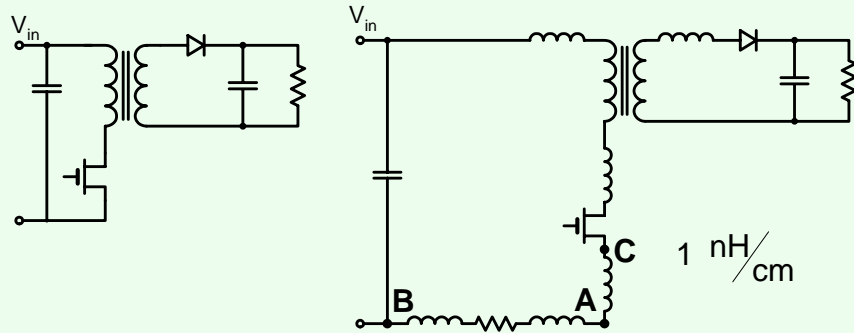
Stray inductance is proportional to area. So is the radiated wave.

Loop Area



Best way is to run the forward-return paths on two sides of the PCB

Parasitic effects: Stray inductance



Two points on power PCB trace will never have same potential $V_A \neq V_B \neq V_C$