Control Design of PWM Converters: From Analog to Digital

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Motivation

- Most switch mode systems need to operated in closed loop
- Performance largely dependent on the Compensator (feedback) design
- Loop control design is conceived as “black magic” OR requiring tedious analytical derivations
- Digital control is becoming relevant
Objective

- To present a user friendly version of control loop design including both analog and digital control
- Based on:
  - Intuition
  - Simulation
  - Simple calculations

Outline

1. Basics of feedback theory and graphical representation
2. Relationship between LoopGain and dynamic response
3. PWM converters as feedback systems
4. Voltage Mode (VM) control
5. Current Mode (dual loop) control
6. Simulation tools
7. Average models
8. Analog compensator networks
9. Digital control
10. Recent research results
11. Q&A
1. Basics of feedback theory and graphical representation

Block diagram of a feedback systems (one loop)

\[ A_{CL} = \frac{S_o}{S_{in}} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}} \]

\[ LG \equiv \beta A_{OL} \]

\[ \frac{S_o}{S_{in}} = \frac{1}{\beta} \]

\[ \frac{S_o}{S_{in}} = A_{OL} \]
Block Diagram

\[ A_{CL} = \frac{S_o}{S_{in}} = \frac{H_1 P}{1 + H_1 H_2 K P} \frac{1}{\text{LG}(f)} \]

Effect of Feedback

\[ A_{CL} = \frac{S_o}{S_{in}} = \frac{P}{1 + H_2 PK} \frac{1}{\text{LG}(f)} \]

\[ A_{CL, \text{LG}(f)\gg1} = \frac{1}{H_2 K} \]
**PWM Converter**

Power

$V_{in}$

$V_o$

$V_{ref}$

$R_1$

$R_2$

$R_3$

$C$

MOD

$\beta_m$

$V_o$

$V_{ref}$

$\beta_e$

$\theta$

**Block diagram concepts**

$A_{CL} = \frac{S_o}{S_{in}} = \frac{H_1 P}{1 + H_1 PK \ LG(f)}$

$A_{CL|_{LG(f)>1}} = \frac{1}{K}$
Audio susceptibility

\[
S_o \quad \frac{H_2}{V_{in}} \quad 1 + LG
\]

But loop gains are equal: \( \text{LG}(f) = H_1 K \)
Block diagram division

\[ \text{LG}(f) = AB \]

A – known (power stage + divider)
B – unknown (have to be designed)

Graphical representation of BA
conventional method

- Tedious – need to re-plot BA
- Analysis (not design) oriented
- Requires iterations
Graphical Representation of BA

\[ 20 \log A - 20 \log \frac{1}{B} = 20 \log (BA) \]

\[ 20 \log A - 20 \log \frac{1}{B} \Rightarrow B \cdot A = 1 \]

Stability of Feedback System

\[ H(s) = \frac{b_m s^m + b_{m-1} s^{m-1} + \ldots + 1}{a_n s^n + a_{n-1} s^{n-1} + \ldots + 1} \]

- \( \circ \) - Zero
- \( \times \) - Pole

- RHP solutions include the term \( \sin(\omega t)e^{\alpha t} \)
Stability Criterion

\[ A_{CL} = \frac{H_1 K}{1 + LG(f)} \]

- The system is unstable if \(1 + LG(f)\) has roots in the right half of the complex plane.
- Nyquist criterion is a test for location of \(1 + LG(f)\) roots.
- Nyquist criterion is normally translated into the Bode plane (frequency domain)

Nyquist

- Stable
Nyquist

- Oscillatory

Nyquist

- Unstable
- The culprit: Phase Lag
- Phase Lead in LG can help stabilize a system
\[ \varphi_m = \varphi_{|BA|=1} - (-180^\circ) = \varphi_{|BA|=1} + 180^\circ \]
Minimum Phase Systems
no Right Half Plane Zero (RHPZ)

Rate of closure (ROC)
(minimum phase systems)
Application of the $1/B$ curve
Rate of closure

- Rate of closure of BA is the difference between the A and B slopes
- No need to re-plot BA
- Design oriented approach

Stability Criterion

If rate of closure $-20 \text{dB/dec}$ system is stable
Phase Margin Examples

For minimum phase systems history is not important
Approximate Phase Margin Calculation

- Get the accurate phase at intersection by simulation

Design Steps

- Draw A
- Select cross point of BA (<< than \( f_s/2 \), for PWM)
- Select B shape
Stability of a Source-Load System

- $Z_L \rightarrow$ negative resistance

System stability

\[ \text{LoopGain} = \frac{1}{Z_S} Z_L \]

Convenient way to examine the LG stability is the Nyquist stability test
2. Relationship between Loop Gain and dynamic response

\[
A_{CL} = \frac{1}{K} \frac{s^2}{\omega_0^2} + \frac{1}{s} + \frac{1}{\omega_0 Q + 1} \quad \text{for } \phi_m \leq 50^\circ
\]

\[
A_{CL} = \frac{1}{K} \frac{s}{\omega_0} + 1 \quad \text{for } \phi_m \geq 50^\circ
\]

- For small \( \phi_m \), \( A_{CL} \) behaves as a second order system.

Response in Closed Loop
Overshoot and Q in Closed Loop in Response to step in $S_{in}$

$$Q \approx \frac{\cos \varphi_m}{\sin \varphi_m} \quad \text{for} \quad \varphi_m < 50^\circ$$

Design target $\varphi_m \geq 45^\circ$

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Load-Step Response

$$\frac{S_{out}}{\Delta I} = \frac{Z_O}{1 + A \cdot H_1 \cdot K} \frac{Z_O}{L_G}$$

- Small-signal output impedance
Load-Step Response

- Affected by:
  - Output impedance
  - ESR of output capacitor
  - Slew rate of inductor

Output Impedance (Immunity to load changes)

\[
Z_{of} = \frac{V_{out}}{\Delta i_o} = \frac{Z_o}{1 + \frac{AB}{LG}}
\]

- Buck converter – small signal
Audio-Susceptibility (Line Regulation) (Immunity to input voltage changes)

\[ \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{H_2}{1 + LG(f)} \]

- Large LG reduces susceptibility

Steady-state (DC) Error

\[ S_c = \frac{S_{\text{in}}}{1 + LG} \]

- \( S_c \) is the offset between the sampled output and reference
- Small DC error for large LG(0)
Dynamic Response Summary

- Systems that have a slope of −20 db/dec are easy to control
- Response is largely determined by LG(f)
- Desired LG:
  - LG as large as possible at low frequencies (small DC errors)
  - LG of large BW - intersection point of A and 1/B (quick response, fast recovery, rejection of Vin changes)
- Phase margin > 45° (reasonable overshoot)

The culprit: Phase delay in LG

Nyquist

Design target $\phi_m \geq 45^\circ$
3. PWM converters as feedback systems

**Issues:**

- Stability
- Rejection of input voltage variations (audio susceptibility)
- Immunity to load changes
- Quick response to reference change - good tracking.

**PWM converter in closed loop**

- Small signal responses
- Linearization around operating point
**Type of Blocks**

**Small Signals (Perturbation) Responses**

- Power stage is a Switching System (may be non linear)
- Feedback is an analog or digital controller
- Modulator: mixed mode
- Linear control theory based design → small signal response

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**Small-Signals (Perturbation) Responses**

- Analytical solutions
- Simulation
  - Injection of sinusoidal perturbation
  - AC analysis of behavioral average model

- This seminar promotes the simulation approach
Small signal response of the modular

- Relationship between $v_e$ and $d$ ($K_m = d/v_e$)

Small $d$

$d$ is the AC component of $D$
Modulator

\[ V_t = \frac{(V_p - V_v) t}{T_s} + V_v \]

\[ V_t = V_e = \frac{(V_p - V_v) t_{on}}{T_s} + V_v \]

\[ t_{on} = D_{on} = \frac{(V_e - V_v)}{V_p - V_v} \]

\[ d = \frac{V_e}{V_p - V_v} - \frac{V_e}{V_a} \]

\[ K_m = \frac{d}{Ve} = \frac{1}{Va} \]

THE CONTROL DESIGN PROBLEM

- **A** → Power Stage; **B** → compensator
4. Voltage mode (one loop) control

Block diagram

The power conversion system
Buck small-signal frequency response (CCM)

Buck frequency response (CCM)

- Second order plus zero due to ESR of \( C_o \)
**Dependence on $V_{in}$**

- **$V_{in}$**: 5V, 10V, 15V

- **Magnitude**
- **Phase**

**Effect of Load**

- **$R_L$**: 10Ω - CCM, 50Ω - DCM, 100Ω - DCM
Buck Derived Converters

- Forward
- Half bridge (HB)
- Full Bridge (FB)

- Simulation is the simplest way to obtain the transfer functions

Boost Power Stage
Small signal response

- RHPZ – non minimum-phase system
CM Boost

- $20 \text{ dB}(V_{\text{OUT}} / V_{\text{error}})$
- $20 \text{ dB}(V_{\text{OUT}} / V_{\text{error}})$
- $10 \text{ Hz}$, $100 \text{ Hz}$, $1 \text{ kHz}$, $1 \text{ MHz}$

Buck-Boost (Flyback) Power Stage

- RHPZ – non minimum-phase system
5. Current Mode (dual loop) control

Current Feedback

- The problem of voltage mode control: Transfer function is second order
- Solution: Add current Feedback

- System order is reduced for each state variable (inner loop) feedback
The effect of current feedback

For ‘strong’ feedback

\[ LG >> 1 \quad v_e \rightarrow 0 \]
\[ i_o = \frac{1}{N} v_e \]

Transfer function with closed Current Loop

- First order system!
Current Mode

![Circuit diagram for Current Mode](https://via.placeholder.com/150)

- **Flat**: \( \frac{V_o}{V_e} \)
- **First order**: \( \frac{V_o}{V_e} \)

The advantages of current feedback

![Gain plots](https://via.placeholder.com/150)

- **Typical power stage VM**
  - Gain: \( \frac{V_o}{V_e} \)
  - Frequency: \( f \)
  - Roll-off: \(-40 \text{db/dec}, -20 \text{db/dec}\)

- **Same power stage (outer loop) with CM**
  - Gain: \( \frac{V_o}{V_e} \)
  - Roll-off: \(-20 \text{db/dec}, -40 \text{db/dec}\)
7. Peak Current Mode (PCM) control

PCM Modulator

\[
\frac{V_o}{V_{in}} = f(D_{on}) \text{ is the same!}
\]
Implementation CM Boost

Some controllers have amplifiers for sensed current

The nature of Subharmonic Oscillations

The geometric explanation

- $D < 0.5 \quad \Delta I_2 < \Delta I_1$

- $D > 0.5 \quad \Delta I_2 > \Delta I_1$

*For $D > 0.5$ need slope compensation*
Extra delay in PCM (Ridley)

- PCM is a current sampling process
- Subject to sampling delay
- Delay was derived by Ray Ridley
- Important for frequencies above $f_s/10$
- Mostly of theoretical importance

Average Current Mode (ACM) Block diagram

- Current sample is filtered first attenuate high frequency ($f_s$)
PCM and ACM

- Both are current feedbacks
- Both reduce the order of system
- The difference is in BW of the current feedback loop
- Both increase the output impedance

Advantages of peak CM (PCM)

- Cycle by cycle protection
- Better dynamics

Disadvantages

- Leading edge spike
- Subharmonic oscillations
6. Simulation tools

- General purpose simulators
- Dedicated simulators
- PC and web based simulators

- This seminar promotes PC based general purpose simulators

Why Simulation

- Most control design methods apply graphical representations of transfer functions
- One can get the plots from analytical expressions or by simulation
- Simulation is the easiest way to get “A” (the small signal response of the power stage)
**Computer Simulation of Power Conversion Systems**

- Switch-Mode Converters
  - Average Modeling
    - Analog Simulation (SPICE, Saber, etc.)
      - Large Signal
      - DC
      - Small Signal
    - Discrete Simulation (MATLAB, ACSL, etc.)
    - Symbolic Analysis (MATHEMATICA, MACSYMA, etc.)
      - Analytical Expressions
      - Voltage, Current Stresses
      - Voltage, Current Ripples
      - Large Signal
  - Cycle by Cycle
    - Analog Simulation
      - Closed Loop Response

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**Desired Simulator’s Features for Power Electronics Systems**

- Convergence
- Physical models
- Small signal analysis
- Interfaces
- Run time
- Behavioral models
- Statistical and optimization analysis
- Discrete domain simulation capabilities
Some Popular Modern Simulators

SPICE Based (Berkeley)
- PSPICE – MicroSim - Orcad - Cadence
- ICAP/4 – Intusoft
- MICROCAP - Spectrum

Others
- PSIM - Powersim
- Simploter -Ansoft
- PLECS -Plexim

Power IC Models Library
- AEi – Design Automation

PSPICE – The Physical Simulator
- Most popular
- SPICE based simulator (Berkley)
- Used extensively for circuit simulation
- Extensive physical models libraries
- Behavioral models (ABM)
- AC analysis
- Statistical analysis
- Optimization tool
- Some PWM models
- MATLAB/Simulink interface
Working with PSPICE

PSPICE Convergence Problems

- Very common in switched circuits simulation
AEi Power IC Library

- PWM controllers are not included in PSPICE libraries
- AEi’s library supports Power Electronics
  - 150 SPICE Models for Popular Power ICs
    - Regulators, Controllers, Switchers
    - FET Drivers
  - Support for Capture and Schematics
    - Symbols
    - Example Applications schematics/simulations
    - Documentation

PSIM - The Switching Circuit Simulator

- Disregards switching instances
- Fast and effective time domain algorithm
- Constant time step approach
- Transient (time domain) based AC analysis
- User friendly intuitive interface
- Generic models: passive, switchers, motors
- Analog Behavior Models library
- Simulink interface
- Interface to magnetics program

- Prone to errors in simulation results
- Simple output graphics utility
PSIM AC Model

- Multiple time-domain runs are used to obtain AC response

PLECS – The MATLAB Plug-In

- Power tool-kit for SIMULINK
- Allows the simulation of power stage as integrated part of MATLAB (SIMULINK) simulation without introducing extra delays
- Ideal for investigating digital control loops in power systems

- Only generic models
- Simulink interface for both schematic and graphics
PLECS Circuit as a Simulink Block

PLECS Circuit

PSPICE cycle-by-cycle model

- Uses physical level models of “real” devices
PSIM Flyback cycle-by-cycle model (Time Domain)

Demo
Real time: 3 ms

PSIM DCM cycle-by-cycle simulation results

- Textbook waveforms

R_{load}=220\Omega
PSPICE vs. PSIM Flyback

cycle-by-cycle simulation results

![Graph showing primary, secondary current, and output voltage waveforms for PSPICE and PSIM simulations.](image)
Small Signal (AC) Analysis
(Needed for Control Design)

Two Alternatives:

1. Full switched circuit:
   Injection of a sinusoidal perturbations
   PSPICE → manually
   PSIM → automatic

2. Average Model
   PSPICE → AC analysis
   (linearization by simulator)
   PSIM → automatic transient injection

Small signal response by injection of sinusoidal perturbations (time domain)

- Transient simulation – any simulator
PSIM Realization (Buck)

Power-Stage small signal transfer function
By injection of sinusoidal perturbation - PSIM & PSPICE
The Behavioral Approach
Average Model of Flyback - PSPICE

- Average models can be applied to obtain frequency response – AC analysis (to be discussed later)

Signal injection versus Average model

- Signal injection
  - Applies the switching schematics as is
  - Takes a long time to run
  - Noisy at high frequency
- Average model
  - Runs very fast
  - Need to built a behavioral equivalent
  - Some topologies/controllers are not easy to convert to average circuits
PSIM vs. PSPICE AC Comparison

\[ V_{out} \]

Behavioral average modeling of switch mode systems

Applications:
- DC transfer functions
- Transient (large signal, time domain) phenomena
- Small signal (AC, time domain) transfer functions

Not applicable to:
- Switching details, rise and fall times, spikes
- Device characteristics and losses
- Subharmonic oscillations

- Conduction losses can be accounted for
- HF ripple can be estimated
7. Average Models
The Switched Inductor Model (SIM) Strategy

- Identify the switched assembly
- Replace the switching part by a continuous behavioral (analog) equivalent circuit
- Leave the analog part as-is
- Run the combined circuit on a general purpose simulator

The modeling methodology presented in this seminar is highly ‘portable’, independent of simulator

Demonstration by PSPICE Ver. 10.5 (Demo Edition)

The switched inductor model

- The problematic part: Switched Assembly
- Rest of the circuit continuous - SPICE compatible
- The objective: translate the Switched Assembly into an equivalent circuit which is SPICE compatible
Average Simulation of PWM Converters

Buck

Boost

Buck - Boost

Possible switch modes

$T_{ON}$ - switch conduction time
$T_{OFF}$ - diode conduction time
$T_{DCM}$ - no current time (in DCM)
The Switched Inductor Model (SIM) (CCM)

The concept of average signals

Objective: To replace the switched part by a continuous network
**Average current**

\[ I_a = I_c = I_L \]

Similarly:

\[ I_c = I_L \frac{T_{OFF}}{T_S} = I_L D_{off} \]

**Toward a continuous model**

\[ I_a = I_L \]

\[ I_b = I_L \cdot D_{on} \]

\[ I_c = I_L \cdot D_{off} \]

\[ G_a, G_b, G_c \cdot \text{current dependent sources} \]

\[ G_a = I_L \]

\[ G_b = I_L \cdot D_{on} \]

\[ G_c = I_L \cdot D_{off} \]
**I_L derivation**

\[ \frac{dI_L}{dt} = \frac{V}{L} \Rightarrow \frac{d\langle I_L \rangle}{dt} = \frac{V}{L} \]

\[ \langle X \rangle = \bar{X} = \text{Average value} \]

**Average inductor voltage**

\[ \bar{V_L} = \frac{V(a,b) \cdot T_{on} + V(a,c) \cdot T_{off}}{T_S} = V(a,b) \cdot D_{on} + V(a,c) \cdot D_{off} \]
The Generalized Switched Inductor Model (GSIM) Model

\[ G_a = I(L) \]
\[ G_b = I(L) \cdot D_{on} \]
\[ G_c = I(L) \cdot D_{off} \]
\[ V_L = V(a,b) \cdot D_{on} + V(a,c) \cdot D_{off} \]

Topology independent!

Example: Implementation in Buck Topology

1. The formal approach

\[ G_a = I(L) \]
\[ G_b = I(L) \cdot D_{on} \]
\[ G_c = I(L) \cdot D_{off} \]
\[ E_L = [V_0 - V_{in}] \cdot D_{on} + [V_0 - 0] \cdot D_{off} \]
**Implementation in Buck Topology**

2. The intuitive approach - by inspection

\[ E_{in} = V_{in} \cdot D_{on} \]
\[ G_b = I_L \cdot D_{on} \]
\[ E_{in} + V_o \rightarrow V_L \]

Polarity: (voltage and current sources) selected by inspection

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**Boost**

- Emulate average voltage on inductor
- Create \( I_L \) dependent current sources
Making the model SPICE compatible

$I_L$ and $D_{ON}$ are time dependent variables \{\(I_L(t), D_{ON}(t)\)\}

$D_{ON}$ is not an electrical variable

---

In SPICE environment

\[ V(D_{on}) \times I(L_I) \]

Name of node: "$D_{on}$"

$D_{on}$ is coded into voltage
Running SPICE simulation

DC (steady state points) - as is

TRAN (time domain) - as is

AC (small signal) - as is

- Linearization is carried out by simulator!

Discontinuous Model (DCM)

\[ T_{off} = T_s - T_{on} \]

\[ D'_{off} = \frac{T_s - T_N}{T_s} = 1 - D_{on} \]

\( D'_{off} \neq 1 - D_{on} \)
The combined DCM / CCM model

\[ G_a = I_L \frac{D_{on}}{D_{on} + D_{off}} \]
\[ G_b = I_L \frac{D_{off}}{D_{on} + D_{off}} \]
\[ G_c = I_L \frac{D_{off}}{D_{on} + D_{off}} \]
\[ V_L = V(a,b)D_{on} + V(a,c)D_{off} \]
\[ D_{off} = \min \left(1 - D_{on}, \left( \frac{2I_L f_s}{V(a,b)D_{on} - D_{on}} \right) \right) \]

Synchronous Power Stages (diode replaced by switch)

- Only two stated for switched inductor: open and closed
- No third state as in DCM
- Use CCM model
Example: Buck Converter

File: Buck_cy_by_cy.OPJ

Cycle by Cycle simulation of PWM Buck converter

PARAMETERS:
- VIN = 10V
- LOAD = 75W
- COUT = 220uF
- RLOAD = 15Ω

PARAMETERS:
- RESR = 0.5Ω
- RLOAD = 0.1Ω

PARAMETERS:
- FS = 100%
- TS = 1.1%
Power Start-Up at Constant $D_{on}$

Zooming up
Average model

File: Buck.OPJ

Average simulation by SIM-Model of PWM Buck converter

- $D_{on}$ coded into voltage
- $D_{off}$ for CCM/DCM
Inductor

$V(Don) \times V(a,b) + V(Doff) \times V(a,c)$

Input side

$V(Don) \times I(Lout)/(V(Don)+V(Doff))$

$V(Doff) \times I(Lout)/(V(Don)+V(Doff))$
Output side

DC Sweep plus Parametric (on Rload)
Sweeping $R_{load}$ Constant $D_{on}$

Diode losses

DCM

CCM

Transient Analysis – Power Turn-On

Simulation Settings - trans

Analysis type: Time Domain (Transient)

Options:
- General Settings
- Automated Script
- Monte Carlo/Worst Case
- Parametric Sweep
- Temperature Sweep
- Steady-State Point
- Load Bias Point

Run to time: 500 seconds (TSTOP)

Start saving data after: 0 seconds

Transient options:
- Maximum step size: 10u seconds
- Skip the initial transient bias point calculation (SKIPBP)

Output File Options: OK Cancel Apply Help
Power Start-Up at Constant $D_{on}$

Comparing Cycle-by-Cycle to Average Simulation
AC Analysis
The Real Strength of Average Simulation

Linearization
• The circuit is linearized by simulator (elements, devices and expressions)

• Numerical linearization!
e.g. a source \( f(x,y,z) \) is replaced by:

\[
\begin{align*}
\frac{f(X + \Delta X, Y, Z) - f(X, Y, Z)}{\Delta X} & x \\
+ \frac{f(X, Y + \Delta Y, Z) - f(X, Y, Z)}{\Delta Y} & y \\
+ \frac{f(X, Y, Z + \Delta Z) - f(X, Y, Z)}{\Delta Z} & z
\end{align*}
\]

• Transparent to user
PSpice simulations examples

Buck Average

Buck Cy by Cy

Boost
Boost Simulation

SIM-Model under CCM & DCM for PWM Boost converter

![Diagram of Boost Converter]

Parameter: ESR of C_out
- 100mΩ
- 10mΩ
- 1mΩ

Frequency Response

\[ R_{\text{Load}} = 10\, \Omega \]
$R_{\text{Load}} = 1000\text{Ohm}$

**PSpice simulation example**

Boost simulation
Modulators – The Duty Cycle Generators

- General representation of a switch mode DC-DC converter

PWM MODULATOR - Voltage Mode

\[
\frac{D}{V_e} = K_M \text{ (voltage mode)} = \frac{V_E - V_M}{V_P - V_M}
\]

\[
\frac{d}{V_e} = \frac{V_e}{V_P \cdot V_M}
\]
Coding

\[ K_M \text{ (voltage mode)} = \frac{V_E - V_M}{V_P - V_M} \]

D coded into voltage

\[ 0 \leq V_D \leq 1 \]

Duty Cycle Limiter

- Behavioral dependent source ETABLE

\[ \text{TABLE} = (0.1, 0.0, 1) (0.9, 0.0, 0.9) \]
Average Current Mode

- $V_E$ is a function of $V_o$ and $I_L$
- ‘Control’ is the original analog circuit
- Same modulator as in voltage mode

Peak Current Mode Control

$L=195 \mu\text{m}$

$28\text{v}$

$R_s = 25\text{m}\Omega$

$R_1 = 47.5\Omega$

$R_2 = 2.5k\Omega$

$R_o = 11.2\Omega$

$C = 2000\mu\text{F}$

$C_f = 0.23\mu\text{F}$

$R_f = 72.2k\Omega$

$V_p = 0.25\text{v}$

$3.25$

$FF$
Current Mode CCM

\[ E_{Don} = \frac{V(V_e) - KS \frac{I(L)}{V(\text{Don}) + V(\text{Doff})}}{TS \left( MC + KS \frac{V(a,b)}{2L} \right)} \]

- \( V(V) \)
- \( KS = \text{Current Loop Gain} \)
- \( MC = \text{Slope Compensation} \)
- \( TS = \text{Switching Period} \)
- \( L = \text{Inductance of main inductor} \)
- \( |I(L)| = \text{Average inductor current} \)

If your can write an expression, it can be modeled!
Inductor

\[ v^{(sw)} + v^{(don)} + v^{(c)} + v^{(out)} + v^{(off)} + v^{(in)} \cdot (1 - v^{(don)} - v^{(off)}) \]

Duty Cycle Generator

\[ \min(\text{abs}(2^{(w)} \cdot v^{(in)} / (ts \cdot v^{(don)} \cdot (v^{(in)} - v^{(sw)}))), 1 - v^{(don)}) \]

\[ f_s \cdot (v^{(error)} - k_s \cdot v^{(c)}) / (mc + k_s \cdot (v^{(in)} - v^{(sw)}) / (2\cdot v^{(lin)})) \]
V(out)/V(Don) as normal
V(out)/V(Verror) lower order

PSpice simulation example
CM-Boost
Models of IC Controllers

- Vendors do not supply simulation models of IC controllers
- Large signal controllers' models are supplied with some simulators (e.g. PSIM)
- Average models (applicable for small signal analysis) are available from AEi
- It is easy to build your own behavioral average models (for control)

The Power Stage small-signal response

- A prerequisite for control design
- Can be obtained by analytical derivations/expressions
- By Simulation
  - On switched model (cycle by Cycle)
  - Average models
Feedback Loop Design of PWM Converters

1. Find $A(f)$ of Power stage
2. Decide on $f_0$
3. Choose type of compensating network
4. Calculate feedback network

Make $|\beta A|$ as large as possible

The Relationship to PID

$$H(s) = \frac{v_{\text{comp}}}{v_e} = K_p + \frac{K_I}{s} + s \cdot K_d =$$

$$= \frac{K_d \cdot s^2 + K_p \cdot s + K_I}{s} = \frac{K_d (s + \omega_{z1}) \cdot (s + \omega_{z2})}{K_I}$$

$$\omega_{z1,2} = \frac{-K_p \pm \sqrt{(K_p)^2 - 4K_dK_I}}{2K_d}$$
The Relationship to PID

\[ \frac{V_{\text{comp}}}{V_e} = \frac{K_d \cdot s^2 + K_p \cdot s + K_l}{s} = \frac{K_d (s + \omega_{z1}) \cdot (s + \omega_{z2})}{K_l s} \]

\begin{align*}
\text{B} & \quad \text{Log}(f) \\
& \quad f_1 \quad f_2 \\
\end{align*}

\[ \frac{V_{\text{comp}}}{V_e} = \frac{1}{B} \]

\begin{align*}
& \quad \text{Log}(f) \\
& \quad f_1 \quad f_2 \\
\end{align*}
The Relationship to PID

BW Limitations (of LG, crossing of A and B)

- PWM is a sampled data system.
- Nyquist sampling theorem applies.
- Cross over frequency $f_c$ (A, B, LG) < $f_s/2$
- In practice $f_c < 10 f_s/2$
8. Analog compensator networks

Possible phase compensation schemes
Lag (A)

\[ A_o = \frac{R_f}{R_{in}} \]

\[ f_p = \frac{1}{2\pi C_f R_f} \]

one pole

f

A_o
**Lag (B)**

\[ A_0 = A_{OL} \text{(ampl.)} \]

\[ f_L = \frac{1}{2\pi C_f R_f} \]

\[ A_2 = \frac{R_f}{R_{in}} \]
Lag-Lead (B)

Double zero compensation scheme

Useful region, phase advance
Double Zero (B)

Double Zero- Alternative
Application of Double Zero Compensator

Rate of closure
20 db/dec

Phase advance by compensator

Voltage Mode Control
Compensator Design Example

VM Regulator
Obtaining the Loop Gain by Simulation

\[ \text{LG} = \frac{S_f}{S_E} \]

Loop Gain by Simulation

\[ \text{LG} = \frac{S'_f}{S'_E} \]
**Loop Gain by Simulation**

\[ LG = \frac{S'_f}{S'_\varepsilon} \]

**Loop-Gain**

Getting Loop-Gain under closed loop response \{A(f)B(f)\}

\[ V_{\text{in}} = 0 \]

\[ LG(f) = \frac{V_1}{V_2} \]
Rules for Getting Loop-Gain by Simulation

The relevant analysis is .AC

• Locate the AC source at the output of a low impedance device (could be real or behavioral)

• Set the AC value to any value (1 V is fine)

• Make sure that there are no other AC sources in the system

• Check bias point (.OUT file)

• Remember that the classical stability criteria take into account the phase reversal (180°)

PSpice Simulation

VM Regulator
PSIM Demonstration

Large signal

Schematic

Probe

Small signal

Schematic

LoopGain

Probe

TF

Probe

Peak and Average Current Mode

Two step design: inner loop and outer loop
The advantages of current feedback (PCM or ACM)

Typical power stage VM

Same power stage (outer loop) with CM

- With closed inner-loop

Inner Loop design
Average Current Mode

$V_{in}$

$V_{in}$

$L$

$1mH$

$V_{E,OUT}$

$V_{E}$

$K_{M}$

$V_{C}$

Vac = 1V; Vc = Constant (operating point); KS = 1/20

$V_{O}$

$R_{O}$

$470 \mu F$

$160\Omega$
The response for inner loop design

\[ I(L_1)/V(V_e) \]

\[ 1/\beta \]

F = 13kHz; Gain = -13.3db = 0.22
The error amplifier (For KS = 1/20)
Closed inner Loop

Vac = 1V ; Vc = Constant (operating point) ; KS = 1/20
**Loop Gain**

Phase margin 60°

**Nyquist Plot**

- Imaginary(LG) versus Real(LG)
Nichols Plot

- $|LG|$ versus Phase(LG)

Closed Inner Loop (Tracing)

$\frac{I(Li)}{V(Vc)}$
Closed Inner Loop

- Toward Power factor Correction (open loop)

Transient Simulation - CCM

In CCM: Don+Doff = 1
Transient Simulation - CCM/DCM

After changing $L_m$ to 300$\mu$H

Three Loops Feedback PFC System (Conventional CCM)
UC3854 Based Average Model

CCM - Based on UC3854
Voltage Control Loop

Output Section

Excitation

Error Amplifier and Compensation Network

Input Voltage Step Response:
115Vrms to 230Vrms

Pout=250W, Slew Rate=160V/mS
**Input Voltage Step Response:**
115Vrms to 230Vrms

- Input Voltage
- Output Voltage

Pout=250W, Slew Rate=160V/mS

---

**Current Loop Gain at Different Input Voltages**

Vin=50V, 100V, 200V, 300V
Loop Gain of Voltage Control Loop

PSpice simulation

PFC-AC

PFC-TRAN
CCM Control Concept with no Sensing of Input Voltage

Average Model
Input Behavior at Different Line Voltages

Pout=1kW, Vin=80Vrms, 230Vrms, 265Vrms

Loop Gain of Current Control Loop

$\Phi_m = 90^\circ$
Current Loop Transfer Function

\[
\frac{i_L}{v_{in}} = \text{const}
\]

Frequency

PSpice simulation

PFC_no_sens-AC  PFC_no_sens-TRAN
Conventional Border Line Control Method

MC33261 Based Average Model
MC33261 Based Average Model

PSpice simulation

PFC_bord-AC  PFC_bord-TRAN
**Border Line Control Concept with no Sensing of Input Voltage**

![Diagram](image1)

**Principle of Operation**

\[
I_{pk}(t) = 2I_{av}(t) = \frac{V_{in}}{L} T_{on} \\
I_{av}(t) = \text{const. if } T_{on} = \text{const.}
\]
MC33260 Based Average Model

\[ E_{on} = f(\text{control}) \]

\[ E_{off} = f(\text{inductor discharge time}) \]

\[ D_{on} = \frac{T_{on}}{T_{on} + T_{off}} \]

\[ D_{off} = \frac{T_{off}}{T_{on} + T_{off}} \]
Combined Stage (Boost-Flyback)

Principle of Operation

- $C_B$ serves as output capacitor for Boost Section and as input voltage source for Flyback section.
Behavior at Different Power Levels

- Output Voltage
- Inductor Current

Vin=230V, Pout=100W, 50W

Combined Stage (SEPIC with Transformer)
Behavior at Different Power Levels

Vin=230V, Pout=70W, 50W

PSpice simulation

PFC_DCM - avg
PFC_DCM - CBC
9. Digital Control

Control of PWM converters
Voltage Mode

• Voltage regulator
Control of PWM converters
Current mode

- Additional feedback loop
- Reduces system order
- Faster response
- Simple controller
- Cycle-by-cycle protection (PCM)

Analog vs. Digital

**Analog**

**Advantages**
- Efficient and accurate
- Wider Bandwidth than Digital
- Higher Resolution
- Easier Design
- Lower cost

**Disadvantages**
- Degradation Due to Component Aging
- Component Temperature Drift
- More Parts (Lower Reliability)
- Limited Upgrades
- Difficulty of Integrator Clamp and Preset
- Limited in performing smart control algorithm
- Difficult to perform fine tuning and adaptations
**Analog vs. Digital**

**Digital**

**Advantages**
- Flexible
- Well-defined Behavior
- No Drift in Digital Part
- Software Upgrade Path
- Less Parts (Higher Reliability)
- Easy Clamp and Preset
- Communication
- Advanced Control (non-linear)
- On-the-fly adaptation capability

**Disadvantages**
- Higher cost
- Limited Bandwidth \( f_{BW} \leq f_s/10 \) to \( f_s/6 \)
- Complex programming
- New technology still not widely accepted

**Design challenges of digital control**

**Current mode**

**Peak Current Mode**
- Very high sampling rate – min. 10*fs
- Additional D/A to generate \( i_c \)

**Average Current Mode**
- Can be done on a single sample in cycle
- LPF can be implemented in software
- Delays
PWM converters as feedback systems

Analog

- Power stage
- Feedback

\[ \frac{V_o}{V_d}(f) \] Power stage
\[ \frac{V_e}{V_o}(f) \] Compensator
\[ \frac{d}{V_e}(f) \] Modulator

* Linear control theory based design → small signal response

Traditional Analog PID Compensators

Voltage Mode Control

- Plant
- Compensator
- Loop-gain

\[ A(s) = \frac{k_p \left( \frac{s}{\omega_p} + 1 \right)}{s^2 + \frac{\omega_p}{\omega_n} s + \frac{\omega_p Q_p}{\omega_n}} + 1 \]

\[ B(s) = \frac{\left( \frac{s}{\omega_c} + 1 \right) \left( \frac{s}{\omega_c^2} + 1 \right)}{s^2 + \frac{\omega_c}{\omega_c^2} s + \frac{\omega_c^3}{\omega_c^2} + 1} \]

* The converter is modeled as a second order system
* High cross over frequency for fast response
Digital/discrete control

\[ \text{LG} = K_t K_M K_{A/D} e^{-s\Delta T} P(s) B(z) e^{-s\Delta T} \equiv \frac{1}{z} \]

- Sampling and computation delay
- Additional gain – \( K_{A/D} \)

Sampling Issues

ZOH

[Diagram showing ZOH with time axis and \( \Delta T \) notation]
Prof. S. Ben-Yaakov, Control Design of PWM Converters

**ZOH**

\[ f_s = 10\text{KHz} \]

**Sampling Delays**

\[ T_s = \frac{1}{f_s} \]

Sample (n) → A/D computation → PWM (n+1) → Sample (n+1) → Sample (n+2) (result of sample (n))
Slow Sampling Rate

\[ T_s = \frac{1}{f_s} \]

**Sampling rate**

\[ \frac{f_s}{2} \]

Compensation network, continuous

\[ K = \frac{R_1}{R_2} \]

\[ \tau = R_1 C \]

\[ V_e(t) = C \frac{dV_c(t)}{dt} + \frac{V_c(t)}{R_1} \]

Differential equation:

\[ -K V_e(t) = \tau \frac{dV_c(t)}{dt} + V_c(t) \]

Integral equation:

\[ -K \int V_e(t) dt = \tau \int \frac{dV_c(t)}{dt} + \int V_c(t) dt \]

Laplace transform:

\[ \frac{K}{s} V_e(s) = \tau V_c(s) + \frac{1}{s} V_c(s) \]

Transfer function:

\[ \frac{V_c(s)}{V_e(s)} = \frac{K}{s \tau + 1} \]
Discretization rules

Differential equations transforms to difference equations
\[
\frac{dV(t)}{dt} \Rightarrow \frac{V[n] - V[n-1]}{\Delta T}
\]

Integral equations transforms to summations
\[
\int V(t) dt \Rightarrow \Delta T \sum_{k=-\infty}^{n-1} V[k]
\]

Z-transform is the discrete time dual of the Laplace transform
\[
V(s) = \int_{-\infty}^{\infty} V(t) e^{-st} dt \Leftrightarrow V(z) = \sum_{k=-\infty}^{\infty} V[k] z^{-k}
\]

Transfer functions are represented in Z

Unstable if \( a > 1 \)
The intuitive meaning of the $z$ operator
$s \Rightarrow$ derivative operator; $z \Rightarrow$ Delay operator

$$\frac{v_o(z)}{v_{in}} = \frac{z}{z^2 - 1}$$

$$\frac{v_o(z)}{v_{in}} = \frac{z^{-1}}{1 - z^{-2}}$$

$$v_o(1 - z^{-2}) = v_{in} z^{-1}$$

$$v_o = v_o z^{-2} + v_{in} z^{-1}$$

$$v_o = v_o (n - 2) + v_{in} (n - 1)$$

Continuous to discrete transformation

- Pole-Zero matching
- Zero Order Hold (ZOH)
- Trapezoid (bilinear) transformation
Pole-Zero matching

- Map discrete poles/zeros by $z_i = e^{s_i \Delta T}$
- For complex s-domain roots $s_i = a_i + jb_i \rightarrow z_i = e^{a_i \Delta T} e^{jb_i \Delta T}$
- Maintain same DC gain $G(s)|_{s=0} = G(z)|_{z=1}$

$$\frac{V_c(s)}{V_e(s)} = \frac{K}{s \tau + 1} \rightarrow \frac{V_c(z)}{V_e(z)} = \frac{KP}{z - e^{-\Delta T/\tau}}$$

$V_c(s)|_{s=0} = V_c(z)|_{z=1} \rightarrow P = 1 - e^{-\Delta T/\tau}$

$$\frac{V_c(z)}{V_e(z)} = \frac{K(1 - e^{-\Delta T/\tau})}{z - e^{-\Delta T/\tau}} = \frac{m}{z - n} \quad m, n - constants$$

Zero Order Hold (ZOH)

Hold equivalent = sampled area

$s \leftrightarrow \frac{z - 1}{\Delta T}$

Transfer function:

$$\frac{V_c(z)}{V_e(z)} = \frac{K \Delta T}{\Delta T + \tau} \left( \frac{1}{Z - \frac{\tau}{\Delta T + \tau}} \right) = \frac{m}{z - n}$$

$V_c[n] \rightarrow Z^{-1} \rightarrow V_e[n]$
**Trapezoid (bilinear) transformation**

**Hold equivalent = sampled area**

\[
\frac{V_C(s)}{V_e(s)} = \frac{K}{s \tau + 1} \quad \text{s} \leftrightarrow \frac{2}{\Delta T} \frac{z - 1}{z + 1}
\]

**Transfer function:**

\[
\frac{V_C(z)}{V_e(z)} = \frac{2\tau \frac{z - 1}{\Delta T} + 1}{\Delta T \frac{z - 1}{\Delta T}}
\]

\[
\frac{V_C(z)}{V_e(z)} = \frac{K \Delta T/2 \left( z + 1 \right)}{\tau + \Delta T/2 \left( z - 1 \right)}
\]

**Comparison of hold types**

Bode Diagram

\[
\frac{V_C(s)}{V_e(s)} = \frac{10}{0.1s + 1}
\]

fs=50KHz
Effects of sampling rate

Hold Type: ZOH
Discretization:
Inherent Phase-lag

A/D and PWM Resolution
The Limit Cycle Problem

Oscillatory output [mV/bit]
Stable output
**No Limit cycle rules**

One bit of the DPWM should change $V_o$ by less than 1 bit of the A/D

Taking into account the system gains

$$K_{PS}K_{I}q_{DPWM} < q_{A/D}$$

Compensator must include integral action (included in PID)

System must satisfy Nyquist criterion

$$1 + A(s)B(s) > 0$$

Stability

$$1 + A(s)B(s) \neq 0$$

Oscillations

---

**Digital Compensator Design Methods**

- Frequency domain based
- Pole location in z plane
- Time domain design
Frequency domain design

1. Design a frequency domain controller (Bode, Nichols, etc.)
2. Refinement: take into account the sampling and computational delays
3. Translate the analog controller into a Z equivalent
4. Simulate by numerical simulator (e.g. MATLAB)

Frequency domain design

References


Z Plane Design
Using the MATLAB SISO tool

1. Define the system structure
2. Define the Plant response
3. Define the compensator template
4. Select the analysis view (Root Locus, Bode, Nichols)
5. Insert design constraints (gain, BW, PM, settling time, Natural frequency, etc.)
6. You can use the GUI to change pole/zero locations (either in S or Z and observe the resulting closed loop response)

• Trial and error procedure

MATLAB SISO tool
References


Time domain Discrete Controller Design

- Digital compensator operates in the sampled-data domain
- Direct controller design - does not involve errors related to approximations (s to z)
- When working in the time domain, system attributes such as bandwidth and phase margin seem artificial
- Relevant parameters are: rise time, overshoot etc.
- Improved performance of the closed loop system compared to other discrete design approaches
- Does not involve trial and error procedure

References

Time domain Discrete Controller Design

- Plant transfer function (continuous): $A(s)$
- $S$ to $Z$ transformation: $A(s) \rightarrow A(z)$
- Defining the desired closed loop response: $A_{CL}(s)$
- $S$ to $Z$ transformation: $A_{CL}(s) \rightarrow A_{CL}(z)$
- Ideal controller:

$$A_{CL}(z) = \frac{A(z)B(z)}{1 + A(z)B(z)} \quad \rightarrow \quad B(z) = \frac{A_{CL}(z)}{1 - A_{CL}(z)} \frac{1}{A(z)}$$

Closed-loop response

$45^\circ < \phi_m < 90^\circ$

$2^{nd}$ order system

$$\frac{1}{s^2 + \frac{s}{\omega_n Q} + 1}$$

Design constraint:
System will have the characteristic equation
Describing the closed-loop response by time domain characteristics

Assuming 2nd order system

\[ \frac{V_o(s)}{d(s)} = \frac{1}{s^2 + \frac{s}{\omega_n} + \frac{1}{\omega_n Q}} \]

Rise time: \( t_r \approx \frac{1.8}{\omega_n} \Rightarrow \omega_n \approx \frac{1.8}{t_r} \)

Overshoot

\[ M_p = e^{-\frac{\pi}{2Q}} \sqrt{1 - \frac{1}{4Q^2}} \Rightarrow Q = \frac{\sqrt{1 + \left( \frac{\ln(M_p)}{\pi} \right)^2}}{2 \ln(M_p)} \]

Describing the desired \( A_{CL} \) in Z

- Second order characteristic equation sets the \( A_{CL}(z) \) denominator \( (a_0, a_1, a_2) \)

\[ s^2 + \frac{s}{\omega_n Q} + \frac{1}{\omega_n Q} \]

\[ z \rightarrow b_0 z^2 + b_1 z + b_2 \]

\[ a_0 z^2 + a_1 z + a_2 \]

- To derive the complete \( A_{CL} \) equation (i.e. numerator) additional constraints are to be satisfied:

  - Stability at infinity (bounded system) \( A_{CL}(z)_{|z=\infty} = 0 \)

  - Steady state error to step \( A_{CL}(z)_{|z=1} = 1 \)

  - Response to ramp (velocity constant) \( \frac{dA_{CL}(z)}{dz} \bigg|_{z=1} = \frac{1}{K_V} \)
Template-oriented controller

- Ideal controller to satisfy the design constraints
  \[ B(z)_{\text{Ideal}} = \frac{A_{\text{CL}}(z)}{1 - A_{\text{CL}}(z)A(z)} \]

This design method suffers from:
- controller implementation on digital platform vary by design (plant, \(A_{\text{CL}}\), etc.)
- High order - too many parameters – long computation time

Template-based controller

- In each computational event, only data points around the sampling instant are considered
- The controller uses only information that is in the vicinity of the sampling instant and is blind to all other information
- The implemented finite difference equation can be based on a short-term time response of the system rather than on the full response
A look at the step response of $B(z)_{\text{ideal}}$

Objective:
- Find a compensator template that will match (or will be close to) the ideal response – at least at the first few samples
- The compensator should have fewer computation cycles

The answer - PID controller

**PID template: continuous**

$$
\frac{V_c(s)}{V_e(s)} = \frac{s^2 + \frac{s}{\omega_c} + 1}{\omega_c^2 + \omega_c Q + 1}
$$

**PID template: discrete p-z matching**

$$
\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{z^{-1} - z^{-2}}
$$

Taking into account the sampling delay (A/D)

$$
\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}}
$$
**PID controller**

Difference Equation (will be implemented on the digital platform)

\[ V_c[n] = V_c[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2] \]

Only 3 samples!!!
Only 4 computations!!!

---

**Extracting PID coefficients (a, b, c)**

[Graph showing step response with ideal and PID curves]
**PID coefficients extraction procedure**

\[ V_c[n] = V_c[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2] \]

\[ \begin{align*}
  n &= 0 & V_c[0] &= V_c[-1] + aV_e[0] + bV_e[-1] + cV_e[-2] \\
  n &= 1 & V_c[1] &= V_c[0] + aV_e[1] + bV_e[0] + cV_e[-1] \\
\end{align*} \]

**Design example**

\[ V_o = 5V \quad \text{Switching frequency=sampling rate= 50KHz} \]

\[ \text{Tr}=100u \quad \text{MP}=10\% \]

\[ A_{CL}(z) = \frac{0.5044z + 0.4123}{z^2 - 1.403z + 0.4956} \]
Plant response

\[ PS(s) = \frac{3.333 \times 10^8}{s^2 + 2500s + 1.333 \times 10^6} \]

ZOH \[ PS(z) = \frac{0.06548z + 0.06459}{z^2 + 1.908z + 0.96} \]

Ideal controller response

\[ B(z) = \frac{0.5044z^3 - 1.375z^2 + 1.271z - 0.3958}{0.06548z^3 - 0.1249z^2 + 0.05945z} \]
Extracting PID coefficients (a, b, c)

\[ B(z) = \frac{3.4 - 6.15z^{-1} + 2.93z^{-2}}{1 - z^{-1}} \]

Closed loop response
Closed loop step response - results

- Reference is stepped from 5V to 6V

A look at the frequency domain

PM=40
BW=4KHz
Experimental

PM=33
BW=3.2KHz

Load step

PID coefficients
a=3.4
b=-6.15
c=2.93

V_{out}
**Slower Response**

Switching frequency = sampling rate = 50KHz

Vo = 5V  
Tr = 500u  
Mp = 0%  No over shoot

**Controller response**

![Step Response Graph](image)

Derived PID: \(B(z) = \frac{1.52 - 2.81z^{-1} + 1.38z^{-2}}{1 - z^{-1}}\)
Closed loop step response - results

- Reference is stepped from 5V to 6V
Experimental

PM=80
BW=1.5KHz
Load step

PID coefficients
a = 1.52
b = -2.81
c = 1.38

Comparison to analog design

The analog controller was set to have the same bandwidth as the digital design

Load step applied: 1A to 1.5A
Load step - analog (Spice simulation)

Load step - analog
Load step digital

PID compensation in voltage mode control

Transfer Functions

Plant

Area of interest

$|A(j\omega)|$

$|\frac{1}{B(j\omega)}|$

$\omega_{nr}$

$\omega_{cs}$

Frequency

-40dB/dec

-20dB/dec

Comp

Loop-gain

$|A(j\omega)B(j\omega)|$

$\omega_{nr}$

$\omega_{cs}$

Frequency

-40dB/dec

-20dB/dec

$A(s)B(s) = \frac{k}{\sigma} \left( \frac{s}{\omega_{cr}} + 1 \right)$

$k, \omega_{cr}, \alpha, \beta, \gamma, \sigma$

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**PID compensation in voltage mode control**

Closed-loop

\[ A_{CL}(j\omega) = \frac{s/\omega_{n} + 1}{s^2/\omega_{abv}\omega_{crs}/k + s/\omega_{abv} + 1} \]

Additional zero in the closed loop response

The known – second order relationships to the closed loop parameters no longer valid

**Comparison of second order template to the actual time domain response**

Simulation of step response for Same PM and BW

\[ A_{CL}(s) = \frac{s/\omega_2 + 1}{s^2/\omega_n + s/\omega_n Q + 1} \]

Actual response

Second order

Overshoot

Rise Time

Amplitude

Time (sec)
Relationship of time domain attributes to the system parameters

Assuming second order system - traditional

\[ A_{CL}(s) = \frac{1}{s^2 + \frac{s}{\omega_n} + 1} \]

Rise time: \( t_r \approx \frac{1.8}{\omega_n} \Rightarrow \omega_n \approx \frac{1.8}{t_r} \)

Overshoot \( M_p = e^Q \Rightarrow Q = \frac{\sqrt{\frac{\ln(M_p)}{\pi}}}{2} \)

Taking into account the closed loop zero

\[ A_{CL}(s) = \frac{s + 1}{\frac{s}{\omega_p} + \frac{s}{\omega_n} + 1} \]

\[ \omega_n = \omega_{pn} \sqrt{\frac{k_p \omega_{c1}}{\omega_{c2}}} \]

\[ Q = \frac{\sqrt{k_p \omega_{c1} \omega_{c2} \omega_{c3} \omega_{p} \omega_{n} \omega_{n} \omega_{n}}}{\omega_{c2}^2 \omega_{n}^2 + k_p \omega_{c1} \omega_{p} \omega_{n} \omega_{n}} = \frac{1}{Q_p} \]

Normalizing factors

Deviation of plant's double pole from bandwidth \( n = \frac{\omega_{pn}}{\omega_n} \)

Deviation of controller second zero from bandwidth \( m = \frac{\omega_p}{\omega_n} \)
Relationship of time domain attributes to the system parameters

Normalized Rise time:
\[ \theta_{n, t_r} = \frac{2Q}{\sqrt{4Q^2 - 1}} \left[ \frac{1}{\sqrt{1 - \frac{1}{4Q^2} - 1}} - \frac{2Q - 1}{\sqrt{4Q^2 - 1}} - \right] \]

Normalized Overshoot
\[ M_p = \left( 1 - \frac{1}{2Q} \frac{m}{m} \right) \exp \left( - \frac{1}{\sqrt{1 - \frac{1}{4Q^2} - 1}} \sqrt{4Q^2 - 1} \right) \]

Effect of low loop gain below the crossover frequency on the closed loop response

Separating the compensator contributions

\[ |A(j\omega)B(j\omega)|_{\text{lead}} \]

\[ |A(j\omega)B(j\omega)|_{\text{lag}} \]

\[ A_{C_{\text{lead}}}(s) \]

\[ A_{C_{\text{lag}}}(s) \]

\[ u(t) \]

\[ y_{\text{lead}}(t) \]

\[ y_{\text{lag}}(t) \]

Lead

Lag
Effect of low loop gain
Lag contribution

\[ A_{CL\_lag}(s) = \frac{s + 1}{\frac{s}{\omega_c^2} + \frac{k_p \omega_c \omega_c^2}{\omega_c^2 + k \omega_c^1}} \]

\[ y_{\text{unit\_step\_lag}}(t) = 1 - \frac{1}{1 + \frac{k_p \omega_c^1}{\omega_c^2}} e^{-\omega_c^2 t} \]

System Identification
System identification

\[
\frac{a_0 + a_1 z^{-1} + \ldots + a_{n-1} z^{-(n-1)}}{1 + b_1 z^{-1} + \ldots + b_n z^{-n}}
\]

\{a_0, a_1, \ldots, a_{n-1}, b_1, b_2, \ldots, b_n\} - ?

Proposed procedure main features
- Time domain based algorithm
- Memory efficient – utilizes short data sequences
- Generic template for all basic PWM topologies
**System identification Algorithm**

**Basic**

- Data records
- $\frac{N(z)}{D(z)}$
- $y$
- $e$
- $u$

Least squares

Carried out by MATLAB function `stmcb(n,d,it)`

**Iterative**

- Data records
- $\frac{1}{D_{r}(z)}$
- $\frac{1}{D_{s}(z)}$
- $0$
- $N(z)$
- $\hat{y}$

Least squares + Prefilter

---

**System identification Experimental implementation**

**Sampling instance selection to reduce switching noise**

- Gate command
- On/off

**Switching cycle**

- Time

**Averaging synchronous excited sequence – improve SNR**

- Output voltage

- Command
- Capture period
- Rest period

- Time
System identification
Results – Buck converter

\[ A(z) = \frac{-0.00644z + 0.0088}{z^2 - 1.987z + 0.98} \]

Identified Vs. Measured
Identified Vs. average model

System identification
Results – Boost converter

\[ A(z) = \frac{0.1414z - 0.047}{z^2 - 1.753z + 0.803} \]

Identified Vs. Measured
Identified Vs. average model
Controller design based on system identification

$A_{\text{Boost,ID}}(z) = \frac{0.2526z - 0.197}{z^2 - 1.866z + 0.8844}$

$T_r = 400\mu s$

$M_p = 10\%$

$B(z)_{\text{Boost,F}} = \frac{2.287 - 3.122z^{-1} + 1.03z^{-2}}{1 - z^{-1}}$
Thank you for Your Attention

10. Q&A
Sort Biography of Presenter

Prof. Shmuel (Sam) Ben-Yaakov

- BSc degree in Electrical Engineering from the Technion, Haifa Israel, in 1961
- MS and PhD degrees in Engineering from the UCLA, in 1967 and 1970 respectively.
- Full Professor at the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva, Israel,
- Heads the Power Electronics Group of BG University
- Published over 250 scientific and technical papers in leading journals and conferences
- Holds about 20 patents (as an inventor)
- Consultant to companies worldwide on design-oriented theoretical issues in the areas of analog and power electronics as well as on product development.
- Founder and CTO of Green Power Technologies Ltd. (http://www.g-p-t.com)
- Present research interests include: power electronics aspects of piezoelectric elements, analog and digital control, power factor correction, lighting electronics, soft switching and active thermal cooling.

Primary to secondary isolation

The problem:

![Diagram of primary to secondary isolation](image-url)
Alternative

A

\[ P_n \]

\[ V_o \]

feedback

isolation

B

D

\[ \text{Power stage} \]

\[ V_o \]

feedback

isolation

C

\[ \text{Power stage} \]

feedback

isolation

Gain

D

\[ \text{Power stage} \]

isolation

Gain + feedback

V_{ref}