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(54) **METHOD AND CONTROL CIRCUITRY FOR IMPROVED-PERFORMANCE SWITCH-MODE CONVERTERS**

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(57) **ABSTRACT**

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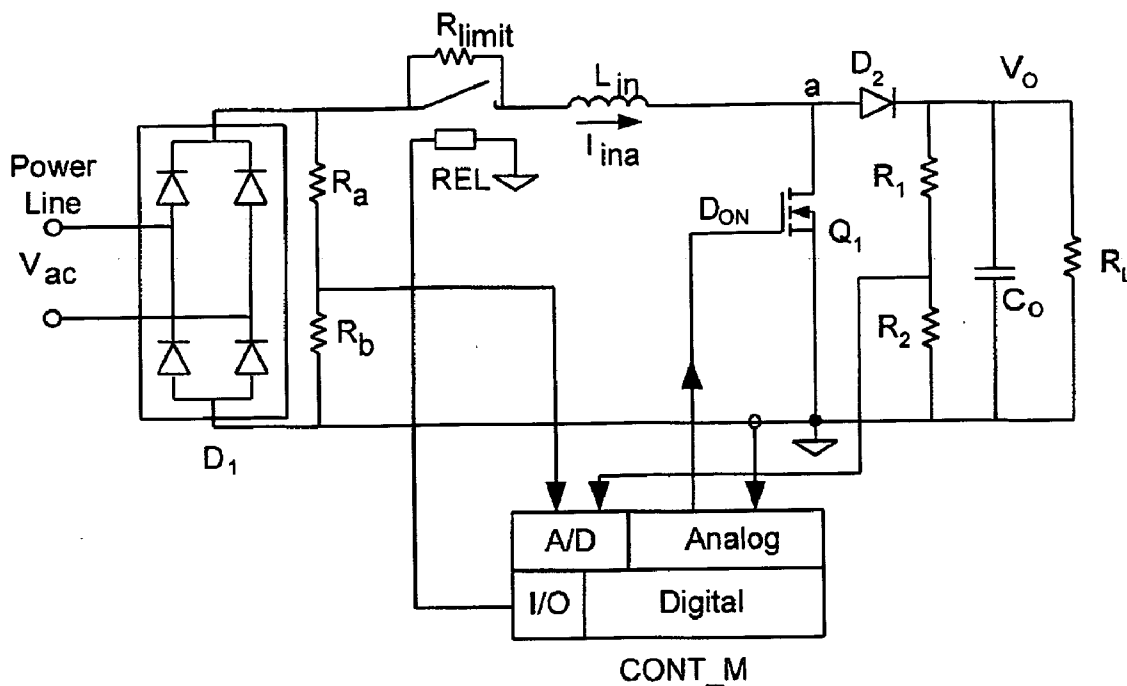
A system and method for supplying power to a load and for controlling the power factor presented to the power line. Output voltage is controlled by a digital, outer, control loop, and inner, analog, control loop causes the input current to be substantially proportional to the input voltage at any particular point in the power line cycle. Thus, the system presents a load to the power line that appears to be purely resistive. The use of an analog multiplier is not required, nor is sampling of input voltage. Limiting of inrush current provides for brown-out protection and soft-start.

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**Related U.S. Application Data**

(60) **Provisional application No. 60/592,377, filed on Aug. 2, 2004.**



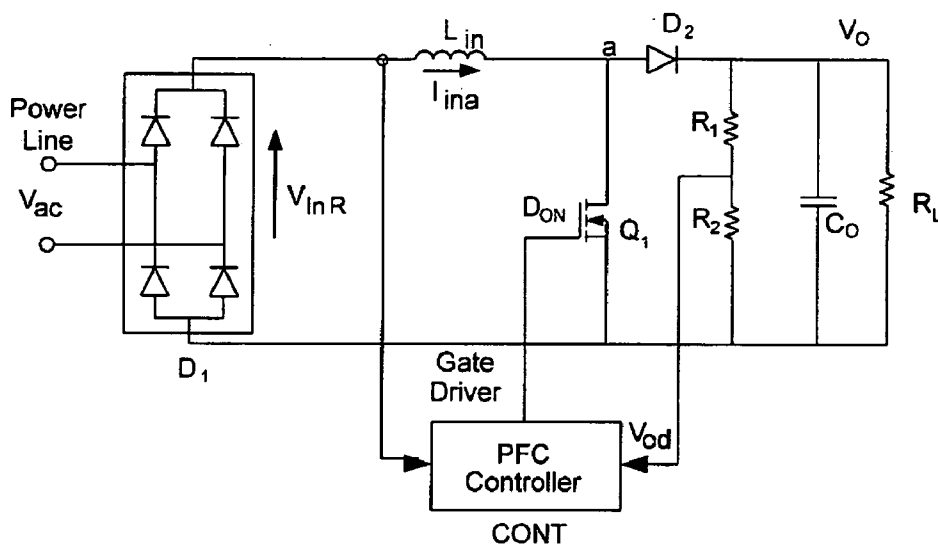


Fig.1 (Prior Art)

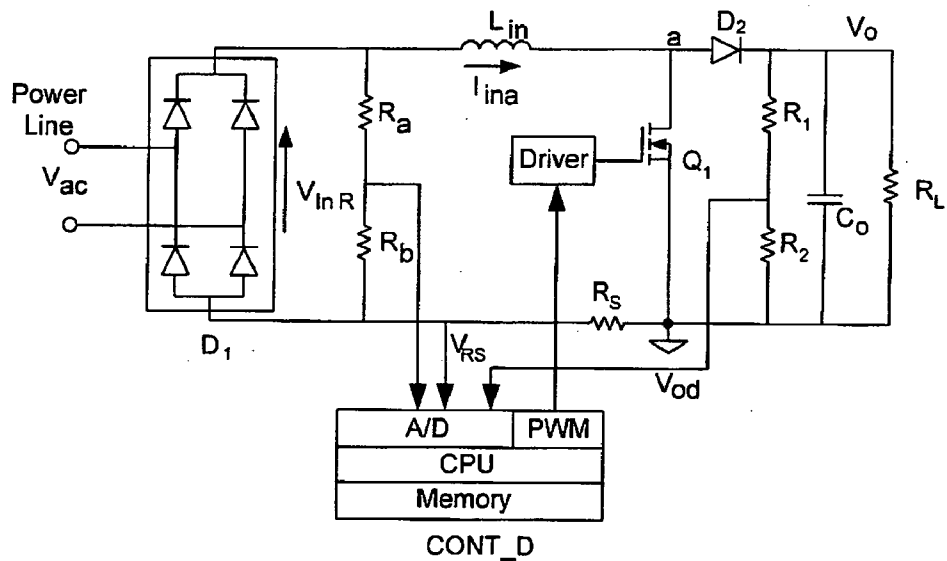


Fig. 2 (Prior Art)

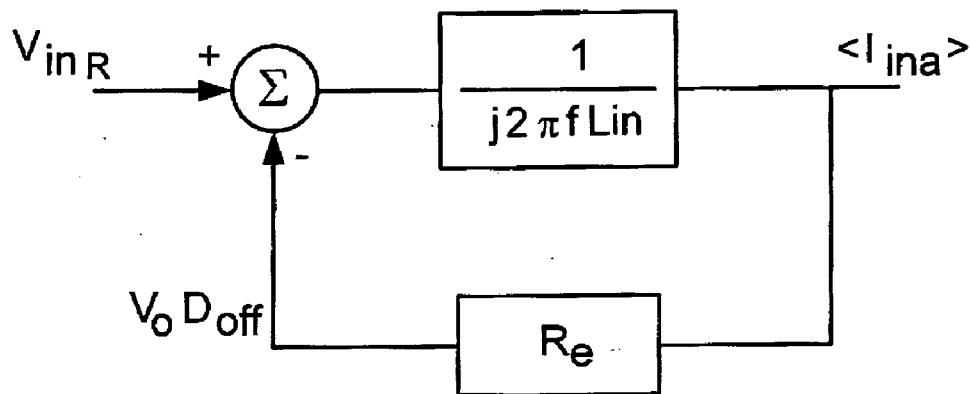


Fig.3 (Prior Art)

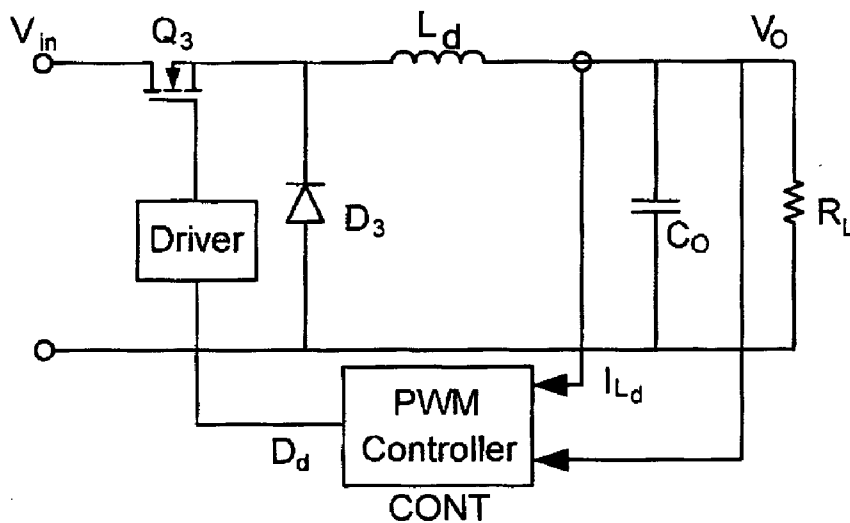


Fig. 4 (Prior Art)

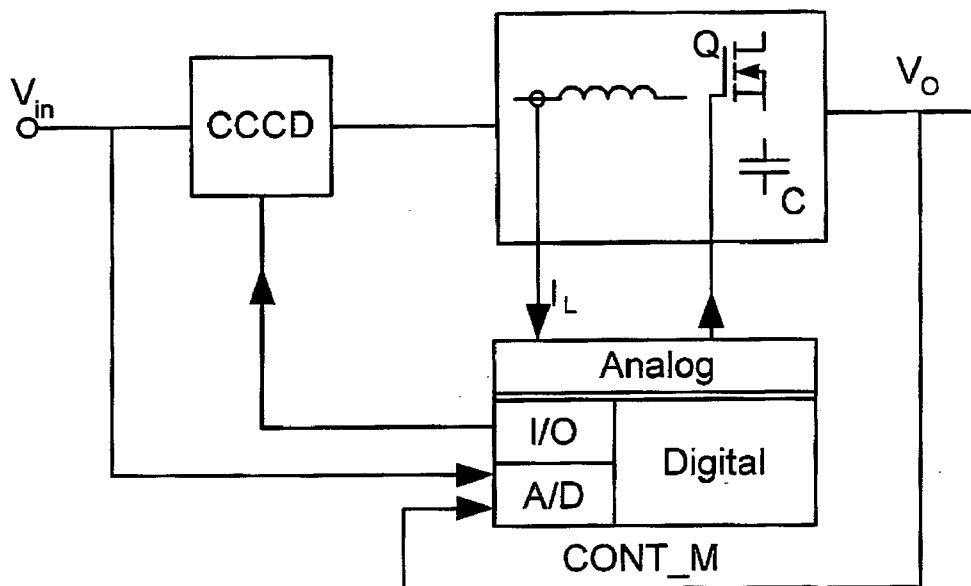


Fig. 5

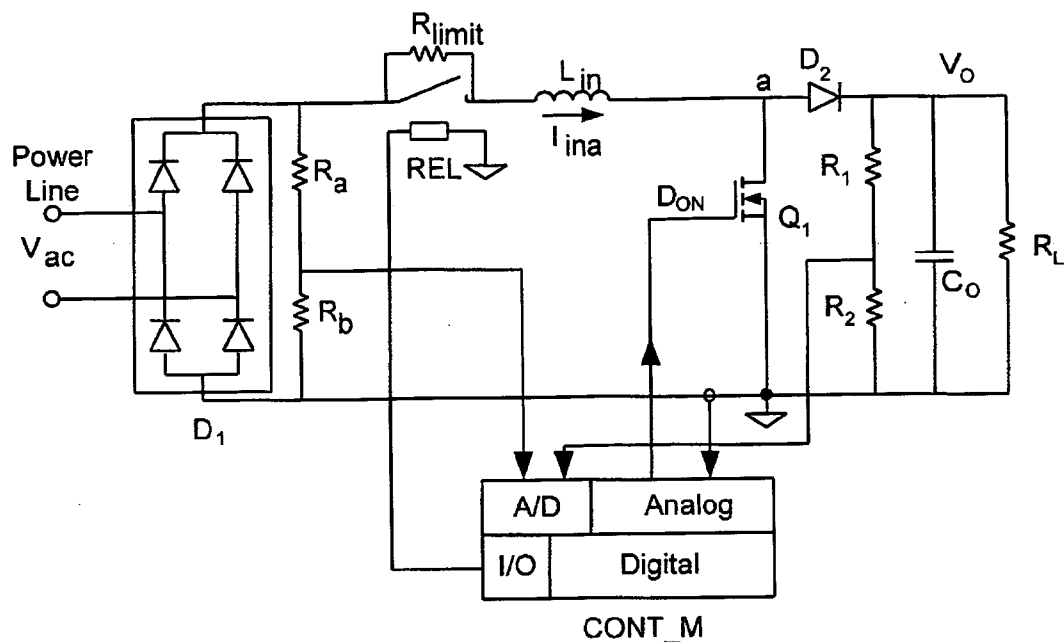


Fig. 6

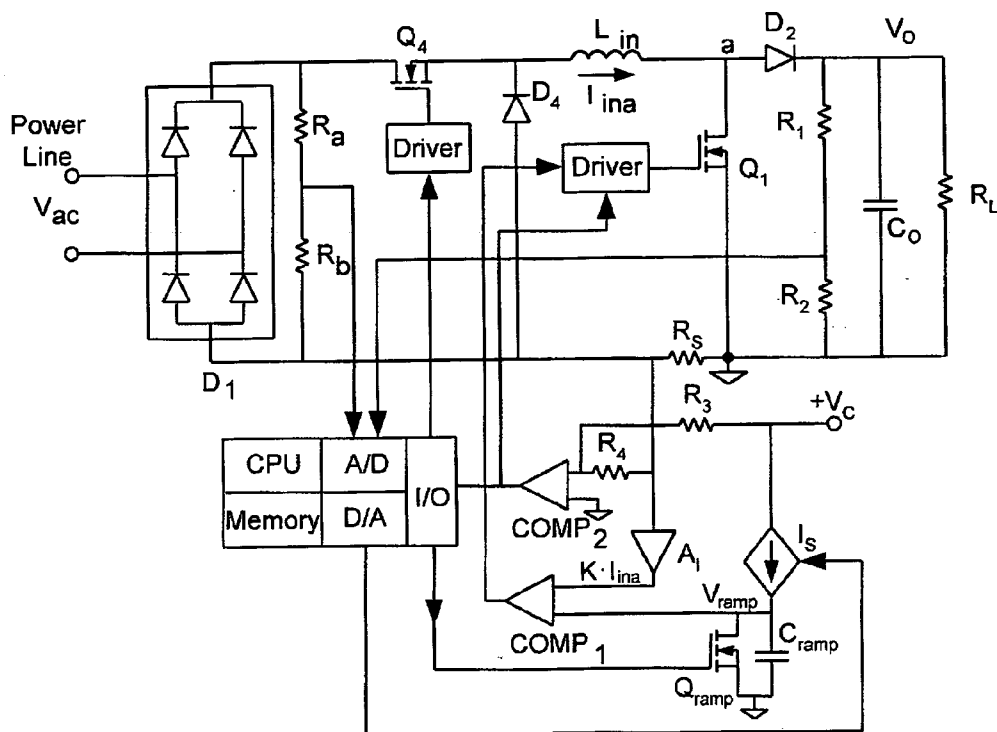


Fig. 7

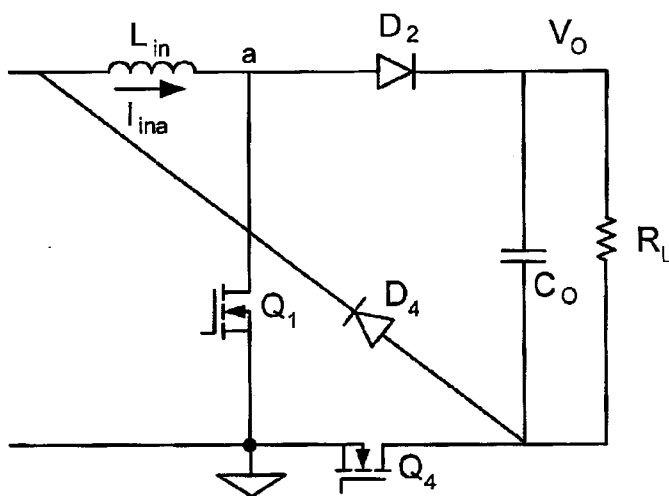


Fig. 8

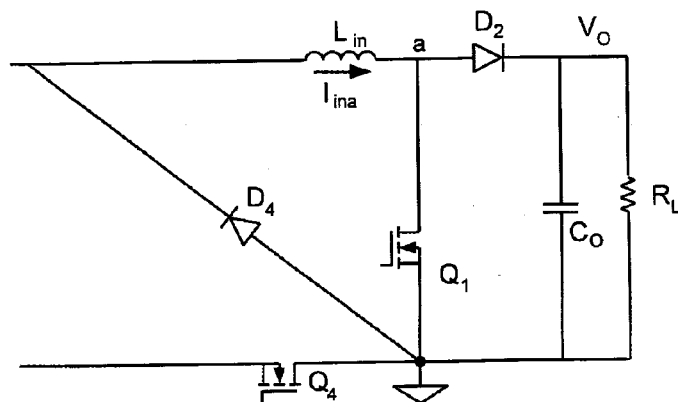


Fig. 9

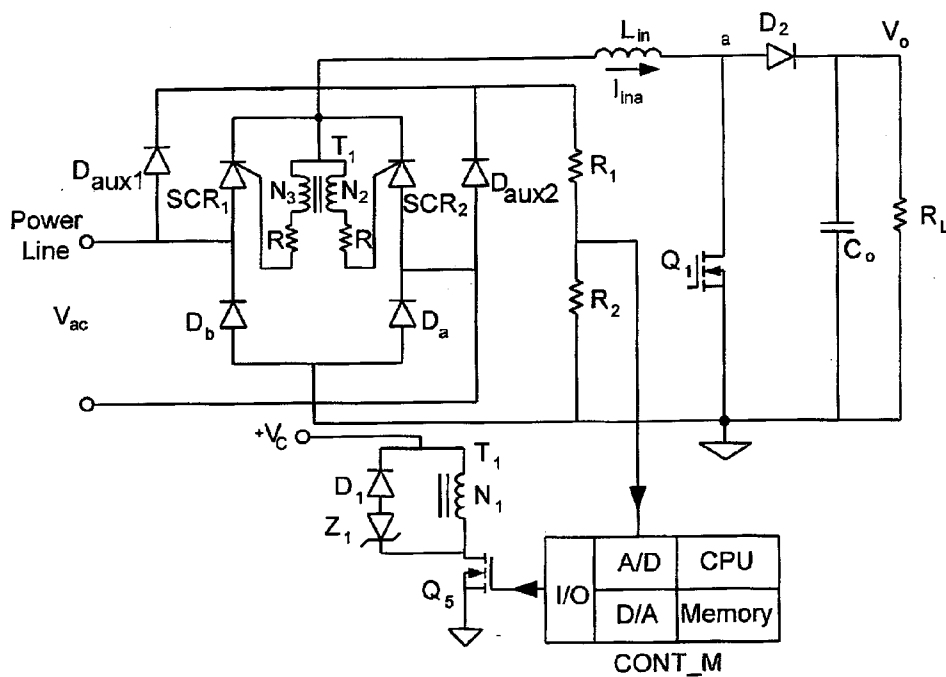


Fig. 10

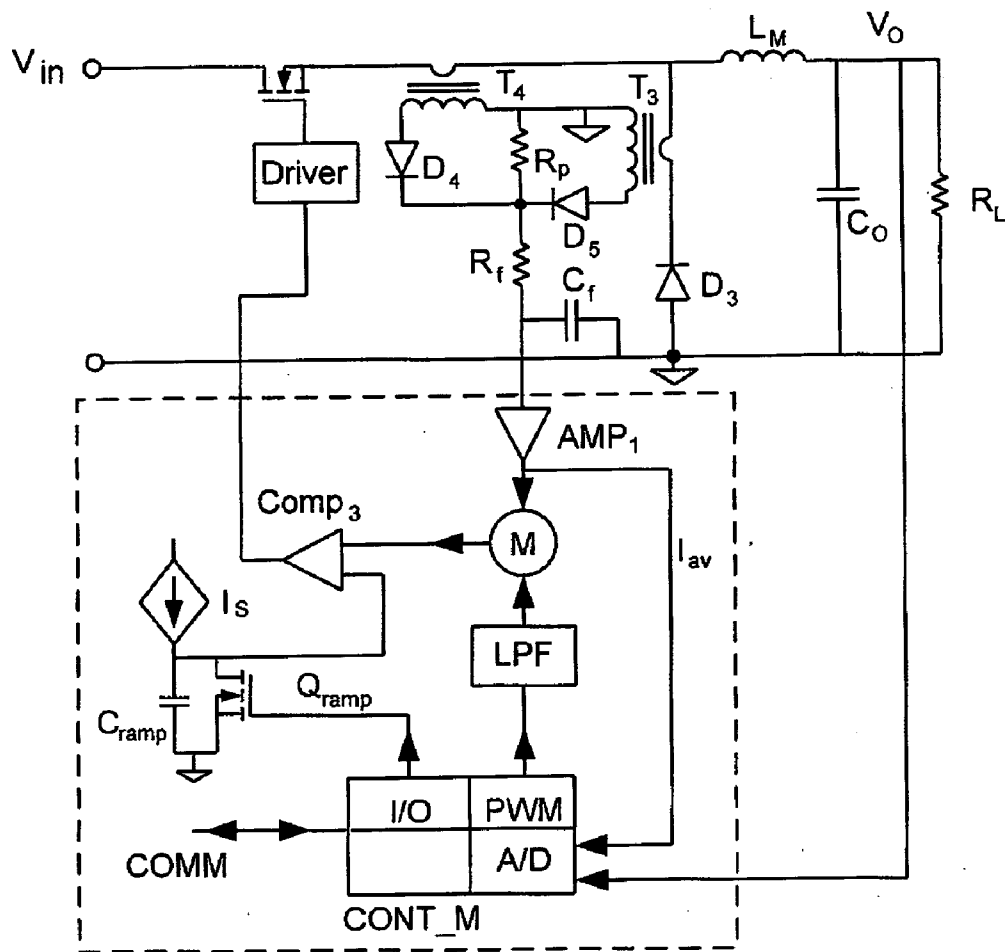


Fig. 11



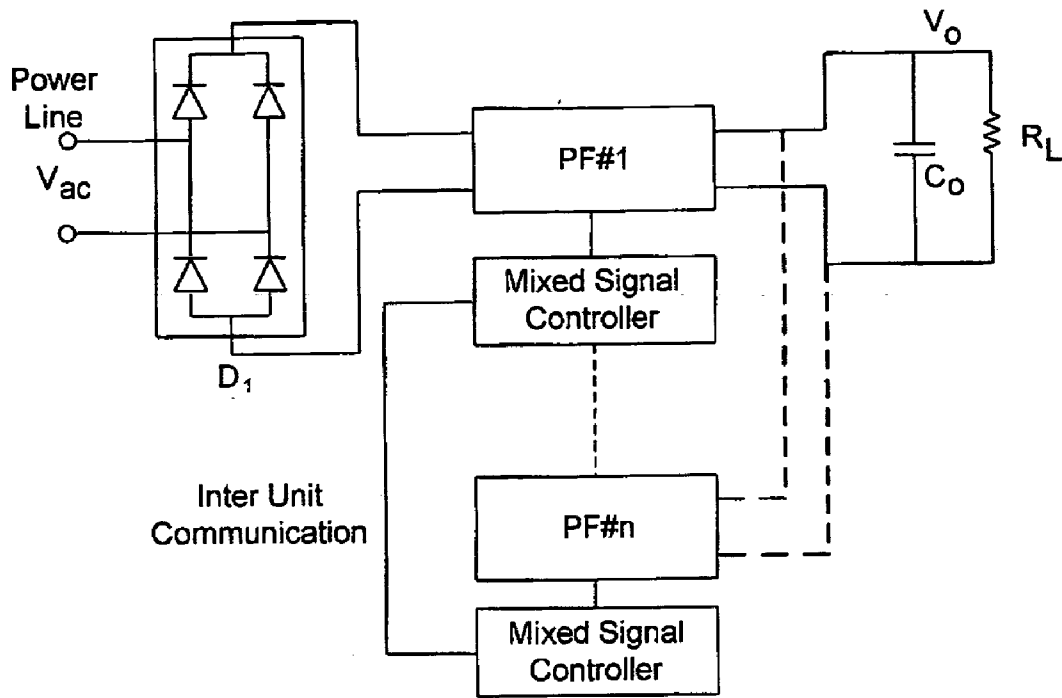


Fig. 12.

## METHOD AND CONTROL CIRCUITRY FOR IMPROVED-PERFORMANCE SWITCH-MODE CONVERTERS

### RELATED APPLICATIONS

[0001] This application claims the benefit of earlier-filed provisional application Ser. No. 60/592,377, filed on Aug. 2, 2004 and entitled "Method and Controller Circuitry for Improved Performance Switch-Mode Converters".

### FIELD AND BACKGROUND OF THE INVENTION

[0002] The present invention relates to the field of switching power converters. More particularly, the present invention relates to a method and circuitry for improving the input current and/or output voltage regulation of switching power converters.

[0003] Currently, there are several types of power converters which are widely used for DC-to-DC, DC-to-AC, AC-to-DC and AC-to-AC power conversion. In some applications the purpose of the converter is to provide a regulated output voltage. In other applications the purpose of the power conversion scheme is to shape the input current at the input terminals of the converter so that the input current will follow the shape of the input voltage. For example, in a power converter known in the art as an Active Power Factor Correction (APFC) converter, the role of the converter is to ensure that the current drawn from the AC power line is in phase with the line voltage with minimum high-order harmonics. A typical and well-known implementation of an APFC converter is illustrated in FIG. 1 (prior art). In FIG. 1, input voltage  $V_{ac}$  is rectified by diode bridge  $D_1$  and fed to a "Boost" or "Step-up" converter that includes an input inductor  $L_{in}$ , a transistor  $Q_1$ , a high frequency rectifier  $D_2$ , an output filter capacitor  $C_o$  and a load  $R_L$ . A power switch  $Q_1$  is driven by a high frequency control signal having a duty-cycle  $D_{ON}$  so as to force an input current  $I_{ina}$  to follow the shape of rectified input voltage  $V_{inR}$ , in which case the power converter behaves essentially as a resistive load on the AC power line; i.e., the power factor (PF) is unity.

[0004] The growing use of APFC converters is driven by the concern for the quality of AC power line supplies. Injection of high harmonics into the power line, and poor power factor in general, are known to cause many problems. Among these are lower efficiency of power transmission, possible interference to other electrical units connected to the power line and distorted shape of the line voltage. In light of the practical importance of APFC converters, many countries have adopted, or are in the process of adopting, voluntary and mandatory standard and statutes, which set limits on the permissible current line harmonics injected by any given electrical equipment powered by the AC mains, in order to maintain relatively high power quality. Another advantage of an APFC converter is that it allows a better exploitation of the power that can be drawn from a given AC power line. Without power factor correction, the current drawn from AC power line includes a relatively high level of unwanted harmonics, which may be greater than the magnitude of the first harmonic of the current, the latter being the only component that contributes real power to the load. The generally undesirable  $I^2R$  heating of wiring and motor and transformer windings is proportional to the square

of the rms value of the current, which includes contributions from all harmonics. Additionally, protection elements, such as fuses and circuit breakers, generally respond to the rms value of the current. Consequently, the rms value of the current limits the maximum power that can be drawn from the line. In equipment having power factor correction the rms current essentially equals the rms value of the first harmonic of the current (due to the suppression of higher harmonics) and, hence, the power that can be drawn from the line essentially reaches the maximum theoretical value. It is thus evident that the need for APFC circuits is widespread and that economical implementation of such circuits is of prime importance. Cost is of great concern considering the fact that the APFC is generally an additional expense not directly related to the basic functionality of the equipment in which the APFC converter is included.

[0005] Common APFC circuits generally operate in closed feedback configurations. For example, in the circuit illustrated in FIG. 1 (prior art) a power factor correction (PFC) controller CONT samples an input current  $I_{ina}$  and generates pulses  $D_{ON}$  in order to drive a power switch  $Q_1$  such as to force a current  $I_{ina}$  in an inductor  $L_{in}$  to follow the shape of a rectified input voltage  $V_{inR}$ . Input current  $I_{ina}$  is adjusted for any given load  $R_L$  by monitoring output of the voltage divider  $R_1, R_2$  to form a low-voltage sense voltage  $V_{od}$  proportional to an output voltage  $V_O$ , comparing it to a desired value for  $V_O$  and applying a resulting error signal to adjust  $D_{ON}$ . Controller CONT could be based on analog circuitry.

[0006] In the circuit illustrated in FIG. 2 (prior art) a controller CONT\_D is implemented as digital circuitry. In this system the shape of the rectified power line voltage  $V_{inR}$  is sampled by utilizing voltage  $V_{inR}$ , which is obtained from voltage divider  $R_a, R_b$ . In this case  $V_{inR}$  is used as the reference voltage for the desired shape of input current  $I_{ina}$ . Controller CONT\_D also receives a voltage  $V_{Rs}$ , measured across a sense resistor  $R_s$  and proportional to input current  $I_{ina}$ . By applying a preprogrammed control algorithm, CONT\_D generates pulses  $D_{ON}$  in order to drive power switch  $Q_1$  such as to force inductor current  $I_{ina}$  to follow reference voltage shape  $V_{inR}$ . Current  $I_{ina}$  is adjusted for any given load  $R_L$  by monitoring output voltage  $V_O$  via voltage divider  $R_1, R_2$  to generate a reference signal  $V_{od}$  that is applied in the algorithm of CONT\_D to adjust  $D_{ON}$  so as to keep  $V_O$  close to a predetermined level.

[0007] A digitally implemented controller has numerous advantages compared to an analog controller, such as the ability to adjust and optimize the control functions by re-programming the controller, even after installation, the robustness and stability of digital circuitry, as compared to analog circuitry, the ease of including remote control and monitoring functions via a communication interface, and the utilization of sophisticated new circuitry resulting from the rapid advancement of digital VLSI technology. Notwithstanding the many advantages of digital controllers, cost is still an obstacle that makes wide usage of this approach uneconomical in many applications. The main reason for the high cost is the requirement for a relatively wide-bandwidth control loop. In an APFC system two feedback loops are recognized: an "inner" current-control loop and an "outer" voltage-control loop. In the inner, current, loop the input current is sensed and the required control signal having an appropriate duty-cycle is generated according to a predetermined algo-

rithm. The bandwidth of this current-control loop must be wide, corresponding to a short response time. This helps to quickly correct any deviation of the current from the required value. On the other hand, the voltage-control loop needs to be slow-responding because its function is to correct the parameters of the inner loop so that the target input current will correspond to the power drawn by the load. In fact, a fast-responding outer loop is considered harmful because it will cause undesired distortion of the input current due to modulation by the ac ripple of the output voltage. This phenomenon is well known to persons trained in the art and this is why the design of the outer loop generally specifies a narrow bandwidth.

[0008] The requirement for a wide bandwidth for the inner current-control loop implies that, in the case of a digital controller, the rate of sampling of the input current signal must be high. This implies that the analog-to-digital (A/D) converter of the digital controller (see FIG. 2) must include fast-responding circuitry of high accuracy in order to provide the required performance of the inner loop. The need for a wide-bandwidth inner loop is demonstrated in detail by considering an APFC control algorithm that does not require sensing of input voltage, as seen in U.S. Pat. No. 6,307,361, to Ben-Yaakov et al., "Method and Apparatus for Regulating the Input Impedance of PWM Converters" incorporated by reference for all purposes as if fully set forth herein.

[0009] In FIGS. 1 and 2,  $V_a$  (the voltage at node "a") is a cyclic pulsating voltage having magnitude  $V_o$  during  $T_{OFF}$  when  $Q_1$  is in a non-conductive state, and zero during  $T_{ON}$ , when  $Q_1$  is in a conductive state. Consequently, the average value of  $V_a$  is:

$$\langle V_a \rangle = \frac{V_o T_{OFF}}{T_S} \quad (1)$$

wherein  $T_S$  is the Pulse Width Modulated (PWM) switching period, with  $T_S = T_{OFF} + T_{ON}$ , and the angle-brackets ( $\langle \rangle$ ) imply an average value over a switching period.

[0010] Equivalently,

$$\langle V_a \rangle = V_o D_{OFF} \text{ wherein} \quad (2)$$

$$D_{OFF} = \frac{T_{OFF}}{T_S} \quad (3)$$

[0011] Similarly,  $D_{ON}$  is defined as:

$$D_{ON} = \frac{T_{ON}}{T_S} \quad (4)$$

corresponding to when  $Q_1$  is in a conductive state.

[0012] The average voltage across inductor  $L_{in}$  is ( $V_{inR} - \langle V_a \rangle$ ) and the resulting average current  $\langle I_{ina} \rangle$  will be:

$$\langle I_{ina} \rangle = \left| \frac{V_{inR} - \langle V_a \rangle}{j2\pi L_{in} f} \right| \quad (5)$$

wherein  $f$  is the first harmonic component of the input current.

[0013] As has been shown in a number of publications (e.g., Ben-Yaakov, S. and Zeltser, I., "The dynamics of a PWM boost converter with resistive input." IEEE Trans. Industrial Electronics, 46, pp. 613-619, 1999), the control law required to insure that the input terminal of the APFC will exhibit a resistive nature and be equivalent to a resistance  $R_e$  is:

$$D_{off} = \frac{R_e}{V_o} \langle I_{ina} \rangle \quad (6)$$

[0014] The block diagram of FIG. 3 illustrates the interaction between Equations (5) and (6). The closed-loop response of this system is given by:

$$\frac{I_{ina}}{V_{inR}} = \left| \frac{1}{R_e} \frac{1}{1 + \frac{j2\pi f}{2\pi f_o}} \right| \text{ wherein:} \quad (7)$$

$$f_o = \frac{1}{2\pi} \frac{R_e}{L_{in}} \quad (8)$$

[0015] Equation (8) implies that good tracking

$$\left( \frac{I_{ina}}{V_{inR}} \cong \frac{1}{R_e} \right)$$

is obtained up to the break frequency  $f_o$ , at which point the loop gain of the system approaches unity. This implies that for proper operation, the controller should be capable of processing signals up to the frequency  $f_o$ . This is illustrated by considering, for example, a 1 kW APFC stage operating from a 220 Vac line and with  $L_{in} = 1$  mH. In this case:

$$R_e(1 \text{ kW}) = \frac{220^2}{10^3} = 48 \Omega \text{ and } f_o(1 \text{ kW}) = 7.6 \text{ kHz}$$

[0016] However, if the load power drops, say, to 5% of its nominal value, we find:

$$f_o(50 \text{ W}) = 153 \text{ kHz}$$

[0017] It will be clear to those trained in the art that the required sampling rate for this case is at least 500 kHz to avoid instabilities or poor dynamic response due to low sampling rates and sampling delays.

[0018] In order for the inner, current-control loop to be sufficiently accurate, both the resolution of the A/D and that of the PWM circuitry of the digital controller of FIG. 2)

need to be high. Because the resolution of the PWM signal of a digital controller is limited by the clock signal, the requirement for a high-resolution PWM signal implies that the digital controller must have a high clock frequency. For example, if the converter runs at a switching frequency of 100 kHz and the required resolution of the PWM signal is 1:1000 (10 bits resolution) then the required clock frequency will be 100 MHz.

[0019] In contrast to the strict requirements of the inner loop for a fast sampling rate, high accuracy of A/D conversion, and high clock frequency for generating a high-resolution PWM signal, the outer voltage loop can use a low sampling-rate A/D of relatively low accuracy. This is due to the fact, discussed above, that the required bandwidth for the outer loop is small. Typical values for bandwidth are 10 Hz (see again Ben-Yaakov, S. and Zeltser, I., "The dynamics of a PWM boost converter with resistive input."). The resolution of the A/D needed for the outer loop is relatively low because, in most practical applications, the required accuracy of  $V_o$  is relaxed. This is possible because the APFC stage is normally followed by a DC-DC converter that controls the final output voltages of the system. Such a DC-DC converter is typically rather insensitive to variations in input voltage. Notwithstanding the relaxed requirements of the outer loop, it is the inner loop that sets the specification of the digital controller for an APFC per the prior art of FIG. 2. Consequently, in this prior art implementation, the required bandwidth for the inner, current-control loop, and the need for a high-resolution PWM signal dictate the selection of a digital controller with a very high clock frequency and a high-resolution, fast-sampling A/D. This significantly increases the cost of the digital solution as compared to the analog approach for APFC controllers.

[0020] Another engineering issue that needs attention in the design of AC-DC converters is the control of the inrush current. That is, limiting the high current that will develop when power is applied to the system while bus capacitor  $C_o$  is discharged or at low voltage. Prior-art solutions to this problem fall into two categories. One approach is to insert a thermistor having a negative temperature coefficient in series with the input terminals. Because the resistance of the thermistor is large when the thermistor is cold, the thermistor will limit the inrush current. Once capacitor  $C_o$  has been charged and the thermistor has warmed up the resistance of the thermistor will decrease and the power dissipated in the thermistor will be reduced. Nonetheless, the thermistor will dissipate power even when warm, and therefore reduce the overall efficiency of the system. Furthermore the high steady-state temperature of the thermistor can reduce the reliability of the converter by introducing a hot spot. Another problem with the thermistor solution is that after a short brown-out period (reduction of line voltage) the inrush current resulting from restoration of full line voltage can be high because the thermistor may not have had enough time to cool down sufficiently during the brown-out.

[0021] A second approach to solving the inrush current problem is the introduction of an inrush-current control element activated by extra analog circuitry plus some logic circuitry operative to sense the instant of application of power to the system, as seen in U.S. Pat. No. 6,493,245 to Phadke, "Inrush Current Control for AC to DC Converters", incorporated by reference for all purposes as if fully set forth herein. It is also desirable that the inrush-current control

circuitry be capable of detecting a power-line brown-out so as to activate again the inrush current control element when full line voltage is restored. It is thus clear that the prior-art circuitry needs to be rather extensive, reducing the reliability, and increasing the manufacturing cost, of AC-DC converters.

[0022] In the foregoing discussion, emphasis has been placed on AC-DC converters with respect to the alternative methods for controlling such systems. However, the control issues illustrated above for APFC systems are also relevant to DC-DC switch-mode converters. In a typical prior-art converter, as illustrated schematically in FIG. 4, the objective of controller CONT is to stabilize output voltage  $V_o$  despite changes in load and input voltage. A typical DC-DC converter will include at least one switching element  $Q_1$ , an inductor  $L_{in}$ , and an output capacitor  $C_o$ . For enhanced performance, both inductor current  $I_{in}$  and output voltage  $V_o$  are sensed by controller CONT and used to generate the gate PWM pulse ( $D_{on}$ ). The purpose of sensing the inductor current is to make the inductor behave as a current source and thus reduce the small-signal transfer function of the power stage to that of a first-order system. This decreases the phase delay of the system and therefore helps to achieve a fast feedback response. As is well known in the art, the current-control feedback loop needs to have a wide bandwidth as compared to the voltage-control feedback loop. Hence, as in the case of the APFC systems detailed above, a digital controller for a DC-DC converter will require a high clock frequency and a high sampling-rate A/D converter.

[0023] As in the cases of AC-DC and DC-DC converters, a digital controller for DC-AC inverters will suffer from similar drawbacks. It is thus clear that, notwithstanding the many potential advantages of a digital controller for power switch-mode systems, prior art implementations are complex and costly.

#### SUMMARY OF THE INVENTION

[0024] There is thus a widely recognized need for, and it would be highly advantageous to have, controllers for switch-mode power systems that have the features of digital circuitry without the need for a high sampling-rate A/D and high-frequency clock. One, some or all of the below objectives may be realized in embodiments of the present invention.

[0025] It may be further desirable that a controller for an APFC system be able to be operated in an advanced manner in which there is no need to sample the input voltage, and be able to cope with the large bandwidths required by such a control scheme.

[0026] It is an objective of the present invention to provide circuitry for simplifying the construction, and increasing the reliability and flexibility, of controllers for switch-mode power systems.

[0027] It is another objective of the present invention to provide economical digital circuitry for improving the performance of switch mode controllers.

[0028] It is another objective of the present invention to eliminate the need for a high-resolution, high sampling-rate A/D and high-frequency clock presently associated with digital controllers for switch-mode power systems.

[0029] It is yet another objective of the present invention to provide controller circuitry that can integrate other functions, such as inrush current control and soft start, to simplify the construction, increase the reliability, and reduce the overall cost, of switch-mode converters.

[0030] Other objectives and advantages of the present invention will become apparent as the description proceeds.

#### Definitions

[0031] As used herein, unless otherwise specified, the term “line” refers to an electric power line having at least two conductors. Such lines include DC power lines and AC power lines. DC power lines include, but are not limited to, power lines wherein one conductor, referred to herein as a “neutral” conductor, is substantially at ground potential. AC power lines include, but are not limited to, power lines wherein one conductor is substantially at ground potential, and is known as a “neutral” conductor, and wherein another conductor is at a varying potential and is known as a “phase” or “hot” conductor.

[0032] As used herein, unless otherwise specified, the term “duty-cycle” refers to the ratio of the time a pulse signal is in an on state to the total of the time the pulse signal is in the on state and the time the pulse signal is in a temporally adjacent off state.

[0033] As used herein, unless otherwise specified, the term “off-duty-cycle” refers to the ratio of the time a pulse signal is in an off state to the total of the time the pulse signal is in the off state and the time the pulse signal is in a temporally adjacent on state.

[0034] Aspects of embodiments of the present invention are directed to a method for controlling the operation of a switch-mode converter stage such that, in the case of an APFC, the input current will follow the input line voltage, thus appearing to the power line as a resistive load, and/or, in the case of a voltage regulator, to regulate the output voltage or, in the case of a DC-AC converter, to produce a desired voltage waveform at the output terminals of the converter. This may be accomplished according to the present invention by use of mixed-mode circuitry combining an analog portion and a digital portion. Accordingly, certain embodiments of the present invention may make optimal use of both analog technology and digital technology and eliminate the need for extremely high A/D sampling rates and high-frequency clocks that increase the complexity and cost of purely digital controllers. Furthermore, the present invention also allows increasing the reliability of switch-mode converter systems by enabling the inclusion of additional functions such as inrush current control without adding considerable complexity and/or cost to the controller circuitry. A simplified diagram of a controller according to embodiments of the present invention is illustrated schematically in FIG. 5. The controller illustrated includes mixed-mode circuitry including an analog portion that is primarily for implementing an inner, current-control loop, and a digital portion that is for implementing an outer, voltage-control loop, carrying out logical decisions concerning delays following power failures or brown-outs, driving a Controlled Current Conducting Device (CCCD) used to control inrush current, and other functions that will become clear below.

[0035] Accordingly, embodiments of the present invention may be characterized by utilizing analog circuitry for fast control loops and digital control for slow control loops and supervisory circuitry.

[0036] Embodiments of the present invention may feature some or all of a switch-mode converter apparatus which has improved reliability, programmability features, and lower cost, compared to prior art, for switch-mode power converters, including at least an inductor, a controllable power switch connected in tandem with the inductor, and a mixed-mode controller.

[0037] In some embodiments of the invention, the switch mode converter may include some or all of:

[0038] a) voltage sampling circuitry, for sampling the instantaneous value of the output voltage level;

[0039] b) inductor-current sampling circuitry, for sampling the instantaneous value of the inductor current;

[0040] c) analog control circuitry fed by a signal proportional to the input current and which controls the timing of the switching of the controllable switch in response to input current so as to cause the waveshape of the input current to be essentially similar to the waveshape of the input voltage.

[0041] d) digital control circuitry fed by a signal proportional to the output voltage and which produces a control signal that affects the analog circuitry so as to adjust the input current level to the load and thereby stabilize the input current level and/or output voltage to desired values. The digital circuitry, which may be implemented as embedded firmware or as software running on a data processor such as a computer or microcontroller, can also, optionally, control the operation of the inrush circuitry and/or soft start of the power converter.

[0042] e) inrush current control circuitry operative to limit input current following power-on, operation of the inrush current control circuitry being controlled by the digital control circuitry.

[0043] Preferably, the switch-mode converter may further include:

[0044] f) input voltage sensing circuitry operative to sense the input voltage of the system.

[0045] g) logic-based circuitry or a program operative to utilize the sensed signals of input voltage, input current and output voltage to produce logic commands operative to shift the converter circuitry from one operational mode to another.

[0046] The analog control circuitry can, optionally, further include an amplifier operative to increase the signal level of the sensed input current, a comparator operative to compare the input current signal to a ramp voltage developing across a ramp capacitor, a controlled current source operative to charge the ramp capacitor, interface circuitry operative to interface the digital control circuitry with control terminals of the controlled current source, and a gate driver fed by the comparator and operative to drive the gate of the power switch.

[0047] The inrush current control circuitry can optionally further include a Controlled Current Conducting Device (CCCD) in series with inductor  $L_{in}$  and controlled by the

digital circuitry. During start-up the CCCD is set by the digital circuitry to limit the input current. After the main capacitor is charged the digital circuitry is operative to change the setting of the CCCD such that the CCCD will carry the full current with minimal voltage drop across the CCCD.

**[0048]** According to embodiments of the present invention there may be provided an active power factor correction power converter system comprising an analog control circuitry to control an input current of said system; a digital control circuitry to control an output voltage of said system; a current sampling device in the path of said input current to indicate an instantaneous value proportional to said input current being an input current indication, wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, and wherein said analog control circuitry is responsive to said analog signal.

**[0049]** According to some embodiments of the present invention, there may be provided a method of controlling an input current and an output voltage in an active power factor correction power converter system comprising controlling an input current of said system by an analog control circuitry; controlling an output voltage of said system by a digital control circuitry; wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, and wherein said analog control circuitry is responsive to said analog signal.

**[0050]** According to further embodiments of the present invention, there may be provided an active power factor correction power converter system comprising an analog control circuitry to control an input current of said system; a digital control circuitry to control an output voltage of said system; a current sampling device in the ground path of said input current to indicate an average of an instantaneous value proportional to said input current being an input current indication; a first voltage sampling branch to indicate an instantaneous value of said output voltage being an output voltage indication; a comparator unit responsive to a signal proportional to said input current indication and to a ramp-type signal driven by a controllable current source; a controllable current source to control the rise rate of said ramp-type signal to responsive to said output voltage indication; and a second voltage sampling branch to indicate an instantaneous value of a rectified input voltage of said system being an input voltage indication, wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, wherein said analog control circuitry is responsive to said analog signal, wherein said digital control circuitry further comprises a digital controller comprising logic unit, a digitally controlled analog output, an analog-to-digital converter and an input/output unit.

**[0051]** According to further embodiments of the invention, there may be provided a method of controlling an input current and an output voltage in an active power factor correction power converter system comprising controlling an input current of said system by an analog control circuitry; controlling an output voltage of said system by a digital control circuitry, said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, receiving a signal proportional to an

average of said input current being an input current indication; receiving a signal proportional to an instantaneous value of said output voltage being an output voltage indication comparing said signal proportional to said input current indication to a ramp-type signal; switching a current controllable shunt switch on whenever said signal proportional to said input current indication is bigger than said ramp-type signal and off when it is smaller than said ramp-type signal; controlling a rise rate of said ramp-type signal responsive to a deviation of said output voltage indication from a predetermined value; and controlling a maximum value of said input current by a controllable switching device in response to a signal from said digital control circuitry.

**[0052]** According to yet further embodiments of the present invention, there may be provided a power converter system comprising a rectifying circuitry to rectify an AC power to DC power; an analog control circuitry to control a current drawn from said rectifying circuitry; a digital control circuitry to control an output voltage of said system; a current sampling device in the ground path of said input current to indicate an average of an instantaneous value proportional to said input current being an input current indication; a first voltage sampling branch to indicate an instantaneous value of said output voltage being an output voltage indication; a comparator unit responsive to a signal proportional to said input current indication and to a ramp-type signal driven by a controllable current source; a controllable current source to control the rise rate of said ramp-type signal to responsive to said output voltage indication; and a second voltage sampling branch to indicate an instantaneous value of a rectified input voltage of said system being an input voltage indication, wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, wherein said analog control circuitry is responsive to said analog signal, and wherein said digital control circuitry further comprises a digital controller comprising logic unit, a digitally controlled analog output, an analog-to-digital converter and an input/output-unit.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0053]** The above and other characteristics and advantages of the invention will be better understood through the following illustrative and non-limitative detailed description of preferred embodiments thereof, with reference to the appended drawings, wherein:

**[0054]** FIG. 1 (prior art) illustrates schematically an APFC boost converter based on an analog controller;

**[0055]** FIG. 2 (prior art) illustrates schematically an APFC boost converter based on a digital controller;

**[0056]** FIG. 3 (prior art) illustrates schematically, as a block diagram, a current-control loop of an APFC based on a controller which does not directly sense input voltage;

**[0057]** FIG. 4 (prior art) illustrates schematically two-loop control of a Buck converter;

**[0058]** FIG. 5 illustrates schematically a control scheme for a switch-mode converter according to the present invention;

**[0059]** FIG. 6 illustrates schematically an APFC stage according to a preferred embodiment of the present invention;

[0060] FIG. 7 illustrates schematically an APFC stage according to another embodiment of the present invention;

[0061] FIG. 8 illustrates schematically a possible series transistor connection for implementing the CCCD of the present invention;

[0062] FIG. 9 illustrates schematically a second possible series transistor connection for implementing the CCCD of the present invention;

[0063] FIG. 10 illustrates schematically a possible use of SCRs in implementing the CCCD of the present invention;

[0064] FIG. 11 illustrates schematically a buck converter stage according to an embodiment of the present invention;

[0065] FIG. 12 illustrates schematically a parallel connection of multiple APFC stages according to an embodiment of the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0066] The present invention is of a power converter which can provide a desired output voltage to a load while presenting the power line with a load having desired characteristics, such as, for example, unity power factor.

[0067] Referring now to the drawings, FIG. 6 illustrates a possible embodiment of an APFC stage according to the present invention. The power stage includes an inductor  $L_{in}$ , a main switch  $Q_1$ , a main diode  $D_2$ , and an output capacitor  $C_o$ . The power stage also includes a relay REL having contacts connected in series with inductor  $L_{in}$ . A charging resistor  $R_{limit}$  is placed across the contacts of relay REL so that when those contacts are non-conducting current will flow will be limited by  $R_{limit}$ . According to the present invention, a mixed mode controller CONT\_M, having an analog section and a digital section, samples input voltage, input current  $I_{ina}$ , and output voltage  $V_o$ . The input current signal is processed according to a predetermined control algorithm by the analog section of CONT\_M to produce pulses to be applied to the gate of  $Q_1$ . The digital section or CONT\_M senses output voltages  $V_o$  and compares  $V_o$  to a desired, pre-programmed value, and produces a correction signal applied to the inner loop analog circuitry so as to adjust the input current to the load power at any given time. The digital section of CONT\_M also senses the input voltage to detect the need for inrush current control. Before the system enters the normal state of operation the “normally open” contacts of inrush control relay REL are non-conducting and resistor  $R_{limit}$  is thus in series with inductor  $L_{in}$ . Consequently, during “power-on” bus capacitor  $C_o$  will charge via resistor  $R_{limit}$ , thus limiting the inrush current. Further, during the charging of capacitor  $C_o$  the digital section of CONT\_M disables the analog section of controller CONT\_M such that main switch  $Q_1$  will be kept in the “off” state. Once the digital section of CONT\_M has sensed that capacitor  $C_o$  is sufficiently charged, and if input voltage is detected to be within a pre-determined allowable region, the digital section of CONT\_M activates relay REL so as to effectively bypass  $R_{limit}$  from the circuit. At the same time the digital section gradually reduces the disabling command to the analog section of CONT\_M such that the duty-cycle  $D_{ON}$  of  $Q_1$  will be allowed to increase, in accordance with the method known in the art as “soft start”.

[0068] FIG. 7 illustrates schematically another embodiment of an APFC stage according to the present invention. Input current  $I_{ina}$  is sensed by sense resistor  $R_s$  and amplified by an amplifier  $A_1$  operative to produce a signal  $K \cdot I_{ina}$  proportional to  $I_{ina}$ . A ramp generator including a controlled current source  $I_s$ , a capacitor  $C_{ramp}$ , and a switch  $Q_{ramp}$  is operative to generate a triangular waveform  $V_{ramp}$  that is compared to  $K \cdot I_{ina}$  by a comparator  $COMP_1$  operative to produce a signal having an off-duty-cycle  $D_{OFF}$  according to equation (6):

$$D_{OFF} = \frac{R_e}{V_o} \langle I_{ina} \rangle$$

[0069] A digital controller 10 is operative to adjust coefficient  $R_e/V_o$  so as to match input current  $I_{ina}$  to load power. This is accomplished by comparing a measurement of output voltage  $V_o$  to a desired value for output voltage  $V_o$  and adjusting  $I_s$  to change the rate at which  $V_{ramp}$  increases during the charging of  $C_{ramp}$ . For example, if the measured value of  $V_o$  is less than the desired value of  $V_o$ , as would be the case after a decrease in load resistance  $R_L$ , digital controller 10 increases  $I_s$ , causing comparator  $COMP_1$  to turn on earlier in the  $V_{ramp}$  cycle, in turn increasing  $I_{ina}$  and causing  $V_o$  to increase toward the desired value for  $V_o$ . On the other hand, if the measured value of  $V_o$  is greater than the desired value for  $V_o$ , as would be the case after an increase in load resistance  $R_L$ , digital controller 10 decreases  $I_s$ , causing comparator  $COMP_1$  to turn on later in the  $V_{ramp}$  cycle, in turn decreasing  $I_{ina}$  and causing  $V_o$  to decrease toward the desired value for  $V_o$ . These changes in  $I_{ina}$  change the equivalent resistance  $R_e$  seen by the power line, and thus adjust coefficient  $R_e/V_o$  until output voltage  $V_o$  equals the desired target value for  $V_o$ . As discussed above, this correction need not be fast, so a low sampling rate will suffice. As an example, not to taken as limiting the present invention, a system according to the present invention operating with a power line frequency of 50 Hz can have a bandwidth of 10 Hz in the voltage-control loop and hence a sampling rate of let then 1000 samples per second will suffice. It will be readily apparent to those skilled in the art that adjustment of  $I_s$  by digital controller 10 as described above will compensate for changes in component values in the system, as may occur with aging or temperature changes, other than changes in the voltage-sensing circuitry, and for changes in such parameters as input voltage  $V_{ac}$  and output resistance  $R_L$ .

[0070] Inrush current limiting and protection against a short circuit at the output is provided by a series switch,  $Q_4$ , that is controlled in PWM mode by controller 10 so as to limit the inrush current and to disconnect the circuit when an overcurrent is detected by comparator  $COMP_2$ . The output of  $COMP_2$  also disables the drive to main switch  $Q_1$  for quick protection. Diode  $D_4$  is operative to provide a current path for current flowing through inductor  $L_{in}$  when switch  $Q_4$  is in a non-conductive state. Other possible arrangements for providing inrush current limiting protection are depicted in FIGS. 8, 9 and 10.

[0071] In FIGS. 8 and 9 series transistor  $Q_4$  is placed in the ground branches. This lowers the common-mode noise injection. The advantage of the arrangement of FIG. 8 is the common ground for both  $Q_1$  and  $Q_4$ , eliminating the need for

gate drive isolation for  $Q_4$ . The advantage of the connection of **FIG. 9** is that it does not break the connection between the ground of  $Q_1$  and the ground of load  $R_L$ .

[0072] In the connection of **FIG. 10**, the inrush current is controlled by thyristors  $SCR_1$  and  $SCR_2$ . The control signal is generated by the digital portion of mixed-mode controller  $CONT\_M$  and fed to a pulse transformer  $T_1$  via a transistor  $Q_5$ . Input voltage sensing is facilitated by auxiliary diodes  $D_{aux1}$  and  $D_{aux2}$ .

[0073] Implementation of the present invention in a DC-DC converter is shown in **FIG. 11**. In this example the power stage is of the "buck" topology, and includes a power switch  $Q_4$ , an inductor  $L_M$ , a diode  $D_3$  and an output filter capacitor  $C_o$  to which a load  $R_L$  is connected. Pulse transformers  $T_3$  and  $T_4$  are used to monitor current through inductor  $L_M$ , generating a voltage across a sense resistor  $R_p$ . Resistor  $R_f$  and capacitor  $C_f$  filter out the high-frequency components and amplifier  $AMP1$  amplifies this voltage to a level that is compatible with the input signal range of a multiplier  $M$ . This signal, which is proportional to the average current through inductor  $L_M$ , is multiplied by an error signal generated by the digital portion of mixed-mode controller  $CONT\_M$  to correct changes in output voltage  $V_o$ . The output signal of multiplier  $M$  is fed to a comparator  $COMP3$  that generates the PWM signal. This is accomplished by comparing the output of multiplier  $M$  to a triangular wave generated by a current source  $I_s$  that feeds a ramp capacitor  $C_{ramp}$  which is discharged by transistor  $Q_{ramp}$  at the desired switching frequency. The digital portion of mixed-mode controller  $CONT\_M$  includes, in this embodiment, a logic core, such as a programmable micro-processor or logic array and digital input/output ports. Mixed-mode controller  $CONT\_M$  also includes an A/D section and a capture and compare port, and is operative to generate a PWM signal. The error signal, which is a function of the deviation of output voltage  $V_o$  from a desired value, is converted to a PWM signal which is then filtered by low pass filter  $LPF$  to form an analog signal that is fed to multiplier  $M$ . In the controller scheme of **FIG. 11**, amplifier  $AMP1$ , multiplier  $M$  and the PWM modulator built around comparator  $COMP_3$ , provide the wide bandwidth required for the inner, current-control loop so that the converter can quickly respond to fast current changes. Overall voltage stabilization, which, as mentioned above, requires a lower bandwidth, is controlled by the digital portion of the controller. By sampling the amplified signal that represents the average current,  $I_{av}$ , through inductor  $L_M$ , controller  $CONT\_M$  can detect a persistent overcurrent situation and adjust the PWM signal accordingly. Controller  $CONT\_M$  can also, optionally, send information about the loading level to a supervisory device, such as a computer (not shown) via a communication link  $COMM$ .

[0074] Another embodiment of the present invention is a multiple converter system as illustrated schematically in **FIG. 12**. This figure shows  $n$  converters  $PF\#1 \dots PF\#n$  that are powered from the line and connected in parallel to feed a single load  $R_L$ . Inter-unit communication, facilitated by the present invention, allows for current sharing between units  $PF\#1 \dots PF\#n$  so as not to overload any one of the units  $PF\#1 \dots PF\#n$  and to evenly distribute power losses.

[0075] While the invention has been described with respect to a limited number of embodiments, it will be

appreciated that many variations, modifications and other applications of the invention may be made.

What is claimed is:

1. An active power factor correction power converter system comprising:

an analog control circuitry to control an input current of said system;

a digital control circuitry to control an output voltage of said system;

a current sampling device in the path of said input current to indicate an instantaneous value proportional to said input current being an input current indication

wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, and

wherein said analog control circuitry is responsive to said analog signal.

2. The system of claim 1 wherein said current sampling device is placed in the ground path of said input current.

3. The system of claim 2 wherein said analog control circuitry further comprises:

a comparator unit responsive to an average of said input current indication and to a ramp-type signal generate by a controllable current source; and

a current controlling shunt switch to control the current drawn from a power source of said system,

wherein said current controlling shunt switch is switchable on or off responsive to a signal from said comparator.

4. The system of claim 1 wherein said digital control circuitry comprises a first voltage sampling branch to indicate an instantaneous value of said output voltage being an output voltage indication.

5. The system of claim 4 wherein said digital control circuitry further comprising a digital controller comprising a logic unit, a digitally controlled analog output, an analog-to-digital converter and an input/output unit.

6. The system of claim 5 wherein said digital controller further comprises a data storage unit.

7. The system of claim 4 wherein said digital control circuitry further comprises a second voltage sampling branch to indicate an instantaneous value of a rectified input voltage of said system being an input voltage indication

8. The system of claim 3 further comprising:

a controllable switching device connected in series in the path of said input current to limit said input current.

9. The system of claim 8 wherein said controllable switching device is controllable by a signal from said digital controller.

10. The system of claim 9 wherein said controllable switching device is connected in the ground path of said input current.

11. The system of claim 10 wherein said current controllable shunt switch and said controllable switching device are connected to have a common grounding node.

12. A method of controlling an input current and an output voltage in an active power factor correction power converter system comprising:



- controlling an input current of said system by an analog control circuitry;
- controlling an output voltage of said system by a digital control circuitry;
- wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage, and
- wherein said analog control circuitry is responsive to said analog signal.
- 13.** The method of claim 12 further comprising receiving a signal proportional to said input current being an input current indication.
- 14.** The method of claim 13 further comprising: comparing an average of said input current indication to a ramp-type signal; and
- switching a current controlling shunt switch on or off in response to the result of said comparing step.
- 15.** The method of claim 12 further comprising: receiving a signal proportional to an instantaneous value of said output voltage.
- 16.** The method of **15** further comprising: receiving a signal proportional to an instantaneous value proportional to a rectified input voltage of said system.
- 17.** The method of claim 14 further comprising: controlling a maximum value of said input current by a controllable switching device in response to a signal from said digital control circuitry.
- 18.** The method of claim 17 further comprising: connecting said controllable switching device in series with the ground path of said input current.
- 19.** An active power factor correction power converter system comprising:
- an analog control circuitry to control an input current of said system;
  - a digital control circuitry to control an output voltage of said system;
  - a current sampling device in the ground path of said input current to indicate an average of an instantaneous value proportional to said input current being an input current indication;
  - a first voltage sampling branch to indicate an instantaneous value of said output voltage being an output voltage indication;
  - a comparator unit responsive to a signal proportional to said input current indication and to a ramp-type signal driven by a controllable current source;
  - a controllable current source to control the rise rate of said ramp-type signal to responsive to said output voltage indication; and
  - a second voltage sampling branch to indicate an instantaneous value of a rectified input voltage of said system being an input voltage indication,
- wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage,
- wherein said analog control circuitry is responsive to said analog signal
- wherein said digital control circuitry further comprises a digital controller comprising logic unit, a digitally controlled analog output, an analog-to-digital converter and an input/output unit.
- 20.** A method of controlling an input current and an output voltage in an active power factor correction power converter system comprising:
- controlling an input current of said system by an analog control circuitry;
  - controlling an output voltage of said system by a digital control circuitry, said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage,
  - receiving a signal proportional to an average of said input current being an input current indication;
  - receiving a signal proportional to an instantaneous value of said output voltage being an output voltage indication
  - comparing said signal proportional to said input current indication to a ramp-type signal;
  - switching a current controllable shunt switch on whenever said signal proportional to said input current indication is bigger than said ramp-type signal and off when it is smaller than said ramp-type signal;
  - controlling a rise rate of said ramp-type signal responsive to a deviation of said output voltage indication from a predetermined value; and
  - controlling a maximum value of said input current by a controllable switching device in response to a signal from said digital control circuitry.
- 21.** A power converter system comprising:
- a rectifying circuitry to rectify an AC power to DC power;
  - an analog control circuitry to control a current drawn from said rectifying circuitry;
  - a digital control circuitry to control an output voltage of said system;
  - a current sampling device in the ground path of said input current to indicate an average of an instantaneous value proportional to said input current being an input current indication;
  - a first voltage sampling branch to indicate an instantaneous value of said output voltage being an output voltage indication;
  - a comparator unit responsive to a signal proportional to said input current indication and to a ramp-type signal driven by a controllable current source;
  - a controllable current source to control the rise rate of said ramp-type signal to responsive to said output voltage indication; and
  - a second voltage sampling branch to indicate an instantaneous value of a rectified input voltage of said system being an input voltage indication,

wherein said digital control circuitry is adapted to produce an analog signal responsive to variations in said output voltage,

wherein said analog control circuitry is responsive to said analog signal, and

wherein said digital control circuitry further comprises a digital controller comprising logic unit, a digitally controlled analog output, an analog-to-digital converter and an input/output unit.

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