OP AMP APPLICATIONS

The AD627 Single-Supply Two Op Amp In-Amp

The above-mentioned CM limitations can be overcome with some key modifications to the basic two op amp in-amp architecture. These modifications are implemented in the circuit shown in Figure 2-10 below, which represents the AD627 in-amp architecture.

In this circuit, each of the two op amps is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1, and Q2/A2, respectively. The PNP transistors not only provide gain but also level shift the input signal positively by about 0.5V, thereby allowing the common mode input voltage to go to 0.1V below the negative supply rail. The maximum positive input voltage allowed is 1V less than the positive supply rail.

\[ V_{OUT} = G(V_2 - V_1) + V_{REF} \]

**Figure 2-10: The AD627 in-amp architecture**

The AD627 in-amp delivers rail-to-rail output swing, and operates over a wide supply voltage range (+2.7V to ±18V). Without the external gain setting resistor \( R_G \), the in-amp gain is a minimum of 5. Gains up to 1000 can be set with the addition of this external resistor. Common mode rejection of the AD627B at 60Hz with a 1kΩ source imbalance is 85dB when operating on a single +3V supply and \( G = 5 \).

Even though the AD627 is a two op amp in-amp, it is worthwhile noting that it is not subject to the same CM frequency response limitations as the basic circuit of Fig. 2-7. A patented circuit keeps the AD627 CMR flat out to a much higher frequency than would otherwise be achievable with a conventional discrete two op amp in-amp.

The AD627 data sheet has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages (see Reference 7). In addition, interactive design tools are available on the ADI web site, which perform calculations relating these parameters for a number of in-amps, including the AD627.