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Optimization of the auxiliary switch components in ZVS PWM converters

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A family of PWM converters with an 'auxiliary-switch assisted soft switcher' (AASS) is studied. The basic AASS cell includes an inductor connected in series with the auxiliary switch of the converter, a capacitor in parallel with the main switch or main diode of the converter and an additional capacitor (designated a 'flying' capacitor) connected through an auxiliary diode parallel to the inductor and through an extra auxiliary diode parallel to the main diode of the converter. The unified analysis of steady-state processes in a generalized AASS converter, carried out in this investigation, is applicable to various PWM topologies. It is shown that AASS insures soft switching of all power devices and that the voltage and current stresses are not appreciably higher than in the corresponding hard switched PWM topologies. A design procedure for optimization of AASS parameters is developed. Experimental investigation (a Boost DC–DC converter 130/380 V, 1·1 kW, switching frequency 100...160 kHz) confirmed the results of the theoretical analysis.

1. Introduction

Different topologies of 'zero voltage switchings' (ZVS) PWM converters with an auxiliary switch have been proposed in the last few years (Streit and Tollik 1991, Hua *et al.* 1992, Martins, *et al.* 1993).

The boost topology described by Streit and Tollik (1991), called below the 'auxiliary-switch assisted soft switcher' (AASS), has an important advantage: it ensures soft commutation of all power devices. Soft switching during turn on, for the main and auxiliary switches, is facilitated by a series inductor while the turn off processes, of both switches, are controlled by a single snubbing capacitor, designated below the 'flying capacitor' (FC). A diode bypass toggles this snubber between the main and auxiliary switches such that it is charged during turn off of the auxiliary switch and discharged during turn off of the main switch. Consequently, FC reduces the rate of voltage rise of both the main and auxiliary switches during turn off of each. The AASS is simple, easy to implement and can be applied in other types of PWM converter topologies (e.g. buck, buck–boost, Cuk, etc.). An important feature of the AASS is the fact that it does not increase device stresses appreciably and, in particular, does not hike the peak current of the auxiliary switch. Experiments with this topology conducted independently by this group suggest that this AASS scheme can indeed increase the overall efficiency of MOSFET-based DC–DC converters and active power factor conditioners operating at high switching frequencies (100 kHz and above). An additional bonus of the AASS is the reduction and almost elimination of parasitic switching oscillations which complicate the design of the input filters.

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The objective of the present study was to derive a topology-independent analytical model of the AASS family and to develop a design procedure for optimizing the snubber's parameters. This paper includes a unified analysis of steady-state processes in a generalized converter which applies the AASS. The results of this analysis are applicable to all PWM converter topologies. Also included in the paper are key design details of an experimental Boost converter which was built around the proposed soft switching strategy. The experimental results were found to agree extremely well with the analytical predictions.

2. The generalized AASS converter topology

The analysis presented here was based on the following assumptions.

(1) The converter's elements (switches, diodes, inductors and capacitors) are ideal.

(2) The inductance of the main inductors is infinitely large.

(3) The capacitance of the output capacitor in all converters and the capacitance of the main capacitor in the Cuk, Sepic and Zeta converters is infinitely high.

In the unified equivalent converter topology (Fig. 1) Q_1 is the main switch, Q_2 is the auxiliary switch and D is the main diode of the converter. Other elements (diodes D_1, D_2, D_3, inductor L_r and the capacitors C_1, C_2, C_3) are snubbing elements of the AASS. Note that C_1 and C_2 are connected in parallel and hence only one of them is theoretically required. However, C_1 includes the parasitic capacitances of Q_1 and D_1 while C_2 includes the parasitic capacitance of D. These parasitic capacitances should be taken into account when designing the converter. I_e is the current of the main inductor in buck, boost and buck-boost converters and the sum of the main inductor currents in Cuk, Sepic and Zeta converters. V_e is the voltage applied to the main and auxiliary transistors when they are 'off' and the main diode D is 'on'. Definitions of I_e and V_e for different PWM topologies are given in Table 1 (V_{in} and V_o are the input and output voltages of the converter, I_{in} and I_o are the input and output average currents).

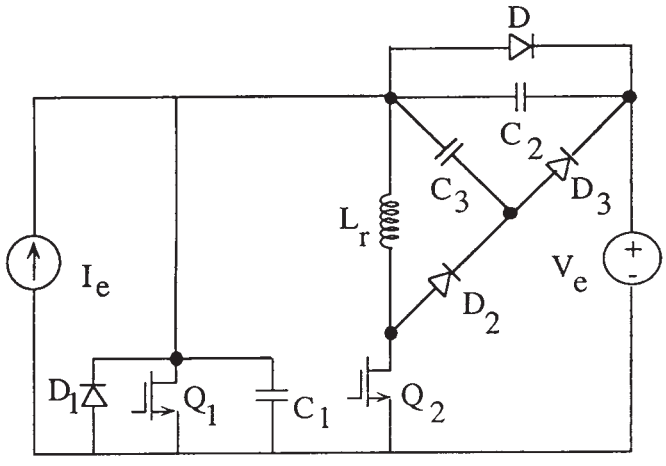

Figure 1. The equivalent circuit of the generalized AASS. See Table 1 for interpretation of the equivalent sources V_e and I_e.

3. Main results of the unified analysis

As will be shown below, the converter can operate in two possible modes: M1 and M2. Current and voltage waveforms of M1 and M2 and given in Figs 2 and 3. First we examine the time intervals which are the same in M1 and M2.

(1) The power delivering interval when both transitors are 'off' and the diode D is 'on'. The diode current is constant: $i_D = I_e$. This interval ends at t_0 when the auxiliary transistor Q_2 is turned on.

(2) Interval $t_o - t_1$. The auxiliary transistor Q_2 and the diode D are 'on'. They close a loop which includes the inductor L_r and the voltage source V_e. A commutation process that involves diode D and transistor Q_2 is started and the transistor current rises according to

$$i_{Q_2} = i_r = \frac{V_e}{L_r}(t - t_o) \tag{1}$$

Topology	Buck	Boost	Buck–boost, Cuk, Sepic, Zeta
I_e	I_o	I_{in}	$I_{in} + I_o$
V_e	V_{in}	V_o	$V_{in} + V_o$

Table 1. Definitions of (V_e) and (I_e) of Fig. 1 for various PWM topologies.

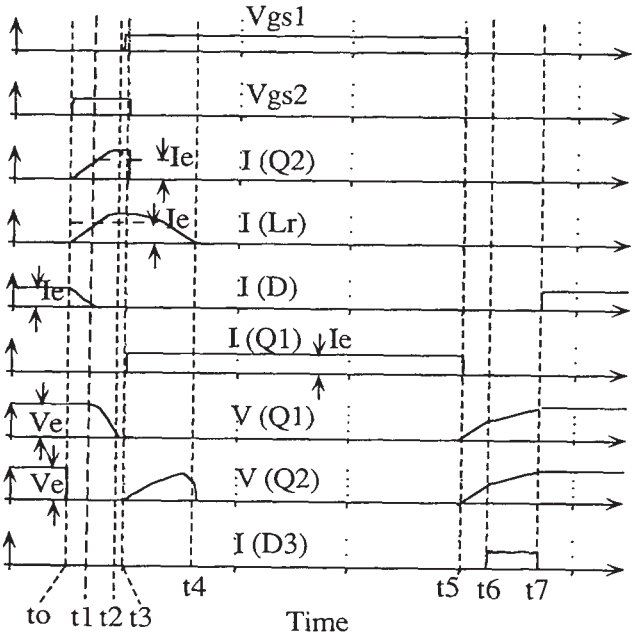

Figure 2. Basic waveforms of the proposed AASS when operating in M1 mode. See Fig. 1 for notation.

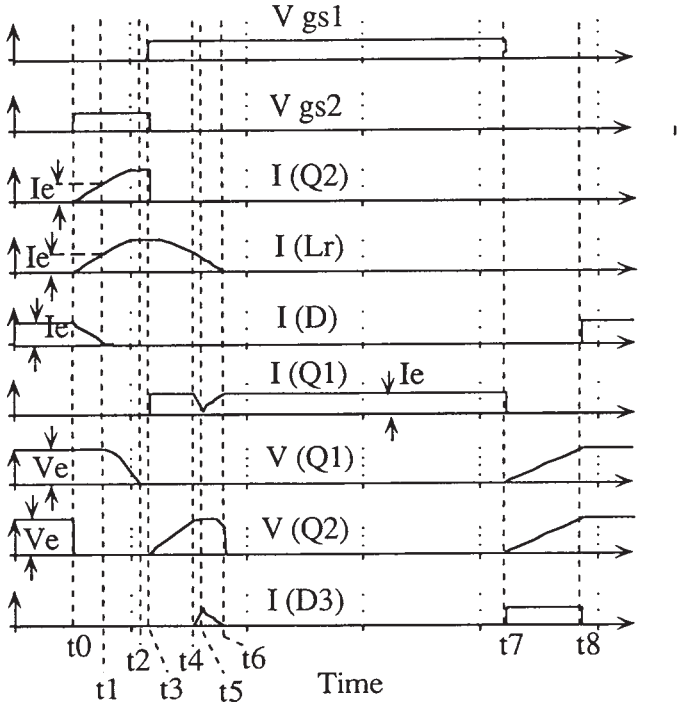

Figure 3. Basic waveforms of the proposed AASS when operating in M2 mode. See Fig. 1 for notation.

and the corresponding diode current decreases:

$$i_D = I_e - i_{Q_2} = I_e - \frac{V_e}{L_r}(t - t_o) \tag{2}$$

This interval ends at t_1 when $i_D = 0$ (D turns off). At this instant $i_{Q_2} = I_e$. The duration of the interval $t_o - t_1$ is found from (2)

$$t_{o-1} = t_1 - t_o = \frac{I_e L_r}{V_e} \tag{3}$$

(3) Interval $t_1 - t_2$. The auxiliary transistor Q_2 is 'on' and the main transistor Q_1 and the diode D are 'off'. The current $i_{Q_2} = i_r$ continues to increase, but its increase is now sinusoidal:

$$i_{Q_2} = i_r = I_e + \frac{V_e}{\left(\frac{L_r}{C_1 + C_2}\right)^{1/2}} \sin\left[\omega'(t - t_1)\right] \tag{4}$$

where

$$\omega' = \frac{1}{(L_r(C_1 + C_2))^{1/2}} \tag{5}$$

The capacitor C_1 discharges and the capacitor C_2 charges under the action of the current $i_r - I_e$

$$\left.\begin{aligned} v_{C_1} &= V_e \cos[\omega'(t - t_1)] \\ v_{C_2} &= V_e\{1 - \cos[\omega'(t - t_1)]\} \end{aligned}\right\} \tag{6}$$

This interval ends at t_2 when the voltage v_{C_1} changes its polarity and the parallel diode D_1 turns on. The duration of the interval $t_1 - t_2$ is found from (5) and (6)

$$t_{1-2} = t_2 - t_1 = \frac{\pi}{2\omega'} = \frac{\pi}{2}(L_r(C_1 + C_2))^{1/2} \tag{7}$$

The current $i_{Q_2} = i_r$ has a maximum value at t_2

$$I_{rm} = I_e + \frac{V_e}{\left(\dfrac{L_r}{C_1 + C_2}\right)^{1/2}} \tag{8}$$

(4) Interval $t_2 - t_3$. The inductor L_r is shorted through the auxiliary transistor Q_2 and diode D_1 (they are 'on'). In the ideal case, when the circuit's resistance is zero, the currents of the inductor L_r and the diode D_1 will be constant

$$i_{Q_2} = i_r = I_{rm} = I_e + \frac{V_e}{\left(\dfrac{L_r}{C_1 + C_2}\right)^{1/2}} \tag{9}$$

$$i_{D_1} = i_r - I_e = \frac{V_e}{\left(\dfrac{L_r}{C_1 + C_2}\right)^{1/2}} \tag{10}$$

The gate voltage must be delivered to the main transistor Q_1 any time within the interval $t_2 - t_3$. This interval is terminated at t_3 when Q_2 turns off. As a result, the conduction of diode D_1 ceases instantly and the conduction of the main transistor Q_1 commences. That is, the currents of D_1 and Q_1 change in stepwise manner. Diode D_2 also turns on in the same instance.

(5) Interval $t_3 - t_4$. Two independent circuits are activated. The first one includes the current source I_e shorted by the turned on transistor Q_1. The second circuit includes the inductor L_r, diode D_2 and the 'Flying' capacitor C_3. The current of the latter decreases sinusoidally

$$i_r = i_{D_2} = i_{C_3} = I_{rm} \cos[\omega''(t - t_3)] \tag{11}$$

where

$$\omega'' = \frac{1}{(L_r C_3)^{1/2}} \tag{12}$$

The voltage on the 'flying' capacitor follows the function

$$v_{C_3} = I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} \sin \omega''(t - t_3)] \tag{13}$$

The voltage of C_3 may or may not reach V_e. This will depend on the amount of energy stored in L_r. The waveforms in the following time intervals will therefore depend on the mode of operation.

Mode 1 (Fig. 2). In this mode the energy stored in the resonant inductor L_r during the intervals $t_0 - t_1$ and $t_1 - t_2$ is lower than required to charge C_3 to V_e

$$\frac{L_r I_{rm}^2}{2} < \frac{C_3 V_e^2}{2} \tag{14}$$

and therefore

$$I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} < V_e \tag{15}$$

The interval $t_3 - t_4$ is terminated when all the energy stored in L_r transferred to the 'Flying' capacitor C_3. At t_4

$$(i_r)_{t_4} = (i_{D_2})_{t_4} = I_{rm}\cos[\omega''(t_4 - t_3)] = 0 \tag{16}$$

and diode D_2 turns off. The duration of the interval $t_3 - t_4$

$$(t_{3-4})_{M1} = t_4 - t_3 = \frac{\pi}{2\omega''} = \frac{\pi}{2}(L_r C_3)^{1/2} \tag{17}$$

The 'Flying' capacitor voltage at t_4

$$(v_{C_3})_{t4} = I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} \tag{18}$$

(6) Interval $(t_4 - t_5)_{M1}$. The main transistor Q_1 is 'on', it shorts the current source I_e. The voltage across the capacitor C_2 is V_e and across the capacitor C_3 is $(v_{C_3})_{t4}$. This interval is terminated at t_5 when Q_1 is turned off.

(7) Interval $(t_5 - t_6)_{M1}$. Both transistors and all diodes are off. The capacitor C_1 is charged and the capacitor C_2 is discharged under the action of the current I_e

$$v_{C_1} = \frac{I_e}{C_1 + C_2}(t - t_5) \tag{19}$$

$$v_{C_2} = V_e - \frac{I_e}{C_1 + C_2}(t - t_5) \tag{20}$$

This interval terminates at t_6 when

$$v_{C_2} = v_{C_3} = I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2}$$

The voltage on the diode D_3, $v_{D_3} = v_{C_3} - v_{C_2}$, changes its polarity in this moment, turning D_3 on. Hence

$$V_e - \frac{I_e}{C_1 + C_2}(t_6 - t_5) = I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2}$$

from which the duration of the interval $t_5 - t_6$ can be derived

$$t_{5-6} = t_6 - t_5 = \left[V_e - I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2}\right]\frac{C_1 + C_2}{I_e} \tag{21}$$

(8) Interval $(t_6 - t_7)_{M1}$. Both transistors and diodes D, D_1 and D_2 are 'off' and the diode D_3 is 'on'. The capacitor C_1 is charged and the capacitors C_2 and C_3 are discharged under the action of the current I_e

$$v_{C_1} = V_e - I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} + \frac{I_e}{C_1 + C_2 + C_3}(t - t_6) \tag{22}$$

$$v_{C_2} = v_{C_3} = I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} - \frac{I_e}{C_1 + C_2 + C_3}(t - t_6) \tag{23}$$

The capacitor currents are constant in the interval $t_6 - t_7$

$$\left.\begin{aligned} I_{C_1} &= I_e \frac{C_1}{C_1 + C_2 + C_3} \\ I_{C_2} &= I_e \frac{C_2}{C_1 + C_2 + C_3} \\ I_{C_3} &= I_e \frac{C_3}{C_1 + C_2 + C_3} \end{aligned}\right\} \tag{24}$$

This interval is terminated at t_7 when $v_{C_2} = v_{c_3} = 0$. Following t_7 the polarity of the voltage across the main diode (D) changes and D turns on. At the same moment D_3 turns off. The duration of the interval $t_6 - t_7$ is found from (23)

$$t_{6-7} = t_7 - t_6 = (C_1 + C_2 + C_3)\frac{I_{rm}}{I_e}\left(\frac{L_r}{C_3}\right)^{1/2} \tag{25}$$

The instant t_7 marks the next power delivering interval when both transistors are 'off' and the main diode D is 'on'.

Mode 2 (Fig. 3). The energy stored in the resonant inductor L_r during the intervals $t_0 - t_1$ and $t_1 - t_2$ is larger than required to charge C_3 to V_e

$$I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} > V_e \tag{26}$$

Therefore, the end of the interval $t_3 - t_4$ differs from Mode 1: at t_4 in Mode 2 $v_{C_3} = V_e$, i.e.

$$I_{rm}\left(\frac{L_r}{C_3}\right)^{1/2} \sin\left[\omega''(t_4 - t_3)\right] = V_e \tag{27}$$

Consequently, at t_4 diode D_3 turns on. The duration of the interval $t_3 - t_4$ is found from (27)

$$(t_{3-4})_{M2} = t_4 - t_3 = \frac{1}{\omega''}\sin^{-1}\left[\frac{V_e}{I_{rm}}\left(\frac{C_3}{L_r}\right)^{1/2}\right] \tag{28}$$

The inductor current at t_4

$$(i_r)_{t4} = I_{rm}\cos\left(\omega'' t_{34}\right) \tag{29}$$

(9) Interval $(t_4 - t_6)_{M2}$. The rest of the energy stored in L_r is transferred to V_e through D_2, D_3 and Q_1. The current of diode D_3 reduces the main transistor current:

$$i_{Q_1} = I_e - i_{D_3} \tag{30}$$

Consequently, the transistor current i_{Q_1} will exhibit a valley in the interval $t_4 - t_6$ (Fig. 3). This interval ends when $i_r = i_{D_2} = i_{D_3} = 0$ and the diodes D_2 and D_3 turn off. The duration of this interval can be found from an approximate equation:

$$(t_{4-6})_{M2} = t_6 - t_4 = \frac{I_{rm} L_r}{V_e} \cos(\omega'' t_{34}) \tag{31}$$

(10) Interval $(t_6 - t_7)_{M2}$. The equivalent circuit of this case is the same as that for the interval $(t_4 - t_5)_{M1}$ but in Mode 2 the voltage across the 'Flying' capacitor C_3 is V_e. The interval ends at t_7 when the main transistor Q_1 is turned off.

(11) Interval $(t_7 - t_8)_{M2}$. The equivalent circuit is the same as that for the interval $(t_6 - t_7)_{M1}$. Under action of the current I_e the capacitors charge and discharge according to

$$v_{C_1} = \frac{I_e}{C_1 + C_2 + C_3}(t - t_7) \tag{32}$$

$$v_{C_2} = v_{C_3} = V_e - \frac{I_e}{C_1 + C_2 + C_3}(t - t_7) \tag{33}$$

The interval terminates at t_8 when $v_{C_1} = V_e$ and $v_{C_2} = v_{C_3} = 0$. The instant t_8 marks the end of the cycle and the beginning of the next power delivering interval. The duration of the interval $(t_7 - t_8)_{M2}$ can be found from (32)

$$(t_7 - t_8)_{M2} = t_8 - t_7 = (C_1 + C_2 + C_3)\frac{V_e}{I_e} \tag{34}$$

The capacitor currents can be obtained from (24).

It is important to note that all transistors and diodes of the AASS operate under soft switching conditions (Table 2). In paricular, the main transistor Q_1 turns on and turns off under ZVS, the auxiliary switch Q_2 turns on at Zero Current Switching (ZCS) and turns off under ZVS. The peak voltage on both transistors and all diodes is V_e. The transistors' and diodes' current stresses are given in Table 3.

The main difference between the M1 and M2 modes is the magnitude of dv/dt of the main switch following turn off (Table 2). The slower rate found in M2 is controlled by the FC C_3 (Fig. 1). However, to obtain this benefit, the peak inductor current I_{rm} (8) must be sufficiently high. This implies that the improved ZVS of the main switch during turn off, achieved in M2, is gained at the expense of larger conduction losses in the auxiliary switch.

4. The voltage ratio

The derivation of the converter voltage ratio V_o/V_{in} is obtained by equating the magnitudes of the positive and negative volt-seconds at the terminals of the main inductor. Furthermore, by substituting the volt-seconds found across the main switch by a rectangular waveform of amplitude V_e and duration $t_{off\,e}$, one can define an equivalent duty cycle (D_e) of the converter. The effective off time is given by

State	Turn on	Turn off	Mode
Q_1	$\frac{dv}{dt}=0$	$\frac{dv}{dt}=\frac{I_e}{C_1+C_2}$	M1
		$\frac{dv}{dt}=\frac{I_e}{C_1+C_2+C_3}$	M2
Q_2	$\frac{di}{dt}=\frac{V_e}{L_r}$	$\frac{dv}{dt}=\frac{I_{rm}}{C_3}$	
D	$\frac{dv}{dt}=\frac{I_e}{C_1+C_2+C_3}$	$\frac{di}{dt}=\frac{V_e}{L_r}$ $\frac{dv}{dt}=0$	
D_1	$\frac{dv}{dt}=\frac{V_e}{[L_r(C_1+C_2)]^{1/2}}$	$\frac{dv}{dt}=0$	
D_2	$\frac{dv}{dt}=0$	$\frac{di}{dt}=\frac{I_{rm}}{[L_rC_3]^{1/2}}$	M1
		$\frac{di}{dt}=\frac{V_e}{L_r}$	M2
D_3	$\frac{dv}{dt}=\frac{I_e}{C_1+C_2}$	$\frac{dv}{dt}=0$	M1
	$\left(\frac{dv}{dt}\right)_{t_4}=\frac{I_{rm}}{C_3}\left(1-\left(\frac{V_e}{I_{rm}}\right)^2\frac{C_3}{L_r}\right)$	$\left(\frac{di}{dt}\right)_{t_6}=\frac{V_e}{L_r}$	M2
	$\left(\frac{dv}{dt}\right)_{t_7}=0$	$\left(\frac{dv}{dt}\right)_{t_8}=0$	M2

Table 2. Switching conditions of transistors and diodes of the AASS.

Transistor or diode	Current stress	Operational Mode
Q_1; D	I_e	
Q_2; D_2	I_{rm}	
D_1	$I_{rm}-I_e$	
D_3	$I_e\frac{C_3}{C_1+C_2+C_3}$	M1
	$I_{rm}\left(1-\left(\frac{V_e}{I_{rm}}\right)^2\frac{C_3}{L_r}\right)^{1/2}$	M2

Table 3. The AASS transistors and diodes current stresses.

$$t_{\text{off e}} = \frac{\int_0^{Ts} v_{Q_1}\,\mathrm{d}t}{V_e} \tag{35}$$

where T_s is the switching period.
The equivalent 'on' time of the converter is

$$t_{\text{on e}} = T_s - \frac{\int_0^{Ts} v_{Q_1}\,\mathrm{d}t}{V_e} \tag{36}$$

Applying (6), (7), (19), (21), (22), (25), (32) and (34) we get from (36)

$$(t_{\text{on e}})_{\text{M1}} = \left(1 - \frac{2}{\pi}\right) t_{1-2} + t_{2-5} + \frac{t_{5-6}}{2} + \frac{t_{5-7}}{2}\frac{I_{\text{rm}}}{V_e}\left(\frac{L_r}{C_3}\right)^{1/2} \tag{37}$$

$$(t_{\text{on e}})_{\text{M2}} = \left(1 - \frac{2}{\pi}\right) t_{1-2} + t_{2-7} + \frac{t_{7-8}}{2} \tag{38}$$

Defining the equivalent duty cycle as

$$D_e = \frac{t_{\text{on e}}}{T_s} \tag{39}$$

we can determine the voltage ratio V_o/V_{in} using well known equations.

Buck:

$$\frac{V_o}{V_{in}} = D_e \tag{40}$$

Boost:

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D_e} \tag{41}$$

Buck–boost, Cuk, Sepic, Zeta:

$$\frac{V_o}{V_{in}} = \frac{D_e}{1 - D_e} \tag{42}$$

The minimal value of the duty cycle corresponds to the case $t_{2-3} = t_{4-5} = 0$ in Mode 1 and $t_{2-3} = t_{6-7} = 0$ in Mode 2

$$(t_{\text{on e min}})_{\text{M1}} = \left(1 - \frac{2}{\pi}\right) t_{1-2} + t_{3-4} + \frac{t_{5-6}}{2} + \frac{t_{5-7}}{2}\frac{I_{\text{rm}}}{V_e}\left(\frac{L_r}{C_3}\right)^{1/2} \tag{43}$$

$$(t_{\text{on e min}})_{\text{M2}} = \left(1 - \frac{2}{\pi}\right) t_{1-2} + t_{3-4} + t_{4-6} + \frac{t_{7-8}}{2} \tag{44}$$

The maximum value of the duty cycle is reached when instant t_7 coincides with $T_s + t_o$ in M1 and when t_8 and $T_s + t_o$ merge in M2. The equivalent turn off intervals will thus be

$$(t_{\text{off e min}})_{\text{M1}} = \frac{t_{5-6}}{2} - \frac{t_{5-7}}{2}\frac{I_{\text{rm}}}{V_e}\left(\frac{L_r}{C_3}\right)^{1/2} + t_{6-7} + t_{o-1} + \frac{2}{\pi} t_{1-2} \tag{45}$$

$$(t_{\text{off e min}})_{\text{M2}} = \frac{t_{7-8}}{2} + t_{o-1} + \frac{2}{\pi} t_{1-2} \tag{46}$$

These expressions are further simplified by applying some additional assumptions:

(1) The duration of the interval t_{5-6} in Mode 1 is negligibly small.

(2) The duration of the interval t_{3-6} in Mode 2 is described by the equation

$$(t_{3-6})_{M2} = \frac{\pi}{2}(L_r C_3)^{1/2} \tag{47}$$

instead of (28) and (31).

(3) The peak voltage on the FC C_3 equals V_e in both modes.

Under these assumptions the simplified equations for both modes are

$$t_{one\,min} = \left(\frac{\pi}{2} - 1\right)(L_r(C_1 + C_2))^{1/2} + \frac{\pi}{2}(L_r C_3)^{1/2} + \frac{1}{2}(C_1 + C_2 + C_3)\frac{V_e}{I_e} \tag{48}$$

$$t_{off\,e\,min} = \frac{1}{2}(C_1 + C_2 + C_3)\frac{V_e}{I_e} + \frac{I_e L_r}{V_e} + (L_r(C_1 + C_2))^{1/2} \tag{49}$$

5. Experimental details

The AASS soft switching scheme analysed in this study was tested experimentally on a boost converter (Fig. 4). The experimental circuit included a saturable reactor L_s in series with the resonant inductor L_r and a resistor R_s connected in parallel to the saturable reactor L_s. These elements damp the parasitic oscillations caused by the reverse recovery of D_2 and D_3, reduce the reverse recovery time and the reverse recovery losses (Hachamov and Ben-Yaakov 1995). Also included was an extra diode D_4 connected in series with the auxiliary transistor Q_2 (Fig. 4) to block its slow body-diode from conduction and to reduce the parasitic capacitance seen by the resonant network.

The experimental converter incorporated a novel driver (Fig. 5) which improves the overall efficiency by reducing to minimum the 'on' time of the auxiliary switch. The driver operation is controlled by two logic gates (A1, A2) and a digital delay.

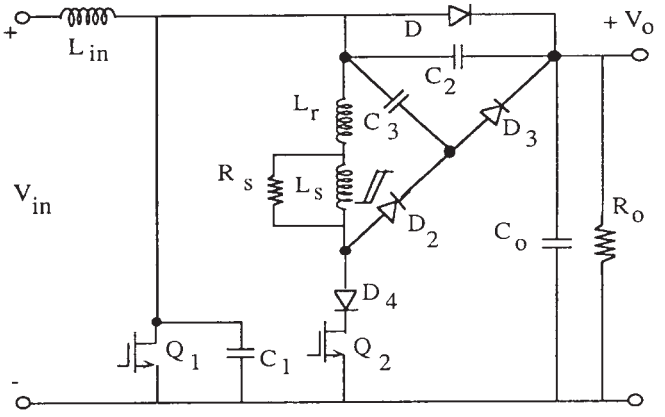

Figure 4. Experimental boost converter: $L_{in} = 0{\cdot}35$ mH; $L_r = 14{\cdot}4\,\mu$H; $C_1 + C_2 = 1{\cdot}6$ nF; $C_3 = 6{\cdot}5$ nF; Q_1 =IRFP460; Q_2 =IRFP460; D=MUR860; D_2 =MUR860; D_3 =MUR460; D_4 =MUR860.

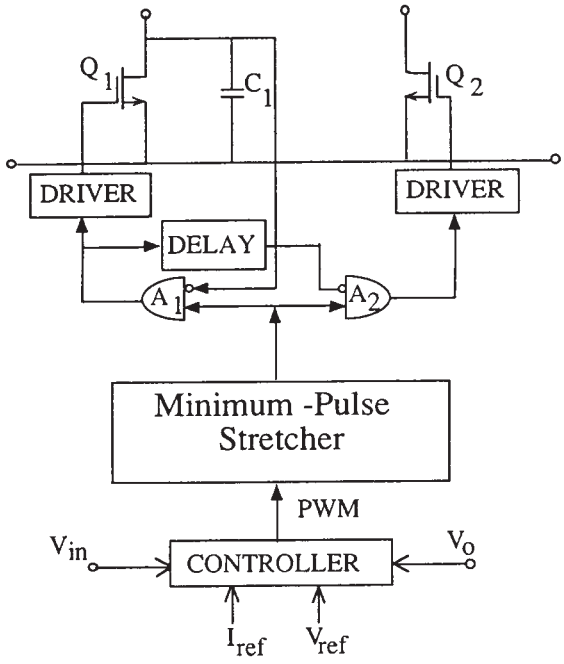

Figure 5. Basic configuration of the experimental driver.

Gate A2 produces the drive to the auxiliary switch being in the 'off' state. Gate A1 produces the drive to the main switch conditioned on the voltage across it being below a predetermined (low) value. The function of the delay is to avoid racing. That is, to give the circuit ample time to secure the turn 'on' of the main switch before the auxiliary switch is turned 'off'. In the present experimental circuit the inherent delays of the gate were sufficient and there was no need for an extra delay. The experimental system also included additional housekeeping protection circuits. Among these was a 'minimum pulse stretcher' which ensures that the pulse delivered to the driver is never shorter than the time required for the resonance inductor to discharge. Without this protection the current of the resonant inductor may build up to dangerous levels.

The parameters of the experimental converter were as follows: input voltage 130 V, output voltage 380 V, output power 1·1 kW, switching frequency $f_s = 100 \ldots 160$ kHz. The efficiency was measured to be 95·9% at $f_s = 100$ kHz and 94·1% at $f_s = 160$ kHz.

The experimental waveforms of the resonant inductor current i_r and the auxiliary switch voltage v_{Q_2} (Fig. 6) confirm that the auxiliary switch Q_2 is turned on under ZCS and is turned off under ZVS.

6. Design guidelines

Consider the basic data of the converter: the nominal value of the equivalent voltage (V_e), the highest and lowest values of the equivalent current ($I_{e\ high}$, $I_{e\ low}$), the maximal and minimal values of the voltage ratio ($(V_o/V_{in})_{max}$ and $(V_o/V_{in})_{min}$). Since the 'on' time of Q_2 (t_{Q_2}) is the limiting factor of the maximum f_s possible, we begin by specifying this parameter.

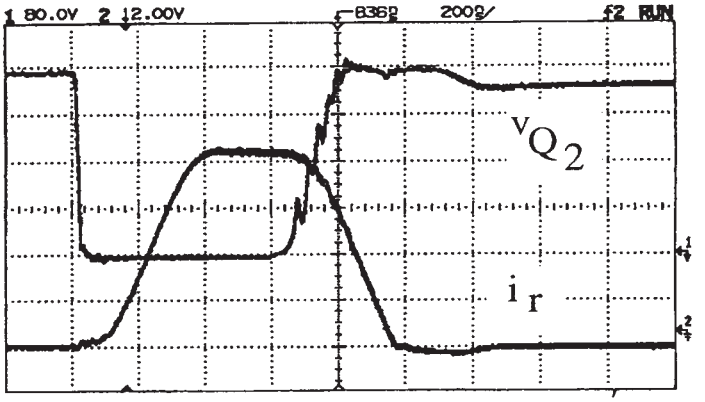

Figure 6. Typical waveforms of the experimental converter. See Fig. 1 for notation. Vertical scale: 80 V div^{-1} and 2 A div^{-1}. Horizontal scale: 200 nS div^{-1}.

Step 1. Determine the conduction interval of the auxiliary switch t_{Q_2}. Currently (mid-1995) commercially available power MOSFETS, driven by a high current driver, t_{Q_2} in the range 0·2 to 0·3 μS are practical.

Step 2. Set the current stress coefficient

$$b = \frac{I_{\text{rm}}}{I_{\text{e}}} \tag{50}$$

corresponding to the highest equivalent current $I_{\text{e high}}$.

Step 3. Calculate the resonant network's parameters L_{r} and $C_1 + C_2$ as a function of t_{Q_2} and b by applying the following condition for the highest value of the equivalent current ($I_{\text{e high}}$)

$$t_{Q_2} = (t_{0-1} + t_{1-2})_{I_{\text{e high}}} \tag{51}$$

From (3), (7), (8) and (51) we get

$$L_{\text{r}} = \frac{1}{1 + \frac{\pi}{2}(b-1)} \frac{V_{\text{e}}}{I_{\text{e high}}} t_{Q_2} \tag{52}$$

$$C_1 + C_2 = \frac{(b-1)^2}{1 + \frac{\pi}{2}(b-1)} \frac{I_{\text{e high}}}{V_{\text{e}}} t_{Q_2} \tag{53}$$

Step 4. Choose C_3 by considering the $\text{d}v/\text{d}t$ of the switches (see the expressions in Table 2). The converter will operate in Mode 2 down to some minimum I_{e}. From (26) and (8) we find that M2 prevails as long as

$$\frac{I_{\text{rm low}} \left(\frac{L_{\text{r}}}{C_3}\right)^{1/2}}{V_{\text{e}}} \geq 1 \tag{54}$$

where

$$I_{\text{rm low}} = I_{\text{e low}} + \frac{V_{\text{e}}}{\left(\frac{L_{\text{r}}}{C_1 + C_2}\right)^{1/2}} \tag{55}$$

Step 5 Apply (48) and (49) to calculate the minimal value of the equivalent turn on interval of the main switch $t_{\text{on e min}}$ and minimum values of the equivalent turn off interval of $t_{\text{off e min}}$.

Step 6. Calculate the minimal and maximal values of the duty cylce $D_{\text{e min}}$ and $D_{\text{e max}}$, using (40), (41) or (42).

Step 7. Calculate the switching frequency

$$f_{\text{s}} = \frac{D_{\text{e min}}}{t_{\text{on e min}}}$$

Step 8. Calculate the minimum value of the equivalent turn off interval of the main switch $t_{\text{off e min}}$ which corresponds to f_{s} and $D_{\text{e max}}$

$$t_{\text{off e min}} = \frac{1 - D_{\text{e max}}}{f_{\text{s}}}$$

Compare this result with the values $t_{\text{off e min}}$ of Step 5. If the values of Step 5 are higher, return to Step 4 and choose lower C_3 or return to Step 7 and choose lower switching frequency f_{s}.

Step 9. Calculate switching conditions of transistors and diodes using Table 2 and the current stresses using Table 3.

7. Conclusions

The AASS topology analysed in detail in this study, seems to be an optimal soft switcher in the sense that it does not impose voltage and current stresses that are appreciably higher than those of the corresponding hard switched PWM topology. But yet, it ensures soft switching of all power devices. This helps to reduce switching losses at high switching frequency and to reduce electromagnetic interference.

The results of this study can be equally applied to the design of other types of soft switched PWM converters.

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