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SHORT PAPER

Design and Analysis of Output Voltage Regulation in Multi-Phase Switched Capacitor Converters

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Abstract A new regulation method based on duty cycle control of the average currents in the multi-phase switched capacitor converters (SCC) is proposed, analyzed, and verified experimentally for the no effective charging case, also known as the fast switching limit. The regulation is accomplished by adjusting the value of the SCC equivalent resistance. To this end, the time slots allotted to each of the SCC topologies are adjusted, while the total switching period is kept constant. The time slots are represented by master and slave duty cycles. By this, the SCC output voltage is expressed analytically as a function of the master duty cycle. In a similar way, analytical expressions for the voltages across the flying capacitors and for the average currents in each of the topologies can be obtained. Excellent agreement was found between the theoretical and experimental results.

Keywords Duty cycle control · Efficiency · Sensitivity · Switched capacitor converter

1 Introduction

Switched capacitor converters (denoted hereinafter as SCC for singular and plural) have inherent losses that make their use prohibitive in many applications. Still, SCC are preferred in some cases due to their IC compatibility, relatively small size, and the lack of magnetic elements. It is well known that the SCC exhibit high efficiency only

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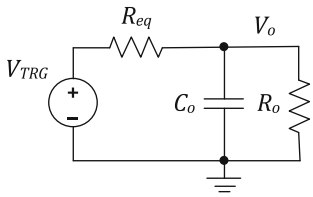


Fig. 1 The equivalent circuit of SCC

when their output voltage V_o is close to the target voltage $V_{\mathrm{TRG}} = M \cdot V_{\mathrm{in}}$, where M is the no-load conversion ratio. However, the efficiency, which can be expressed as $\eta = V_{\mathrm{o}}/V_{\mathrm{TRG}}$, decreases when the SCC are loaded, since the output voltage is less than the target voltage [1,4]. This efficiency drop is due to the SCC inherent losses, which can be modeled by an equivalent circuit that includes the target voltage source and a single equivalent resistance R_{eq} as shown in Fig. 1.

For the two-phase SCC, the regulation by duty cycle control was considered in numerous papers, for example [6,10]. The objective of this study is to develop a simple regulation method for the multi-phase SCC.

2 The Multi-Phase SCC and Regulation Method

The proposed regulation method is demonstrated by considering the binary multi-phase SCC [2,8] with a conversion ratio M=3/8. In normal operation, the switches commutate the capacitors C_j according to the topologies of Fig. 2 with equal time slots t_i for each topology i. All the parasitic resistances in the actual circuit, namely $R_{\mathrm{ds(on)}}$ of the switches and ESR of the flying capacitors are modeled by the total resistors $R_1 \ldots R_4$.

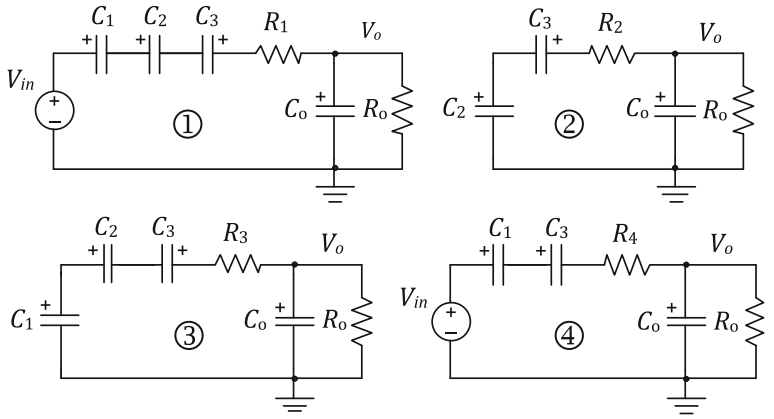


Fig. 2 Topologies of the SCC with the conversion ratio M =3/8

Once topology i is configured, an equivalent capacitor C_i=1/$\sum$(1/C_j) starts to charge or discharge. As evident from Fig. 2, each topology is a second-order circuit, where the state variables are a sum of two exponents. However, under the assumption

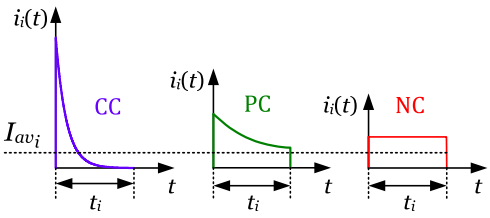


Fig. 3 Possible forms of the current through the equivalent capacitor C_i in topology i

that C_o is very large, and its ESR is negligibly small, the current through C_i is approximated well by a single exponent [4]. Let us denote this current by $i_i(t) = I_{0i}e^{-t/\tau i}$, where I_{0i} is the initial current, and $\tau_i = R_i C_i$. Depending on the ratio t_i/τ_i, the current $i_i(t)$ can take one of three possible waveforms shown in Fig. 3. The charging of C_i is practically completed if $t_i \geq 5\ \tau_i$ and this case is denoted by CC. In the case, when $t_i \approx \tau_i$, the charging is partial (PC), and if $t_i \ll \tau_i$, there is no effective charging (NC), such that during t_i the current through C_i is almost constant.

The current I_{avi} depicted in Fig. 3 is averaged over the switching period. Considering it as a common reference, one can conclude that the RMS of $i_i(t)$ will be minimal in the NC mode, and consequently, the efficiency of SCC operating in this mode is maximal [1,4]. Furthermore, in this case, the SCC output voltage is the most sensitive to the changes of duty cycle as compared to the CC and PC cases.

Based on the above, the NC mode was adopted in this study. Note that if the ESR of C_o cannot be neglected, in the NC mode, we can simply include it into all the total resistors $R_1 \ldots R_4$. This is because the flying capacitors are always charge/discharge in series with a very large C_o. Thus, the ESR of C_o increases the losses and, in case of heavy load, can lead to a considerable increase of the output voltage ripple.

Similarly to the regulation methods presented in [6,10] for the two-phase SCC, the proposed method is based on duty cycle control. To achieve regulation in the multiphase SCC, the time slots t_i could be varied, whereas the total switching period needs to be kept constant. By this, the value of SCC equivalent resistance is adjusted to regulate the output voltage.

3 Derivation of Model

The topologies of Fig. 2 are synthesized using the extended binary (EXB) representation [2,8], which in the case of $M = 3/8$ yields a set of the coefficients $a_{i,j}$ given in Table 1. These coefficients represent the connection polarity of the capacitors C_j (-1 implies that C_j is charging, 1 implies that it is discharging, and 0 implies that C_j is not connected). The values of $a_{i,0}$ are restricted to be either 1 or 0 depending whether V_{in} is connected or not, while $a_{i,4}$ is equal to -1 for all i, since C_o is always charging.

Since the topologies of Fig. 2 are denoted by the index i, and the flying capacitors by the index j, we can use the coefficients $a_{i,j}$ of Table 1 to compose the KVL equations for each topology under steady-state condition:

$$\sum_{j=1}^{3} a_{i,j} V_j - k_i I_i R_i + a_{i,4} V_o = -a_{i,0} V_{\text{in}} \tag{1}$$

Table 1 Set of the coefficients $a_{i,j}$ for M=3/8

ji	$a_{i,0}$	$a_{i,1}$	$a_{i,2}$	$a_{i,3}$	$a_{i,4}$
$a_{1,j}$	1	–1	–1	1	–1
$a_{2,j}$	0	0	1	1	–1
$a_{3,j}$	0	1	–1	1	–1
$a_{4,j}$	1	–1	0	–1	–1

where V_j is the voltages across C_j, and I_i is the currents in each of the topologies averaged over the total switching period T_s. The factors $k_i = T_s/t_i$ scale up I_i to the value of the actual current flowing during t_i.

Under steady-state condition, the sum of the I_i through each capacitor C_j (j≤3) should be equal to zero, while the sum of the I_i through the output capacitor C_o (j=4) is equal to the output current $I_\mathrm{o} = V_\mathrm{o}/R_\mathrm{o}$.

$$\sum_{i=1}^{4} a_{i,j} I_i = 0 \quad \text{and} \sum_{i=1}^{4} a_{i,4} I_i = \frac{1}{R_\mathrm{o}} V_\mathrm{o} \tag{2}$$

Equation (2) can be obtained as the vector product of the columns j=1…4 of Table 1 and the vector of currents I_i. Summarizing (1) and (2) in a matrix form we get:

$$\left(\begin{array}{cccc|cccc} -1 & -1 & 1 & -1 & -k_1R_1 & 0 & 0 & 0 \\ 0 & 1 & 1 & -1 & 0 & -k_2R_2 & 0 & 0 \\ 1 & -1 & 1 & -1 & 0 & 0 & -k_3R_3 & 0 \\ -1 & 0 & -1 & -1 & 0 & 0 & 0 & -k_4R_4 \\ \hline 0 & 0 & 0 & 0 & -1 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & -1 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & -1 \\ 0 & 0 & 0 & \frac{1}{R_o} & -1 & -1 & -1 & -1 \end{array}\right) \times \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_o \\ \hline I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{pmatrix} -V_{in} \\ 0 \\ 0 \\ -V_{in} \\ \hline 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{3}$$

Designate the number of unknowns in (3) by $2m$, such that all the sub-matrices will be of size $m \times m$. Thus, the system of Eq. (3) can be extended to the general case and written concisely as:

$$\left(\begin{array}{c|c} \mathbf{A} & \mathbf{kR} \\ \hline \mathbf{G}_o & \mathbf{A}^T \end{array}\right) \times \begin{pmatrix} \mathbf{V} \\ \hline \mathbf{I} \end{pmatrix} = \begin{pmatrix} \mathbf{V}_{in} \\ \hline \mathbf{0} \end{pmatrix} \tag{4}$$

where $\mathbf{A}$ is the incidence matrix (Table 1, without the first column); $\mathbf{kR}$ is the diagonal matrix comprising -$k_i R_i$; $\mathbf{G}_\mathrm{o}$ is the matrix where all the coefficients, except for $g_{m,m}$=1/R_o are zeros; $\mathbf{V}$ and $\mathbf{I}$ are the column vectors of the unknown voltages and currents, respectively; $\mathbf{V}_{in}$ is a column vector consisting of -V_in and zeros.

Solving (3) for the case of $R_i = R$, we find the conversion ratio $V_\mathrm{o}/V_\mathrm{in}$ as a function of the coefficients k_i and the normalized resistor $p = R_\mathrm{o}/R$:

$$\frac{V_\mathrm{o}}{V_\mathrm{in}} = \frac{3}{8 + \frac{k_1+4k_2+9k_3+16k_4}{8p}} \tag{5}$$

Since $k_i = T_s/t_i = 1/D_i$, the output to input voltage ratio can be expressed as a function of the partial duty cycles D_i:

$$\frac{V_o}{V_{in}} = \frac{3}{8 + \frac{1\frac{1}{D_1} + 4\frac{1}{D_2} + 9\frac{1}{D_3} + 16\frac{1}{D_4}}{8p}}; \quad \sum_{i=1}^{4} D_i = 1 \tag{6}$$

Expression (6) clearly shows that the output voltage can be regulated by controlling the partial duty cycles. This is on par with the results of [4] that evaluated the effect of the duty cycle on the SCC conduction losses. It was also shown in [4] that if the SCC operate in the NC mode, its output voltage is most sensitive to changes of duty cycle. Therefore, this mode was chosen in the present study. One of the simplest regulation strategies is to define one topology as the pivoting and select its duty cycle as the master duty cycle D. The control algorithm can further be simplified by making all the "slave" duty cycles equal. Namely, for a SCC with m topologies:

$$D_i|_{i \neq \text{master}} = \frac{1 - D}{m - 1} \tag{7}$$

It would be desirable that the selected master duty cycle will produce smooth regulation over the required range. In the case of the binary SCC, the required range is the incremental resolution of the converter. That is, the deviation between one target voltage to the lower next. For the M=3/8 case, deviation of interest will be the range from M=3/8 to M=2/8. To test the sensitivity issue, one can express the output to input voltage ratio for the four possible master duty cycles (8) and plot the responses (Fig. 4).

$$\begin{aligned}
\left.\frac{V_o}{V_{in}}\right|_{D=D_1} &= 3(1-D)/\left[8(1-D) + \frac{1+86D}{8Dp}\right] \\
\left.\frac{V_o}{V_{in}}\right|_{D=D_2} &= 3(1-D)/\left[8(1-D) + \frac{2+37D}{4Dp}\right] \\
\left.\frac{V_o}{V_{in}}\right|_{D=D_3} &= 3(1-D)/\left[8(1-D) + \frac{9+54D}{8Dp}\right] \\
\left.\frac{V_o}{V_{in}}\right|_{D=D_4} &= 3(1-D)/\left[8(1-D) + \frac{8+13D}{4Dp}\right]
\end{aligned} \tag{8}$$

The graphs of Fig. 4 suggest that a good choice for the master duty cycle would be $D = D_1$, since it yields a smooth and moderate regulation curve even below the level of M=2/8 (1/4) conversion ratio.

For any selected master duty cycle, the voltages across the flying capacitors will also be affected by the value of this master control variable. The expressions for the capacitors' voltages normalized to the input voltage are given by (9), where $D = D_1$.

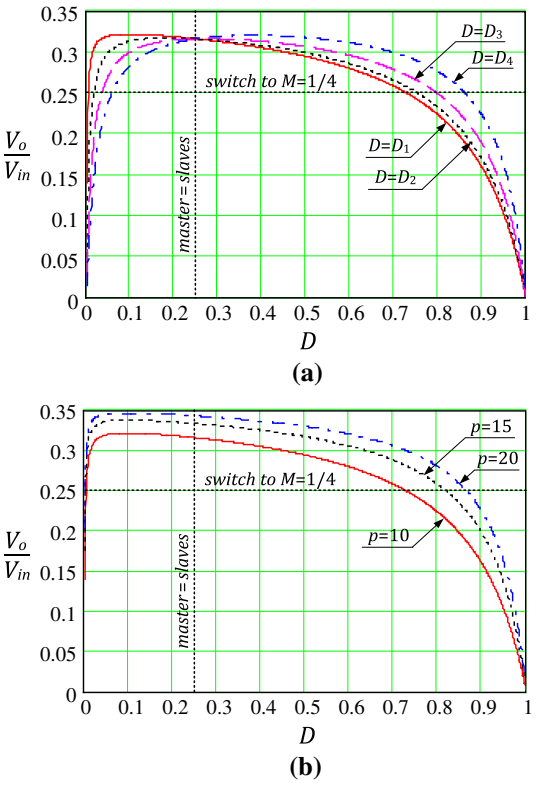


Fig. 4 The regulation characteristics (8) for different D, p=10 (a) and for different p, $D = D_1$ (b)

$$\frac{V_1}{V_{\text{in}}} = \left[4(1-D) + \frac{2+55D}{8Dp}\right] \Big/ \left[8(1-D) + \frac{1+86D}{8Dp}\right]$$
$$\frac{V_2}{V_{\text{in}}} = \left[2(1-D) + \frac{1+23D}{8Dp}\right] \Big/ \left[8(1-D) + \frac{1+86D}{8Dp}\right]$$
$$\frac{V_3}{V_{\text{in}}} = \left[(1-D) - \frac{1+5D}{8Dp}\right] \Big/ \left[8(1-D) + \frac{1+86D}{8Dp}\right] \tag{9}$$

It is evident from (8) and (9) that for high value of p(very low losses), the output voltage will converge asymptotically to V_{TRG}=(3/8)V_{in}, while the voltages across the flying capacitors become binary weighted [2,8].

From the point of view of the SCC equivalent circuit (Fig. 1) any regulation method can be considered as an adjustment of R_{eq}, and, therefore, the regulation characteristics are dependent of R_{o} as:

$$\frac{V_{\text{o}}}{V_{\text{in}}} = M\left(\frac{R_{\text{o}}}{R_{\text{eq}} + R_{\text{o}}}\right) \tag{10}$$

Thus, to regulate the output voltage at very light loads (large R_{o}), one needs very large value of R_{eq}. It can be obtained by the pulse-frequency modulation (PFM) also

known as the burst mode operation [7]. However, this method suffers from tones in the frequency spectrum, which are difficult to filter. As a result, the circuit connected to the SCC is susceptible to noise. To decrease the level of noise, one can spread the tones over a wide range as it is done in [9] by a delta-sigma loop. Another way to obtain very large values of R_{eq} is to use the current-mode control [3,5]. The switching frequency in this approach is constant, and, therefore, can be easily filtered. However, in comparison with PFM, the current-mode control requires more analog components.

Since in the proposed method, the minimal value of R_{eq} is defined by the on-resistances of the switches, and it is intended for heavy loads. Another regulation method suited well for heavy loads is the conventional frequency control. Let us compare between these two methods. For M=3/8, the analytic expression of R_{eq} was derived early in [8]:

$$R_{\mathrm{eq}} = \frac{1}{32 f_s C}\left[7\coth(\beta) + 3\coth\left(\frac{3\beta}{2}\right)\right] \tag{11}$$

where $\beta = 1/(4 f_s RC)$, R is a total resistance in the charge/discharge circuit, and C is the capacitance of single flying capacitor. The parameters for β in (11) are chosen to be as in the experimental setup, namely $R = (4 \cdot 1.2 + 470)\Omega$ and C=4.7 μF. Now, we substitute (11) into (10) and set R_o=pR. The regulation characteristics (10) as function of f_s are built in Fig. 5 for the same p=10, 15, 20.

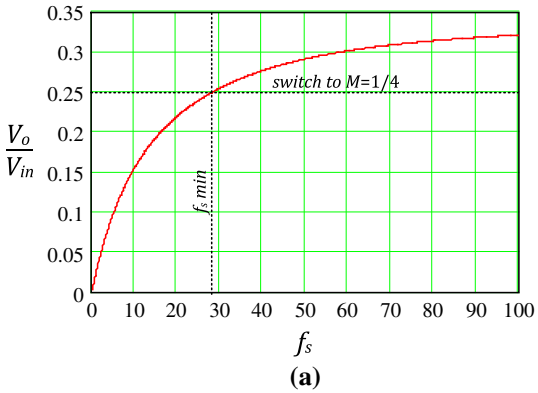
Although the curve in Fig. 5 behaves like the curve in Fig. 4, it is less sensitive to p, and, therefore, the frequency control is also effective at light loads. However, to reach the full regulation in the range of interest ($M > 1/4$) with the frequency control, we need to reduce f_s by 100/28≈3.57 times. Such a wide range of frequency adjustment means higher electromagnetic interferences (EMI), which is prohibitive in some applications. Thus, the main advantage of the proposed method is the constant switching frequency.

4 Experimental Results

The experimental setup used to realize the topologies of Fig. 2 is depicted schematically in Fig. 6. It was built around the CMOS switches MAX4678 with a $R_{ds(on)}$=1.2Ω, which were controlled by a microcontroller dsPIC33FJ12GP202, while $C_1 = C_2 = C_3$=4.7 μF , C_{o}=470 μF ,R_{o}=4.7$k\Omega$, f_s=5.556kHz, and V_{in}=8V. Such the low value of f_s is dictated by that the used microcontroller has no special means to provide high-speed multi-channel PWM for 12 switches. To provide the NC operation at the given f_s, an external resistor R=470Ω was connected in series with C_3. All experiments were carried out for $D = D_1$ and p=10.

The currents $k_i I_i$ measured as the voltage drop across R are depicted in Fig. 7, while the theoretically predicted by (8) and the experimental regulation characteristics are presented in Fig. 8 by solid and dashed lines, respectively.

The behavior of the voltages across the flying capacitors is depicted in Fig. 9, where the solid lines represent the voltages calculated by (9), and the dashed lines are those verified experimentally.



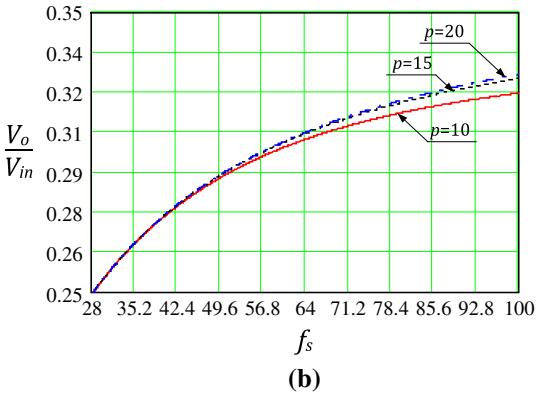


Fig. 5 The regulation characteristics (10) for p=10 (a) and for different p when $M > 1/4$ (b)

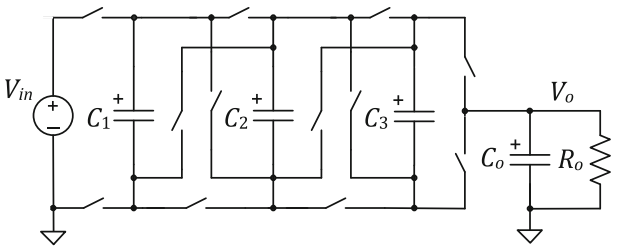


Fig. 6 The structure of the experimental setup circuit

5 Conclusions

A new analytical model was developed and applied to examine the viability of output voltage regulation by duty cycle control of multi-phase SCC operating in the NC mode. The proposed control was verified experimentally and found to achieve almost 50% variation of the output voltage. This range should suffice to provide continuous output voltage control in multi-target SCC in which the coarse control is accomplished by moving from one target voltage to another.

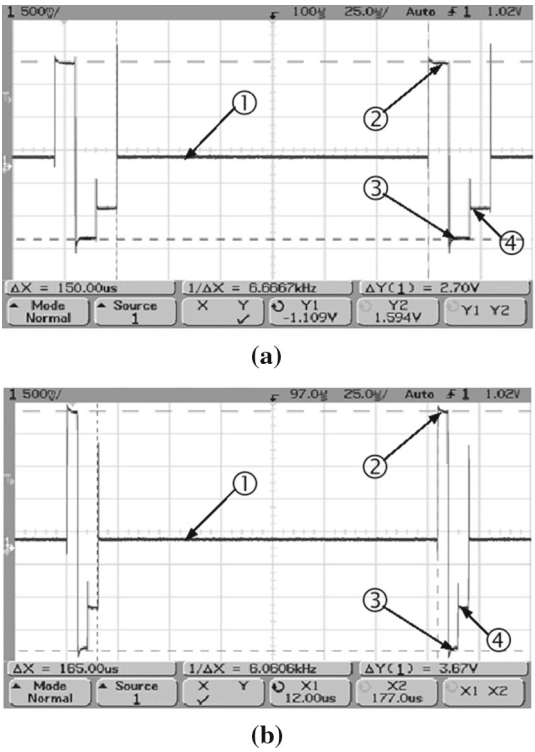


Fig. 7 The currents in all the topologies of Fig. 2 (M=3/8) for $D = D_1$=0.833 (a) and $D = D_1$=0.916 (b). The *circled numbers* correspond to the topologies of Fig. 2

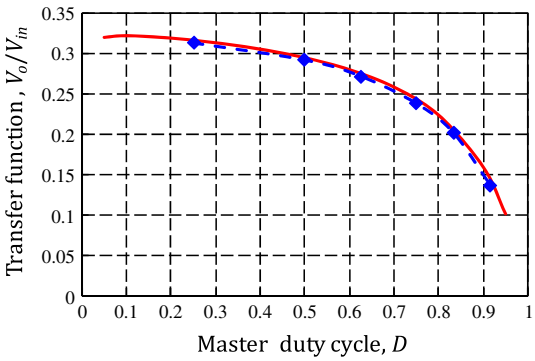


Fig. 8 The SCC regulation characteristics for M=3/8 and $D = D_1$. Solid line: model prediction. *Dashed line* experimental results

The proposed regulation method does not require any additional hardware and can be easily implemented by analog or digital controllers. Like in all SCC systems, regulation is accomplished by increasing losses, which are emulated by the SCC equivalent resistor [1,4]. In the present case, duty cycle control is used to increase the losses. This is achieved by increasing the RMS currents of the slave topologies. For example, comparing Fig. 6a with Fig. 6b, one can clearly notice that the RMS current of, say, topology 2 is higher in Fig. 6b, in which the master duty cycle is higher

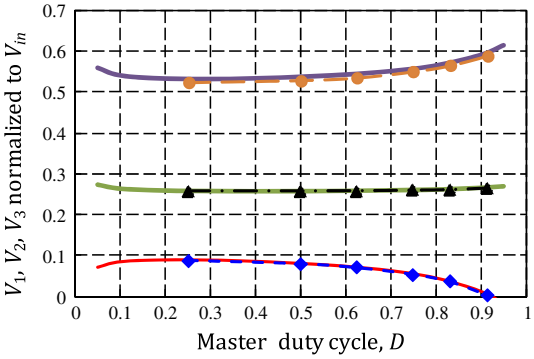


Fig. 9 The voltages across C_1, C_2, C_3 normalized to V_{in} for M=3/8 and $D = D_1$. Solid line: model prediction; Dashed line: experimental results

(D=0.916) as compared to the case of Fig. 6a (D=0.833). However, the regulation characteristics (8) are not only a function of the master duty cycle D but also depend on the ratio of the load and the topologies' resistances (assumed to be equal for the sake of simplicity) $p = R_o/R$. As the load resistance R_o increases, the regulation depth in the range $0< D <1$ will decrease, reaching eventually the point at which it is insufficient (smaller than the multi-target SCC resolution). This situation is of course common in any converter, including those which are based on the switched inductor technology.

A number of control strategies can be used to resolve the problem of SCC regulation at very light loads. Clearly, any of these methods needs to increase the losses when the output current is low. One possible approach will be to reduce the switching frequency (Fig. 5), pushing thereby the topologies into the PC mode, and eventually into the CC mode, both of which have higher losses [1]. Another approach could be frequency hopping or dithering [2,8], which has the disadvantage of introducing a low frequency ripple at the output. The proposed control was verified experimentally, and the results were found to match very well the model predictions. However, due to experimental constraints, the switching frequency was limited to 5.556 kHz. At this frequency, the effect of the parasitic inductances is very small. One should be aware though that parasitic inductance may introduce a significant change in the behavior of the SCC when operated at high switching frequency as discussed and analyzed in [4].

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References

1. S. Ben-Yaakov, On the influence of switch resistances on switched capacitor converters losses. IEEE Trans. Ind. Electron. **59**(1), 638–640 (2012)
2. Ben-Yaakov S., and Kushnerov A., Algebraic foundation of self-adjusting switched capacitor converters. in *IEEE energy conversion congress and expo. (ECCE)* 2009, pp. 1582–1589
3. H. Chung, A. Ioinovici, Switched-capacitor-based DC-to-DC converter with improved input current waveform. IEEE Int. Symp. Circuits Syst. **1**(5), 541–544 (1996)
4. M. Evzelman, S. Ben-Yaakov, Average-current-based conduction losses model of switched capacitor converters. IEEE Trans. Power Electron. **28**(7), 3341–3352 (2013)

5. B.R. Gregoire, A compact switched-capacitor regulated charge pump power supply. IEEE J. Solid-State Circuits **41**(8), 1944–1953 (2006)
6. J.W. Kimball, P.T. Krein, K.R. Cahill, Modeling of capacitor impedance in switching converters. IEEE Power Electron. Lett. **3**(4), 136–140 (2005)
7. Kotowski J., McIntyre W.J., and Parry, J.P., Capacitor DC–DC converter with PFM and gain hopping, U.S. Patent 6,055,168, 25 Apr, 2000
8. Kushnerov A, High-efficiency self-adjusting switched capacitor DC–DC converter with binary resolution, M.Sc. thesis, Ben-Gurion University of the Negev, 2009, 115p
9. A. Rao, W. McIntyre, U.-K. Moon, G. Temes, Noise-shaping techniques applied to switched-capacitor voltage regulators. IEEE J. Solid-State Circuits **40**(2), 422–429 (2005)
10. G. Zhu, A. Ioinovici, Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation. IEEE Int. Symp. Circuits Systems **1**, 553–556 (1996)