Unified Algebraic Synthesis of Generalized Fibonacci Switched Capacitor Converters

Alexander Kushnerov, *Student Member*, *IEEE* and Sam Ben-Yaakov, *Fellow*, *IEEE*

Power Electronics Laboratory
Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev
P.O. Box 653, Beer-Sheva, 84105 Israel
E-mails: kushnero@ee.bgu.ac.il; sby@ee.bgu.ac.il
Website: www.ee.bgu.ac.il/~pel

***Abstract*—A unified algebraic approach to the synthesis of generalized Fibonacci Switched Capacitor Converters (SCC) has been developed. The proposed approach reduces the power losses by increasing the number of target voltages. It is shown that the binary and Fibonacci SCC are private cases of the proposed approach. Furthermore, the proposed generalized SCC is built around the same switch network as the binary and Fibonacci SCC. This feature is extremely beneficial since it provides the option to switch between the different target voltages, thereby increasing the resolution of attainable conversion ratios. In the case of three flying capacitors, six new conversion ratios were introduced in addition to the thirteen that have been realized already. The theoretical results were verified experimentally.**

I. Introduction

Switched capacitor converters (SCC), also known as charge pumps, have been found to be useful in low power applications due to their IC compatibility, relatively high efficiency and the lack of magnetic components that helps to lower the EMI. It is well known that the SCC exhibits high efficiency only when its output voltage, V_o, is very close to the target voltage, $V_{TRG}=M\cdot V_{in}$, where M is the no-load conversion ratio. The SCC efficiency can be approximated by $\eta=V_o/V_{TRG}$ and decreases when the SCC is loaded. This efficiency drop is due to the inherent power losses, which can be modeled by an equivalent circuit (Fig. 1) that includes the target voltage source, V_{TRG}, and a single equivalent resistor, R_{eq}. This resistor represents the losses due to power dissipation in switch resistances and capacitors' ESR [1], [2]. The simplified model of Fig. 1 does not take into account losses due to gate drives, leakage current and other parasitic effects which are not addressed in this work.

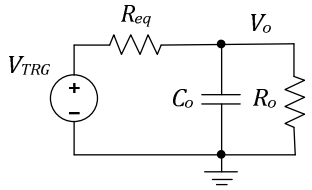

Fig. 1: The equivalent circuit of SCC

Neglecting the parasitic effects, high efficiency is obtained if R_{eq} is small. In this case, V_o will be very close to V_{TRG}. In many applications there is a need to maintain a constant output voltage under input voltage variations or to provide different output voltages for different operational modes of a system. Such a voltage control can be accomplished by adjusting R_{eq} or M or both [3]. The highest efficiency will be obtained if R_{eq} is kept as small as possible and M is changed as required. The latter, however, is a difficult problem since M depends on the SCC topologies. Attempts to introduce multiple values of M have resulted hitherto in circuits with a large number of capacitors and switches that increase the power losses. An effective way to realize many target voltages is the combination of the binary [4],[5] and Fibonacci SCC [6],[7]. The behavior of this combination is depicted by the solid line in Fig. 2 for the resolution n=1...3, while the values on the x-axis represent the attainable conversion ratios. The objective of this study was to introduce additional target voltages to the combined SCC without adding capacitors or switches. The dashed line in Fig. 2 depicts the additional efficiency peaks that are obtained by the insertion of the generalized Fibonacci target voltages, developed in this study, between their existing counterparts.

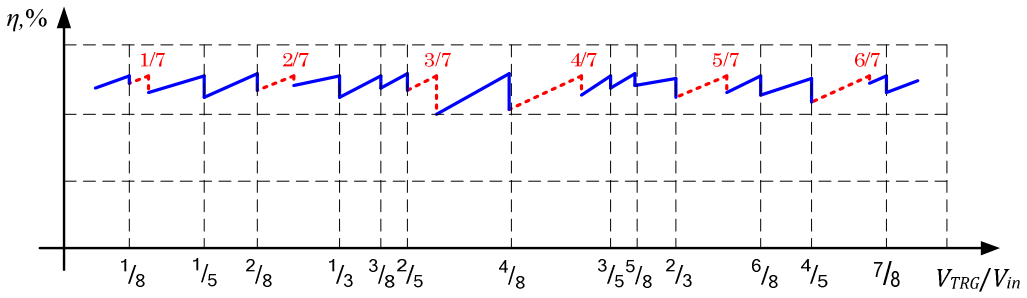

Fig. 2: The expected total efficiency

978-1-4673-0803-8/12/$31.00 ©2012 IEEE

II. Signed Generalized Fibonacci (SGF) Representation

The proposed approach to synthesis of generalized Fibonacci SCC is based on the novel number system described in this section. The generalized (h, k)-th Fibonacci numbers [8]-[10] are defined for $i \geq 2$ and $h \leq k \leq h+1$ as:

$$F_i = F_{i-1} + F_{i-k} + (k-h) \tag{1}$$

where the initial values $F_{2-k} = F_{3-k} = \ldots = F_0 = (h-k+1)$, and $F_1 = 1$. For $h \leq k \leq 3$, the first eight (h, k)-th Fibonacci numbers are given in Table I. Note, that first and third rows are the binary and regular Fibonacci numbers respectively.

TABLE I: The generalized Fibonacci numbers

h	k	Expression	1	2	3	4	5	6	7	8
1	1	$F_i=2F_{i-1}$	1	2	4	8	16	32	64	128
1	2	$F_i=F_{i-1}+F_{i-2}+1$	1	2	4	7	12	20	33	54
2	2	$F_i=F_{i-1}+F_{i-2}$	1	2	3	5	8	13	21	55
2	3	$F_i=F_{i-1}+F_{i-3}+1$	1	2	3	5	8	12	18	27
3	3	$F_i=F_{i-1}+F_{i-3}$	1	2	3	4	6	9	13	19

According to Daykin's theorem [8]-[10], any positive number $F_i \leq N_n < F_{i+1}$ can be represented uniquely as a sum of distinct (h, k)-th Fibonacci numbers:

$$N_n = \sum_{j=0}^{n} A_j F_{n-j+1} \tag{2}$$

where A_j is either 0 or 1; and n sets the resolution. Incrementing the index j, we get the largest (h, k)-th Fibonacci number, F_{n+1}, in the leftmost position, as shown in Table II for $h = 1$, $k = 2$, and n=6.

TABLE II: The (1, 2)-th Fibonacci weights for n=6

j	0	1	2	3	4	5	6
F_{n-j+1}	33	20	12	7	4	2	1

Since Daykin's theorem is, in fact, an extension of Zeckendorf's theorem [11], hereinafter the Daykin expansion is called the EZ-code. The main difference between the EZ-code and its binary counterpart is that not all combinations of "0" and "1" are permitted. Namely, two ones must be spaced with at least $k-1$ zeros, with the only exception for two rightmost ones, which can be spaced with $h-1$ zeros.

For example: if $h = 2$ and $k = 3$ then every pair of "1"s in the EZ-code is spaced with at least two "0"s, except of the rightmost pair, which is spaced with at least a single "0" and may be followed by a string of "0"s. These two permitted bit patterns are illustrated in (3).

$$0\underbrace{100}_{k-1}1\underbrace{0}_{h-1}100 \tag{3}$$

Now, we define the Signed Generalized Fibonacci (SGF) representation for fractions $M_n = N_n/F_{n+1}$ in the range (0, 1) as follows.

The expression (2) is normalized to the largest (h, k)-th Fibonacci number, F_{n+1}, and the coefficients A_j $(j \geq 1)$ are allowed to take one of the three values of 0, 1, and −1, as was done in [12]. The SGF representation also includes a leading coefficient, A_0, which could be either 0 or 1. Namely,

$$M_n = A_0 + \sum_{j=1}^{n} A_j \frac{F_{n-j+1}}{F_{n+1}} \tag{4}$$

where n sets the resolution. Due to A_j taking the extra value of −1, a number of different SGF codes can represent the same fraction M_n, for example:

$$\begin{aligned} {}^4/_7 &= 1 - 1\cdot({}^4/_7) + 0\cdot({}^2/_7) + 1\cdot({}^1/_7) \rightarrow \{1\ \text{-}1\ \ 0\ \ 1\} \\ {}^4/_7 &= 1 - 1\cdot({}^4/_7) + 1\cdot({}^2/_7) - 1\cdot({}^1/_7) \rightarrow \{1\ \text{-}1\ \ 1\ \text{-}1\} \\ {}^4/_7 &= 1 + 0\cdot({}^4/_7) - 1\cdot({}^2/_7) - 1\cdot({}^1/_7) \rightarrow \{1\ \ 0\ \text{-}1\ \text{-}1\} \end{aligned} \tag{5}$$

These different codes are obtained by the spawning rule based on the identity $2F_i = F_{i+1}+F_{i-1}-F_{i-k+1}+F_{i-k}$, which states, in fact, that the addition of two "1"s in the EZ-code induces, in the general case, four carries. The first carry goes one bit left, the second goes one bit right, while the third and the fourth go $k-1$ and k bits right respectively. Note that for k=1 the above identity is reduced to the rule of binary addition, $2F_i = F_{i+1}$, while for k=2 it is reduced to the rule of Fibonacci addition, $2F_i = F_{i+1} + F_{i-2}$.

A rule for spawning the SGF codes:

This rule is iterative and starts with the EZ-code of M_n. Skipping the zeros from the left, add "1" to the first $A_j = 1$. This will turn A_j to "0" and induce four carries. To keep the original M_n value add "−1" to the resulting $A_j = 0$ and generate thereby a new SGF code. The above procedure is repeated for all $A_j = 1$ in the original code and for all $A_j = 1$ in each new SGF code.

Corollary 1: For a resolution n, the minimum number of SGF codes for a given M_n is $n + 1$.

This is because each of the "1"s in the EZ-code with resolution n produces a new SGF code and four carries. Further iterations cause the carries to propagate, so that each "0" in the EZ-code is turned into a "1", which is also operated on to spawn a new code. Hence, the minimum number of codes is the original code plus n, that is $n+1$.

Corollary 2: Each $A_j = 1$ in either the EZ-code or spawned SGF code yields at least one $A_j = -1$ in the same position j of another SGF code.

This is because the spawning procedure involves the substitution of a "1" by a "−1".

1	${}^4/_7$	${}^2/_7$	${}^1/_7$
0	0	1	1
		+1	
0	1	0	1
		−1	
0	1	−1	1

1	${}^4/_7$	${}^2/_7$	${}^1/_7$
0	1	−1	1
	+1		
1	0	0	0
	−1		
1	−1	0	0

1	${}^4/_7$	${}^2/_7$	${}^1/_7$
0	1	−1	1
			+1
0	1	0	0
			−1
0	1	0	−1

Fig. 3: Spawning the SGF codes for M_3=3/7 from the EZ-code {0 0 1 1}.

The example in Fig. 3 shows how three different SGF codes for M_3=3/7 are spawned from the (1, 2)-th EZ-code $\{0\ 0\ 1\ 1\}$. Since $k = 2$, the reduced identity $2F_i = F_{i+1} + F_{i-2}$ is applied. Note that due to $F_0 = 0$ all the overflows beyond the LSB are disregarded. The SGF codes for other M_3, h=1, k=2 are summarized in Table III.

III. Translating the SGF Codes into SCC Topologies

The rules for translating the SGF codes into SCC topologies follow the rules given in [4]-[7] for the binary and Fibonacci SCC. Consider a step-down SCC including a voltage source, V_{in}, a set of n flying capacitors, C_j, and an output capacitor, C_o, which is paralleled to load R_o. For a given M_n the interconnections of V_{in}, C_j, and C_o are carried out according to the following rules:

1) If $A_0 = 1$ then V_{in} is connected in a polarity that charges the output.
2) If $A_0 = 0$ then V_{in} is not connected.
3) If $A_j = -1$ then C_j is connected in a charging polarity (same as the output).
4) If $A_j = 0$ then C_j is not connected.
5) If $A_j = 1$ then C_j is connected in a discharging polarity (opposite to the output).

The above rules are illustrated by translating the SGF codes of M_3=3/7 to the topologies depicted in Fig. 4.

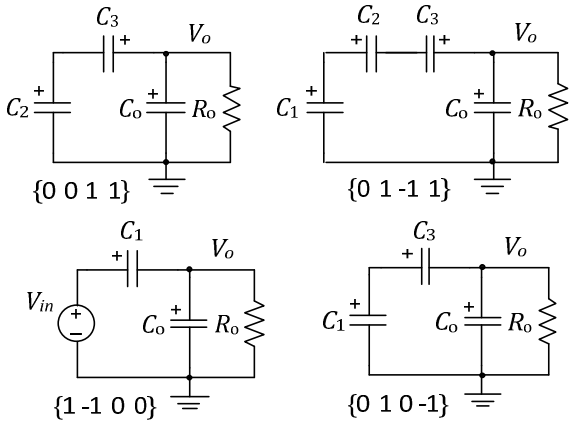

Fig. 4: The topologies of generalized step-down Fibonacci SCC with M_3=3/7.

Let us assume that under steady-state conditions all the capacitors in the topologies of Fig. 3 are charged to constant, but unknown voltages V_1, V_2, V_3, and V_o. To find these voltages we apply Kirchhoff's Voltage Law (KVL) to each topology that leads to the next system of four linear equations:

$$\begin{cases} 0\cdot V_{in} + 0\cdot V_1 + 1\cdot V_2 + 1\cdot V_3 = V_o \\ 0\cdot V_{in} + 1\cdot V_1 - 1\cdot V_2 + 1\cdot V_3 = V_o \\ 1\cdot V_{in} - 1\cdot V_1 + 0\cdot V_2 + 0\cdot V_3 = V_o \\ 0\cdot V_{in} + 1\cdot V_1 + 0\cdot V_2 - 1\cdot V_3 = V_o \end{cases} \quad (6)$$

Solving (6) we obtain the target and (1, 2)-th Fibonacci weighted voltages across the output and flying capacitors respectively: V_o=($^3/_7$)V_{in}; V_1=($^4/_7$)V_{in}; V_2=($^2/_7$)V_{in}; V_3=($^1/_7$)V_{in}. Considering the fact that (6) is solvable it should also be solvable if V_{in} and V_o are interchanged. This means switching the input and output terminals and, in fact, converting the step-down SCC to a step-up SCC as shown in Fig. 5.

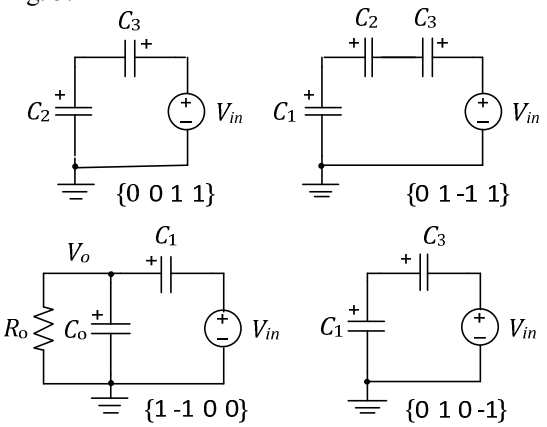

Fig. 5: The topologies of generalized step-up Fibonacci SCC with $1/M_3$=7/3.

The steady-state KVL equations for the SCC topologies of Fig. 5 are:

$$\begin{cases} 0\cdot V_o + 0\cdot V_1 + 1\cdot V_2 + 1\cdot V_3 = V_{in} \\ 0\cdot V_o + 1\cdot V_1 - 1\cdot V_2 + 1\cdot V_3 = V_{in} \\ 1\cdot V_o - 1\cdot V_1 + 0\cdot V_2 + 0\cdot V_3 = V_{in} \\ 0\cdot V_o + 1\cdot V_1 + 0\cdot V_2 - 1\cdot V_3 = V_{in} \end{cases} \quad (7)$$

The solution of such a system is: V_o=($^7/_3$)V_{in}; V_1=($^7/_4$)V_{in}; V_2=($^7/_2$)V_{in}; V_3=($^7/_1$)V_{in}. It is evident that the step-up target voltage V_o=($^7/_3$)V_{in} is reciprocal to its step-down counterpart as in the case of binary and Fibonacci SCC. Note that for n flying capacitors and $h = k = 2$, the highest conversion ratio is equal to the regular Fibonacci number F_{n+2}. This case is of practical importance if there is a need to build a specific charge pump and was reported in [6], [7].

TABLE III: The SGF codes for fractions M_3, $h = 1$, $k = 2$

M_3=1/7				M_3=2/7				M_3=3/7				M_3=4/7				M_3=5/7				M_3=6/7			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3
0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0
0	0	1	-1	0	1	-1	0	0	1	-1	1	1	-1	0	1	1	-1	1	0	1	-1	1	1
0	1	-1	-1	1	-1	-1	1	1	-1	0	0	1	-1	1	-1	1	0	-1	0	1	0	-1	1
1	-1	-1	0	1	-1	0	-1	0	1	0	-1	1	0	-1	-1	0	1	1	-1	1	0	0	-1

Thus, for the same number of the flying capacitors (n=3), we have introduced six new (1, 2)-th Fibonacci conversion ratios: $\{^1/_7, ^2/_7, ^3/_7, ^4/_7, ^5/_7, ^6/_7\}$ in addition to the thirteen $\{^1/_8, ^1/_5, ^1/_4, ^1/_3, ^3/_8, ^2/_5, ^1/_2, ^3/_5, ^5/_8, ^2/_3, ^3/_4, ^4/_5, ^7/_8\}$ of the binary and Fibonacci SCC, which should improve the efficiency as depicted in Fig. 2.

IV. Experimental Results

The experimental setup (Fig. 6) followed the same design as in [4]-[7]. It was built around the CMOS bidirectional switches MAX4678 with an on-resistance of 1.2Ω, while C_1=C_2=C_3=4.7μF, C_o=470μF, and V_{in}=8V. The time slot allotted for each topology was 5μs. The output voltage was measured for R_o=300Ω and R_o=100Ω and is presented in Fig. 7(a) by a solid and a dashed line respectively. The SCC efficiency is presented in Fig. 7(b), for R_o=300Ω (diamonds) and R_o=100Ω (squares).

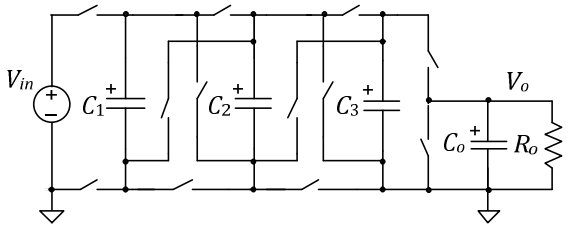

Fig. 6: The switch network used for the generalized Fibonacci SCC.

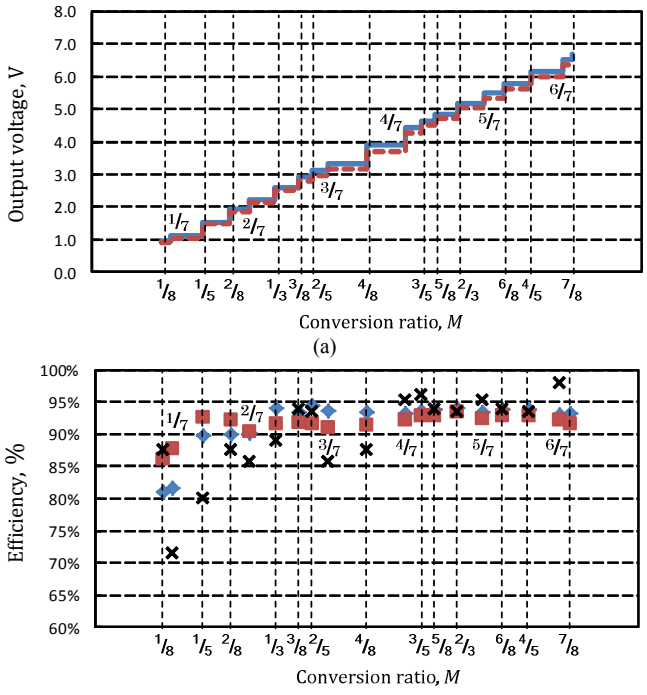

Fig. 7: The output voltage (a) and efficiency (b) of the experimental SCC. The curve of the higher output voltage in (a) is for R_o=300Ω, while the one of the lower voltage is for R_o=100Ω. The points marked by "X" in (b) are estimates of minimum efficiency of a regulated version of proposed SCC in between target voltages and the diamonds and squares are experimental results for R_o=300Ω and R_o=100Ω respectively.

As is evident from Fig 7(b), the measured efficiency is low for low conversion ratios, M_n. This could be explained by the fact that the real SCC has some constant losses, which have a larger effect at low M_n. Additional evidence for the constant losses is that for very low M_n the efficiency is lower for light loads.

V. Conclusion and Discussion

Based on Daykin's theorem, a new SGF representation has been derived and then used for algebraic synthesis of generalized Fibonacci SCC. This new class of SCC reduces the power losses by increasing the number of target voltages. It is compatible with the previously developed binary and Fibonacci SCC and is built around the same switch network. This allows one to increase the density of efficiency peaks by switching between closely spaced neighbor target voltages. The multi-target feature is beneficial in both the cases of unregulated SCC with different output voltages and regulated SCC where the output is maintained at a constant voltage while subjected to load and input voltage variations. In the considered SCC with three flying capacitors six new conversion ratios were introduced in addition to thirteen already realized. The proposed SCC can be considered as hardware that solves a system of linear equations defined by the SGF codes.

The efficiency at the target voltage will be maximal, limited by the equivalent resistor of the circuit and the parasitic losses. The experimental SCC that applied 1.2Ω switches reached above 90% efficiency for most of the target ratios. Regulation in between the target points can be obtained by duty cycle or/and frequency control, but at the expense of increased losses [1]-[3] and consequently a lower efficiency. However, considering the close proximity of the target voltages, the expected efficiency reduction is rather small. The worst case is the gain range between 1/7 and 1/5 (Fig. 7). Applying the relationship η=V_o/V_{TRG}, the minimum efficiency (just before reaching the 1/7 gain) is 71.4%. For the same gain range, the minimum efficiency of the Fibonacci SCC [6], [7] would be 62.5%. Hence, considerable improvement is obtained even at the very low conversion ratios. For higher gains the expected minimum efficiency is considerably higher as is evident from Fig. 7(b) in which the estimated minimum efficiencies in between the target points are marked by "X". It can thus be concluded that the proposed generalization of the multi-target SCC improves its performance. It is rather remarkable that this improvement is obtained at no cost since there is no need to add switches and/or capacitors to the circuit.

Acknowledgment

The first author would like to thank Dr. Moshe Schwartz for providing popular interpretation of Daykin's results. This research was supported by the Israel Science Foundation (Grants No. 476/08 and No. 517/11).

REFERENCES

[1] S. Ben-Yaakov and M. Evzelman, "Generic and unified model of switched capacitor converters," IEEE Energy Conversion Congress and Expo. (ECCE) 2009, pp.3501-3508.

[2] S. Ben-Yaakov, "On the influence of switch resistances on switched capacitor converter losses," IEEE Transactions on Industrial Electronics, Vol. 59, no.1, 2012, pp.638-640.

[3] S. Ben-Yaakov and A. Kushnerov, "Analysis and implementation of output voltage regulation in multi-phase switched capacitor converters," IEEE Energy Conversion Congress and Expo. (ECCE) 2011, pp.3350-3353.

[4] S. Ben-Yaakov and A. Kushnerov, "Algebraic foundation of self-adjusting switched capacitor converters," IEEE Energy Conversion Congress and Expo. (ECCE) 2009, pp.1582-1589.

[5] A. Kushnerov, *High-efficiency self-adjusting switched capacitor DC-DC converter with binary resolution*, M.Sc. thesis, Ben-Gurion University of the Negev, 2009, 115p.

[6] A. Kushnerov and S. Ben-Yaakov, "Algebraic synthesis of Fibonacci switched capacitor converters," IEEE Conference on Microwaves, Communications, Antennas and Electronics Systems (COMCAS) 2011, pp.1-4.

[7] A. Kushnerov and S. Ben-Yaakov, "The best of both worlds: Fibonacci and binary switched capacitor converters combined," IET Power Electronics, Machines and Drives Conference (PEMD) 2012, pp.1-5.

[8] D. E. Daykin, "Representation of natural numbers as sums of generalised Fibonacci numbers," J. London Math. Soc., 35, 1960, pp. 143-160.

[9] D. E. Daykin, "Representation of natural numbers as sums of generalized Fibonacci numbers – II," The Fibonacci Quarterly, Vol. 7, no.5, 1969, pp. 494-509.

[10] V. Laohakosol and J. Chalermchai, "Representing natural numbers as unique sums of positive integers," J. Korea Soc. Math. Edu. Ser. B: Pure Appl. Math., Vol. 11, no.1, 2004, pp. 63-72.

[11] J. L. Brown, "Zeckendorf's theorem and some applications," Fibonacci Quarterly, Vol. 2, no.3, 1964, pp.163-168.

[12] P. Ligomenides and R. Newcomb, "Multilevel Fibonacci conversion and addition," Fibonacci Quarterly, Vol. 22, no.3, 1984, pp.196-203.