Letters

On the Influence of Switch Resistances on Switched-Capacitor Converter Losses

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***Abstract*—The contribution of switch resistances to the losses in switched-capacitor converters (SCC) is reevaluated. The results reaffirm the crucial role that the switch resistances play in the design of open-loop and regulated SCC.**

***Index Terms*—Capacitor charging, losses, switch mode converters, switched-capacitor (SC) converters (SCC).**

I. Introduction

There are some indications that, despite being a seemingly trivial issue, capacitor charging is far from being fully understood. A case in point is the role of switch resistances in the efficiency of switched-capacitor (SC) converters (denoted henceforth as "SCC" for singular and plural). For example, the authors of an earlier correspondence [1], which considered the realization of line and load regulation in SC-based converters, state the following:

> "The on-resistances of the transistors and the equivalent series resistances (ESRs) of the capacitors do not influence the efficiency, in contrary to what [2] has described. The losses are not dependent upon the charging/discharging capacitor current trajectories either."

Another example is a recent publication [3] in which the authors conclude the following:

> "R in the charging circuit does not affect the charging efficiency, but R in the discharging circuit does affect the discharging efficiency."

These statements seem troublesome when applied to SCC systems since basic engineering intuition will anticipate that very large switch resistances must have an effect.

It appears that one culprit causing an uncertainty concerning the role of switch resistances in SCC is the fact that the efficiency η of an SCC can be expressed as

$$\eta = \frac{V_o}{V_T} \tag{1}$$

where V_o is the output voltage and V_T is the target voltage (the no-load voltage) which is linearly proportional to the input voltage and whose value depends on the structure of the SCC. Equation (1) neglects losses which are not associated with the charge transfer via the main SCC paths, such as leakage and drive current losses. These and other parasitic effects are ignored in this letter.

Expression (1) seems to be independent of the switch resistances which might give the impression that switch resistances do not play any role. This is probably one of the reasons that the importance of switch resistances in SCC losses is overlooked.

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II. Role of Switch Resistances in SCC Systems

The discussion to follow is based on the results of a recent study [4] in which closed-form equations were developed for the losses of hard- and soft-switched SCC operating in open loop as a function of the average currents.

It is worthwhile to first state the premises on which the explanations offered in this communication are based.

1) The losses during capacitor charging/discharging are due to the dissipative parts of the circuit while the capacitor charging process, *per se*, is theoretically lossless.
2) Comparative analysis and evaluation of losses in an SCC system require a common reference. An acceptable one would be an identical charge transfer in each subcircuit or identical output current of the SCC.
3) The open-loop SCC can be modeled as a voltage source (target voltage V_T, the no-load voltage) connected in series with an internal resistance R_e.

The first point is self-explanatory while the second point provides the yardstick for comparing losses when changing parameters (e.g., switch resistance values). The third premise is now being universally accepted and widely used by workers in the field [4]–[6].

It follows from point 3 that (1) can be written as

$$\eta = \frac{R_o}{R_e + R_o} \tag{2}$$

where R_o is the load resistance.

Equation (2) clearly shows that the SCC losses are a function of R_e which, in turn, is a function of the losses in each of the subcircuits that are formed by the switch action of the SCC. It was proven in [4] that the average power loss P_i in each hard-switched and unregulated charging/discharging subcircuit i can be expressed as a function of the SCC average output current I_o as

$$P_i = (I_o)^2 \cdot \left\{ k_i^2 \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})} \right\}, \qquad \beta_i = \frac{T_i}{R_i C_i} \tag{3}$$

where f_s is the switching frequency, C_i is the equivalent capacitance in subcircuit i, R_i is the loop resistance, T_i is the duration of switching phase i, and k_i is a constant relating the average subcircuit current to the average output current. This expression and the discussion to follow assume that the subcircuits are of first order and ignore the effect of parasitic inductances that may play a role at high switching frequencies [5], [7] as well as the dependence of capacitor ESR on frequency [5]. It should be noted that (3) is valid for both the charge and discharge processes, which is a manifestation of the fact that the generic charge/discharge equivalent circuit is identical in both cases [4].

Expression (3) is based on premise 1 and complies with the requirement for a common reference of premise 2. The common reference is the average output current I_o of the SCC. The term in brackets can be defined as the equivalent resistance R_{ei} contributed by subcircuit i

$$R_{ei} = \left\{ k_i^2 \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})} \right\}. \tag{4}$$

The total output resistance R_e of the SCC equivalent model is equal to the sum of all R_{ei}'s [4]. This is due to the fact that the losses are expressed as a function of the output current I_o. Hence, the losses of a given SCC will depend on the value of (4) for each of the subcircuits. These values depend, in turn, on the operating mode of the SCC and, in particular, on the value of β_i which will determine if the charging/discharging is completed within T_i (denoted here as the "complete charge (CC)" case), partially completed [partial charge (PC)], or will have a constant current nature with a practically constant capacitor voltage [no charge (NC)]. The asymptotic value for the NC case ($\beta \ll 1$) is

$$R_{ei}|_{\beta \ll 1} = \left\{ k_i^2 \frac{R_i}{f_s T_i} \right\}. \tag{5}$$

Additionally, for the CC case ($\beta \gg 1$)

$$R_{ei}|_{\beta \gg 1} = \left\{ k_i^2 \frac{1}{2 f_s C_i} \right\}. \tag{6}$$

The general expression (4) which is applicable to the PC case and its asymptotic limit for the NC case (5) are clearly dependent on the switch resistance. Therefore, in these operating regions, there is no question that the switch resistance will affect the efficiency. Expression (6), however, seems to point out that, in the CC case, the switch resistance is unimportant. The same resistance-independent result is obtained by an energy balance calculation, when a capacitor is charged to the full value of the charging voltage source.

In the light of the above, a reasonable question would be the following: Is the switch resistance unimportant at least in the CC case? Contrary to what has been stated in the previously cited publications, the answer is still "no." That is, the switch resistance needs to be considered even in this case. To explain this, consider the options that face a designer when choosing the size of the switches in an SCC. In the light of (6), large transistors with very low "on" resistance are wasteful because the lower resistance does not improve efficiency. In fact, very low resistances are harmful since they cause very high peak currents [7] and, hence, will induce higher electromagnetic interference. As the switch resistances increase, the system will eventually hit the point at which the subcircuits (for a given switching frequency and capacitor values) enter the PC region and the equivalent resistance will increase and so will, of course, the losses. This is shown in Fig. 1 which is a plot of the exponential part of (4) as a function of the normalized loop resistance R_i^*; $\{R_i^* = R_i/(T_i/C_i) = 1/\beta_i\}$, while all other parameters are kept constant. As evident from Fig. 1, the subcircuits' losses are indeed insensitive to switch resistances as long as they are small enough, particularly as long as the time constants ($R_i C_i$) of the subcircuits are much smaller than the switching durations T_i. However, if the switch resistance is increased beyond $R_i^* \approx 0.1$, the losses will start to increase (Fig. 1). Therefore, in fact, optimization of SCC systems must take into consideration the switch resistances in all regions. If the SCC is designed to work in the CC region, an optimal switch resistance selection will not only minimize the transistors' size but also reduce the peak charging current.

Notwithstanding the aforementioned explanation of the importance of the switch resistance, there is still an apparent "mystery" that needs to be addressed. If the losses are due to the dissipative elements (premise 1 earlier), how come (6) is independent of the resistance? As a preamble to the answer, it should be clarified that (4) and, hence, the asymptotic expression (6) were derived in [4] by **calculating the power dissipation of the resistance in the subcircuit and not by energy balance**. Hence, the disappearance of the R_i in the asymptotic limit (6) implies that the **mathematical expression** of the dissipation in this case happens to be equal to (6). That is, when calculating the power dissipated in the loop resistance in the CC case, one gets a result

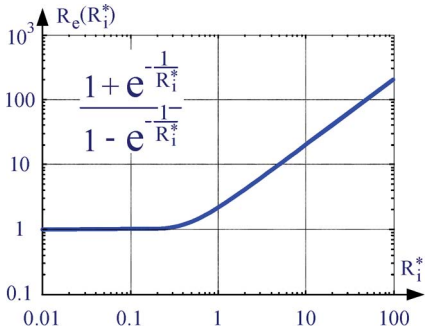

Fig. 1. Behavior of the exponential part of (4) as a function of the normalized loop resistance R_i^*. All other parameters are kept constant.

which is independent of the resistance value. This is apparently just a reflection of the fact that an energy balance calculation for the CC case produces the exact same expression, which implies that this result must be valid for any charging or discharging current profile provided that the operation is in the CC mode.

III. Losses in a Single Charge Transfer

An alternative method to examine the efficiency of SCC systems is to consider the losses of each subcircuit operating in open loop, as carried out in (3). Based on the results of [4], the energy lost in a subcircuit i E_i can be expressed as

$$E_i = (Q_i)^2 \cdot \left\{ \frac{1}{2C_i} \cdot \frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})} \right\} \tag{7}$$

where Q_i is the charge transferred during the interval T_i.

The loss presentation of (7) which applies Q_i as a reference (premise 2) reveals that the loss of a single charge transfer is a function of the switch resistance (embedded in β), save the case of complete charge/discharge ($\beta \gg 1$) when the values of the power terms approach zero.

In the limiting case, when the "on" duration is much smaller than the loop time constant ($\beta \ll 1$), one finds

$$\left(\frac{1+e^{-\beta_i}}{1-e^{-\beta_i}} \right)_{\beta \ll 1} \rightarrow \frac{2R_i C_i}{T_i} \tag{8}$$

and thus, the limiting values for the energy loss E_i can be formulated as

$$E_i = (Q_i)^2 \cdot \left\{ \frac{R_i}{T_i} \right\}. \tag{9}$$

The aforementioned equations reconfirm the fact that the charging/discharging loop resistance will affect the losses, except for the CC case. For the single event case, the loss per charge transfer can be reduced by increased T_i. However, an increase of T_i is not applicable to SCC systems since it dictates a decrease in switching frequency and, hence, a reduction in average-current transfer.

IV. Role of Switch Resistances in Regulated SCC

A corollary to the aforementioned discussion is the implication that switch resistances are important not only in SCC operating in open loop but also in regulated SCC systems, as observed in [9] and [10]. Output voltage regulation in SCC is normally achieved either by increasing the effective R_{ei} of one or more of the subcircuits or by charging one or more of the flying capacitors by a current source. The former can be conveniently achieved by changing the "on" duty cycles of the subcircuits (T_i in aforementioned equations), as shown in [4] and [9]–[11]. Hence, in this approach, regulation is realized

by increasing R_e to keep the output voltage at the desired level. Controlled current charging of a flying capacitor can also be used to regulate the output voltage of an SCC [8]. One way to explain the effect of the current control on the output voltage is by the increased losses (the power dissipated by the MOSFET used as a current source) which reduce the efficiency and thereby limit the energy reaching the output. In fact, any regulation method such as duty cycle control, current source control, frequency control, frequency dithering, or burst mode control is, in one way or another, adjusting the power dissipated by the converter. This stems from the physical fact that the output current of an SCC is related to the input current (save parasitic currents and leakages) by some factor n. Consequently, 100% efficiency would be reached if the output voltage is $1/n$ of the input voltage. Lower voltages imply lower efficiencies which are adjusted, in the regulated SCC, by controlling the losses along the internal charge-transfer paths.

Notwithstanding the fact that regulation is achieved by increasing the losses, the "on" resistances of the switches still play an important role. This is because a high switch resistance will limit the maximum possible efficiency for a given output current and, consequently, the maximum output-to-input voltage ratio for a given load. For example, consider a regulated 1:1 SCC that is stabilized to an output voltage of 5 V while the maximum input voltage is, for example, 10 V. Regulation at 10-V input will be achieved by increasing the losses, so the efficiency drops to 50%. However, the ability of the regulator to function in a low dropout (LDO) voltage situation, when the input voltage decreases and approaches 5 V, will depend on switch resistances. If the switch resistance is high, the converter will require a considerable dropout voltage and will not be able to operate when $V_{\rm in}$ is approaching 5 V. This is similar to the case of a linear regulator in which LDO operation is achieved by a series device that can be operated with low voltage across it.

V. Possible Reasons for Confusion

As mentioned previously, one possible reason for the impression that loop resistance of the subcircuits does not influence the efficiency of the SCC is (1) which seems to be independent of the switch resistances. However, V_o **is** a function of the switch resistances (3), save the case of the CC mode as discussed previously. Therefore, in the general case, (1) is, in fact, a function of the switch resistances.

The fact that, in the CC mode, the losses are independent of the switch resistance and of the charging/discharging current profile is possibly another reason for the underplaying of the resistance role. Clearly, however, to stay in the CC region, the switch resistance needs to be kept below $R_i^* \approx 0.1$; otherwise, the SCC will enter the PC region.

Another possible reason for reaching inconsistent conclusions regarding the influence of switch resistances on SCC losses is the application of analytical methods that lack a clear common reference (premise 2). In physics textbooks and many papers, the losses are expressed as a function of voltage differences and are not linked to the amount of charge or average current that passes during the charge/discharge process. However, voltage differences are not independent variables, and they are dictated by the charge that needs to be transferred by the SCC. Once this is taken into account, as expressed in (7) and (9), it becomes clear that, per charge, or average-current transfer, the losses are a function of the loop resistances, save the case of CC.

VI. Conclusion

Switch resistances are important attributes in open-loop and regulated SCC in both the charging and discharging processes, and in fact, there is no fundamental difference between the two processes with respect to losses. When SCC operate in the PC or NC mode, switch resistances influence the efficiency such that an increase in the resistances will increase the SCC losses. In the CC mode, an increase in switch resistances, while all other parameters are held constant including switching duration T_i, will not affect the efficiency until $R_i^* \approx 0.1$. From that point on, the SCC will enter the PC region, and the efficiency will drop. SCC operation in the deep CC mode is suggestive of poor design since their low switch resistances (and, hence, large silicone areas) do not improve the efficiency, while causing high peak currents. Switch resistances are also important in regulated SCC, since a high switch resistance will reduce the maximum achievable efficiency, i.e., the maximum output-to-input voltage ratio for a given load. A high switch resistance will thus limit the input voltage range for which regulation is possible [12].

Although the discussion in this letter has been focused on hard-switched SCC, the general conclusions—concerning the role of switch resistance—apply also to soft-switched SCC [2], as discussed in [4]. Furthermore, the losses of related circuits, such as capacitor-switched regenerative snubbers [13], are also a function of the loop resistance.

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