Letters

Behavioral Average Modeling and Equivalent Circuit Simulation of Switched Capacitors Converters

Shmuel (Sam) Ben-Yaakov, *Fellow, IEEE*

***Abstract*—A generic behavioral average circuit model of a switched capacitor converter (SCC) is proposed and demonstrated by a unity conversion SCC. The model is based on the average currents concept and can be used to calculate or simulate the average values of the SCC variables such as output voltage, capacitor voltages, and subcircuit currents. The model is valid for all operational ranges of an SCC (complete, partial, and no charge) and is compatible with any circuit simulator that includes dependent sources. Excellent agreement was found between full switched-circuit simulation, average simulation by proposed model, and experimental results.**

***Index Terms*—Modeling, power conversion, simulation, SPICE, switched capacitor converters.**

I. Introduction

SWITCHED capacitor converters (denoted as SCC for singular and plural instances), also referred to as "Charge Pumps," have inherent losses that make their use prohibitive in many applications. Even so, SCC are preferred in a number of cases due to their IC compatibility, relatively small size, and the absence of magnetic elements. SCC can be modeled as a network that is configured by the switches to a set of subcircuits that charge and discharge flying capacitors. The average behavior of SCC systems was analyzed in numerous earlier studies (see, e.g., [1]–[11]), in which the expressions of the voltage transfer ratios and the expected losses were derived. Full circuit simulation can be carried out by various software packages to verify the theoretical calculations and to test alternative designs. However, full simulation that includes the switching transients suffers from at least two deficiencies: the need for long simulation time and convergence problems due to the fast transitions caused by the switches. As experienced in the case of switched inductor converters [12]–[15], average circuit simulation could help to alleviate these problems and, in fact, can provide additional information and a better insight into the simulated converter.

Manuscript received November 18, 2010; revised April 5, 2011 and July 15, 2011; accepted September 1, 2011. Date of current version January 9, 2012. This work was supported by the Israel Science Foundation under Grant 476/08 and Grant 517/11. Recommended for publication by Associate Editor R. (Letters AE) Zane.

The author is with the Power Electronics Laboratory, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva, 84105 Israel (e-mail: sby@ee.bgu.ac.il).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2011.2171996

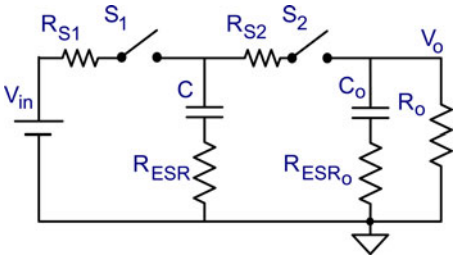


Fig. 1. Unity conversion ratio SCC.

The objective of this study was to develop an average model of SCC systems that would be compatible with any circuit simulator and be capable of providing pertinent data such as the output voltage, the average current in the subcircuits, the average voltage across the capacitors, and the efficiency. Furthermore, average circuit models can help to gain a better understanding of the role of switch resistance, capacitance value, clock duration, and duty cycle. The proposed simulation model is in fact a translation of the analytical results of [10] into average equivalent circuits. As such, the accuracy of the model is identical to the results of [10] and it is limited by the assumptions of its derivation (such that the subcircuits can be approximated by a first-order *RC* circuit).

II. Basic Theoretical Considerations

For the sake of clarity and brevity, we consider first a 1:1 SCC system depicted in Fig. 1. The converter includes a flying capacitor C with a lossy component $R_{\rm ESR}$, two switches S_1 and S_2 with "ON" resistances of R_{s1} and R_{s2}, respectively, an output filter capacitor C_o with $R_{{\rm ESR}o}$ and load resistance R_O. As the switches run at a frequency of f_s, the circuit toggles between two subcircuits; one during T_1, when S_1 is "ON" [see Fig. 2(a)], and the other during T_2, when S_2 is "ON" [see Fig. 2(b)]. R_1 and R_2 in Fig. 2 represent the total loop resistances

$$R_1 = R_{s1} + R_{\rm ESR} \tag{1}$$

$$R_2 = R_{s2} + R_{\rm ESR} + R_{{\rm ESR}_o}. \tag{2}$$

Each of the subcircuits can be represented by a generic charging circuit (see Fig. 3) that includes a voltage source ΔV_i (where i is 1 for duration T_1 and 2 for T_2), a resistor R_i, and a capacitor C_i

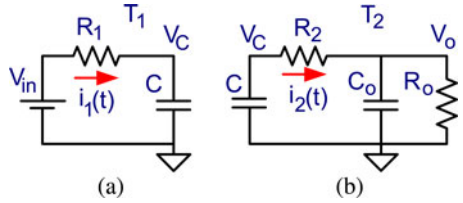


Fig. 2. Subcircuits of the SCC of Fig. 1. (a) Duration T_1; (b) Duration T_2.

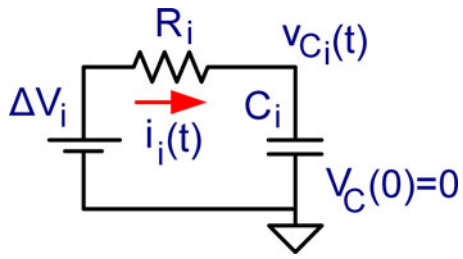


Fig. 3. Generic capacitor-charging equivalent circuit.

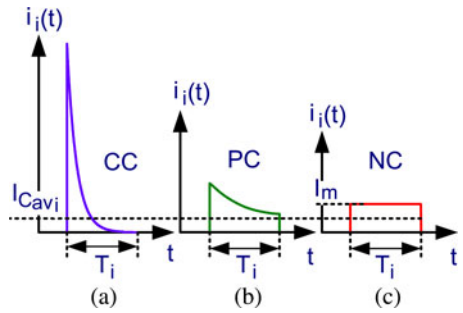


Fig. 4. Possible charging current shapes. (a) Complete charge (CC). (b) Partial charge (PC). (c) No charge (NC).

with an initial condition of zero voltage. For the 1:1 converter

$$C_1 = C \tag{3}$$

$$C_2 = \frac{C \cdot C_o}{C + C_o}. \tag{4}$$

ΔV_i is the voltage across the relevant switch just before it is turned ON.

Once a switch is turned ON, the equivalent capacitor will start charging (by a positive or negative ΔV_i) and a current $i_i(t)$ will build up. Depending on the relationship between the duration T_i and the time constant R_iC_i, the current can take one of three possible shapes. For $T_i >> R_iC_i$, the charging will be completed within T_i [see Fig. 4(a)] this case is denoted as CC. For $T_i \cong R_iC_i$, the charging will be partial [PC, Fig. 4(b)]. For $T_i << R_iC_i$, there will be no effective charging (NC) and the current will be practically constant [see Fig. 4(c)]. In this latter case, the capacitor voltage will stay about constant within T_i.

Assuming a steady-state condition, the average value of the current during T_2, I_{Cav2} (averaged over a switching cycle T_s), will be equal to the output current I_o. Namely

$$I_{\mathrm{Cav2}} = \frac{1}{T_s}\int_0^{T_s} i_2(t)dt = I_o. \tag{5}$$

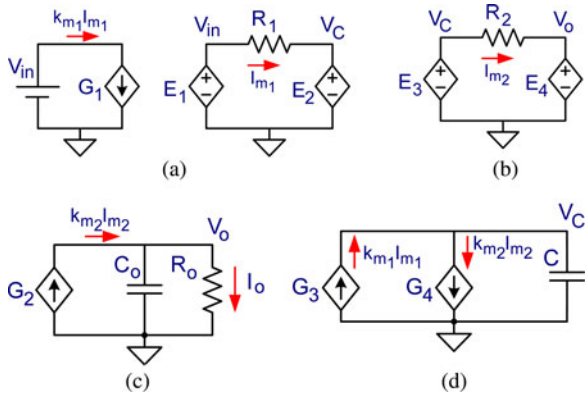


Fig. 5. Average equivalent circuit model of the 1:1 SCC. (a) Emulation of first row of matrix (8). (b) Emulation of second row of (8). (c) Output section. Third row of (8). (d) Capacitor charge balance. Fourth row of (8).

And since the total average current through C is zero

$$I_{\mathrm{Cav2}} = I_{\mathrm{Cav1}} = I_o. \tag{6}$$

Concentrating first on the NC case ([see Fig. 4(c)], the currents I_{mi} within durations T_1 and T_2 are related to the average current I_{Cav} by a factor k_m:

$$k_{\mathrm{mi}} \equiv \frac{I_{\mathrm{Cavi}}}{I_{\mathrm{mi}}} = \frac{T_i}{T_s}. \tag{7}$$

Based on the above, one can summarize the voltage and current relationships for the NC case by the following set of equations:

$$\begin{bmatrix} V_{\mathrm{in}} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & R_1 & 0 \\ 1 & -1 & 0 & R_2 \\ 0 & -\frac{1}{R_o} & 0 & k_{m2} \\ 0 & 0 & -k_{m1} & k_{m2} \end{bmatrix} \begin{bmatrix} V_C \\ V_o \\ I_{m1} \\ I_{m2} \end{bmatrix}. \tag{8}$$

The first two rows of aforementioned matrix are KVL for T_1 and T_2 durations (see Fig. 2), while the third and fourth rows restate (5) and (6).

The set of (8) can be emulated by an equivalent circuit that includes dependent sources and passive elements as follows. The first row is emulated by the circuit of Fig. 5(a) that includes a dependent source E_1 which replicates V_{in}, a resistor R_1, and a dependent voltage source E_2 which replicates the voltage on capacitor C. The instantaneous current I_{m1} is scaled by G_1 to represent the average current (over T_s) that loads the source V_{in}. Similarly, the second row is emulated by the circuit of Fig. 5(b) and the third row by Fig. 5(c). The fourth row which is related to the capacitor's charge balance is emulated by a capacitor C that is fed by two opposing current sources (G_1, G_2) that represent the average currents (over T_s) of the two subcircuits.

The definitions of the dependent sources are thus

$$E_1 \equiv V_{\mathrm{in}};\ E_2 \equiv V_C;\ E_3 \equiv V_C;\ E_4 \equiv V_o \tag{9}$$

$$G_1 \equiv k_{m1}I_{m1};\ G_2 \equiv k_{m2}I_{m2};\ G_3 \equiv k_{m1}I_{m1};$$

$$G_4 \equiv k_{m2}I_{m2}. \tag{10}$$

It should be noticed that the equivalent circuit of Fig. 5 includes instantaneous currents in the KVL circuits [I_m in Fig. 5(a) and

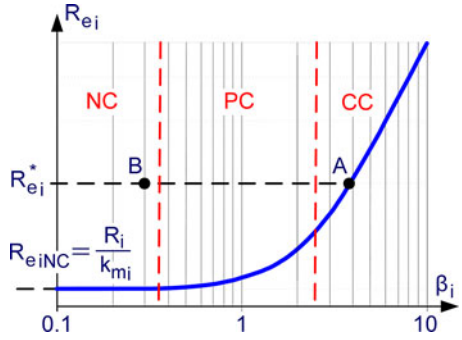


Fig. 6. Behavior of equivalent resistance $R_{\rm ei}$ of a subcircuit. Smooth curve: (8). "A" point: CC operation. "B" point: NC operation of emulating subcircuit.

(b)] and average currents at the input [see Fig. 5(a)], output [see Fig. 5(c)], and charge balance [see Fig. 5(d)] circuits. This is necessary to keep correct KVL relationships on the one hand and, on the other, to maintain correct charge-balance and correct power relationships. It should also be noticed that the model of Fig. 5 assumes a constant voltage on the capacitors which is the correct situation in the NC case and compatible with the notion of "average model."

The equivalent circuit of Fig. 5 includes quite a number of dependent sources that might cause simulation conversion problems. These can be eased by eliminating some of the dependent sources by, e.g., combining the two sections of Fig. 5(a) and replacing E_2 by the capacitor.

III. Extension to the General Switching Case

The model developed in Section II was based on the assumption that the modeled SCC operates in the NC region [see Fig. 4(c)]. The extension of the model to the general case to include the CC and PC modes [see Fig. 4(a) and (b)] can be carried out by applying the relationships between the operational conditions and power dissipation as follows.

As was proven in an earlier publication [10], the average power P_i dissipated by a given subcircuit i during a switching phase duration T_i can be expressed as

$$P_i = (I_{\rm Cavi})^2 \cdot \left\{ \frac{1}{2f_s C_i} \cdot \frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})} \right\}, \quad \beta_i = \frac{T_i}{R_i C_i}. \tag{11}$$

The term in bracket can be defined as the equivalent resistance $R_{\rm ei}$ of switching phase i:

$$R_{ei} = \left\{ \frac{1}{2f_s C_i} \cdot \frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})} \right\}. \tag{12}$$

The behavior of the equivalent resistance function (12) as a function of β shows an increase in value when this parameter becomes larger (see Fig. 6). Applying Taylor series expansion, the asymptotic value of this function $R_{ei\rm NC}$ for the NC case ($T_i << R_i C_i$) is found as the limit of (12) when $\beta << 1$ (see Fig. 6, horizontal line at the bottom of the curve):

$$R_{ei\rm NC} = R_i \frac{T_s}{T_i} = \frac{R_i}{k_{mi}}. \tag{13}$$

Turning now to the CC case ($T_i >> R_i C_i$; $\beta >> 1$), the behavior of the equivalent resistance ($R_{ei\rm CC}$) follows the function:

$$R_{ei\rm CC} = \frac{1}{2f_s C_i}. \tag{14}$$

This is the rising part of the R_{ei} plot shown in Fig. 6.

Assume now that a subcircuit of the given SCC operates under some arbitrary β conditions such that its equivalent resistance is R^*_{ei} and that its position on the plot of Fig. 6 is at point A. That is, outside the NC region. Considering the behavior of (12), it follows that the same power dissipation will be observed in an emulating subcircuit that operates at point B (see Fig. 6) under NC condition, if its loop resistance R^*_i obeys the relationship

$$\frac{R^*_i}{k_{\rm mi}} = R^*_{ei}. \tag{15}$$

This implies that the CC and PC cases can be emulated by an equivalent circuit that is assumed to operate under NC conditions, if the loop resistance is adjusted for equal dissipation. Based on this observation, one can formulate the rules for developing an average circuit model for an SCC running under the CC, PC, or NC conditions.

1) Applying (12), calculate $R_{\rm ei}$ for all of the SCC subcircuits i.
2) Applying (15), calculate the loop resistance R^*_i of the emulating NC subcircuits. Note that for a subcircuit operating in NC: $R^*_i = R_i$.
3) Applying the emulating equivalent resistance values R^*_i, construct the average model as if the subcircuits are operated in the NC region, as discussed in Section II.

The previously proposed procedure requires the calculation of R^*_i for each simulation case. The procedure can be mechanized by defining the resistances R^*_i as variable resistors based on (12) and (15).

IV. Verification by Full Circuit Simulation and by Experiments

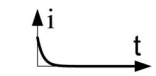
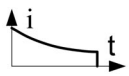
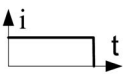
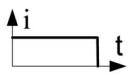
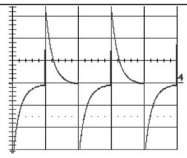
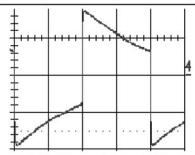
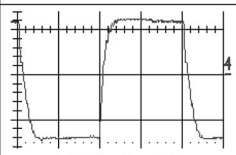
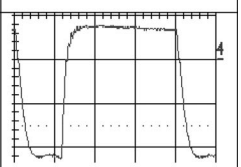
The proposed modeling and simulation approach was verified against full circuit simulations and experimentally. The simulated circuit was the unity SCC of Fig. 1 assumed to have the following parameters:

$$R_{S1}, R_{S2} = 2\Omega;\ C = 10\,\mu{\rm F};\ R_{\rm ESR} = 0.2\,\Omega;$$
$$C_o = 1\,{\rm mF};\ R_o = 10\,\Omega;\ V_{\rm in} = 12\,{\rm V}.$$

The experimental switches were MOSETs IRF540 with added series resistors to reach the 2 Ω values.

The simulation runs cover the three operational regions, CC, PC, and NC and include a case of different durations for T_1 and T_2.The full simulation was carried out by SPICE (OrCAD Ver. 15) applying switches with series resistances to represent the MOSFETS and behavioral dependent sources (EVALUE and GVALUE) to represent the sources of Fig. 5. The "expressions" of these sources were as given in Fig. 5. All the parts of the simulation model need, of course, to be run simultaneously. Some of the simulation results are given in Table I to demonstrate the excellent agreement that was observed. Table I summarizes

TABLE I
SUMMARY OF AVERAGE MODEL SIMULATION, FULL CIRCUIT SIMULATION, AND EXPERIMENTAL RESULTS

Mode / Parameters	CC	PC	NC	NC
				
f_s	5 kHz	25 kHz	250 kHz	250 kHz
k_{m1}	0.5	0.5	0.487	0.7
k_{m2}	0.5	0.5	0.487	0.3
R_{e1}	10.21 Ω	4.71 Ω	4.51 Ω	3.01 Ω
R_{e2}	10.21 Ω	4.71 Ω	4.51 Ω	9.02 Ω
V_C Full simulation	8.00 V	9.09 V	9.15 V	10.36 V
V_C model	7.97 V	9.09 V	9.15 V	10.36 V
V_C Experimental	8.03 V	9.23 V	9.17 V	10.24 V
V_o (DC) Full simulation	3.94 V	6.17 V	6.3 V	5.45 V
V_o (DC) Model	3.94 V	6.18 V	6.3 V	5.45 V
V_o (DC) Experimental	3.86 V	6.17 V	6.07 V	5.34 V
Experimental Capacitor Current Waveforms	 1A/Div; 1ms/Div	 1A/Div; 10μs/Div	 1A/Div; 1μs/Div	 1A/Div; 1μs/Div

the output voltage obtained by proposed simulation model (see Fig. 5), full switched circuit simulation (cycle-by-cycle simulation) and by the experiments.

Excellent agreement was found between the full switched-circuit, average-circuit simulations, and the experimental results. The small deviations of the experimental results from the simulated values at the higher switching frequency are probably due to the finite rise time and dead time of the test circuit. It should be pointed out though, that deviations might be expected if the subcircuits cannot be approximated by a first-order system since the original analytical derivation, on which the proposed simulation model is based [10], assumes a single *RC* charge/discharge process as shown in Fig. 2. For example, if the output capacitor would have been smaller (say 100 μF), the effect of the output pole (C_O, R_O) would have been larger and 2–3% errors would have been observed. Considering the fact that the proposed simulation model hinges on the analytical derivations of [10], which were validated by simulation as well as by experiments, it is accurate to the level of the original model [10].

V. DISCUSSION AND CONCLUSION

The proposed modeling concept described in this letter is fundamentally different from previously published equivalent circuit models of SCC. A main attributes of the new modeling approach is that it covers all operational ranges and not just the asymptotic CC and NC regions (denoted in [7] as the SSL and FSL regions). Another feature of the model is that it can be used to examine the effects of individual elements such as the resistance of each switch, the ESR of each capacitor, the influence of capacitors' values, and the effect of the switching frequency and duty cycle. That is, it generates, on the fly, the contribution of each of the relevant parameters to the total resistance of the SCC converter denoted R_e in [7]. By this, the user can study the contribution of each factor that affects the losses.

Although discussed and demonstrated by a 1:1 SCC, the proposed modeling methodology can be easily applied to multi capacitors and multi phase SCC systems such as those described in [16] by following the examples introduced in [10] and [17]. However, since the proposed model is based on (12) for each subcircuit, it holds only for cases in which the subcircuits can be described as a first-order system. That is, including a single time constant each. SCC topologies that include subcircuits of a higher order are, therefore, not compatible with this modeling approach. It has been shown, though, [10] that in many practical cases, the higher order networks can be approximated by a single time constant and can thus be described by the model presented in [10].

The proposed modeling approach presented here is also valid for SCC systems that apply diodes as switching elements. Following [10] and [17], the inclusion of such diode in the proposed model is straightforward since the KVL-based subcircuits of the model carry the instantaneous currents, and hence if the diodes are placed in the equivalent circuit subcircuits, they will be exposed to the real physical currents that develop in the SCC.

Consequently, the average current through the diodes and the average voltage across them will be correct.

The proposed equivalent circuit model applies the average signal characteristics of SCC systems and like any average models it is transparent to the switching process itself including sampling effects. Since only "bias point" simulation is required for model, the simulation run time is appreciably shorter than full (switched) simulation, especially when a multiphase multicapacitor SCC is examined.

The proposed averaging approach can provide an insight into the operation of SCC systems and help designers to optimize such systems. Being transparent to the switching process, the proposed average simulation model is free of convergence problems that are associated with fast transitions. Even so, convergence problems might arise due to the intricate relationship between the dependent sources that make it difficult for the simulator's algorithm to calculate the bias point.

Another issue that is still unanswered is the ability of the model to predict the dynamic response of the emulated SCC. Further research is needed to resolve this question.

ACKNOWLEDGMENT

The author would like to thank M. Evzelman for carrying out the experiments and some of the simulations for this study and for his editorial assistance.

REFERENCES

[1] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor DC–DC converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 3, no. 1, pp. 92–101, Jan. 1994.

[2] I. Oota, N. Hara, and F. Ueno, "A general method for deriving output resistances of serial fixed type switched-capacitor power supplies," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2000, vol. 3, pp. 503–506.

[3] W.-C. Wu and R. M. Bass, "Analysis of charge pumps using charge balance," in *Proc. IEEE Power Electron. Spec. Conf.*, 2000, vol. 3, pp. 1491–1496.

[4] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, Third Quarter 2001.

[5] Y. P. B. Yeung, K. W. E. Cheng, S. L. Ho, K. K. Law, and D. Sutanto, "Unified analysis of switched-capacitor resonant converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 864–873, Aug. 2004.

[6] J. W. Kimball and P. T. Krein, "Analysis and design of switched capacitor converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2005, vol. 3, pp. 1473–1477.

[7] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[8] I. Oota, N. Hara, and F. Ueno, "A general method for deriving output resistances of serial fixed type switched-capacitor power supplies," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2000, vol. 3, pp. 503–506.

[9] M. Keskin, N. Keskin, and G. C. Temes, "An efficient and accurate DC analysis technique for switched capacitor circuits," in *Proc. Analog Integr. Circuits Signal Process.*, 2002, vol. 30, no. 3, pp. 239–242.

[10] S. Ben-Yaakov and M. Evzelman, "Generic and unified model of switched capacitor converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 3501–3508.

[11] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 127–136, Jan. 2011.

[12] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 490–496, May 1990.

[13] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 497–505, May 1990.

[14] S. Ben-Yaakov, "SPICE simulation of PWM DC-DC convertor systems: Voltage feedback, continuous inductor conduction mode," *Electron. Lett.*, vol. 25, no. 16, pp. 1061–1063, Aug. 1989.

[15] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioral relationships," *Int. J. Electron.*, vol. 77, pp. 731–746, 1994.

[16] S. Ben-Yaakov and A. Kushnerov, "Algebraic foundation of self adjusting switched capacitors converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, San Jose, CA, Sep. 20–24, 2009, pp. 1582–1589.

[17] M. Evzelman and S. Ben-Yaakov, "Optimal switch resistances in switched capacitor converters," in *Proc. IEEE 26th Convention Electr. Electron. Eng. Israel*, Eilat, Israel, 2010, pp. 436–439.