Letters to the Editor

PWM Converters with Resistive Input

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***Abstract*—An average modeling methodology is proposed for deriving pulsewidth modulation (PWM) programming rules that cause dc–dc converters to look resistive at the input terminals. The method can be useful in the design of active power factor correctors that do not need to sense the input voltage.**

***Index Terms*—Power factor, modeling, simulation.**

I. INTRODUCTION

The current interest in active power factor correction (APFC) [1]–[5] prompts investigators to look for improved methods to shape the input current of pulsewidth modulation (PWM) converters. Two groups of solutions have been proposed hitherto: 1) those that rely on direct current feedback [2] and 2) those that apply indirect input current control [3]–[5]. Here, we present an average modeling methodology that can help to derive indirect control schemes for input current shaping of PWM converters.

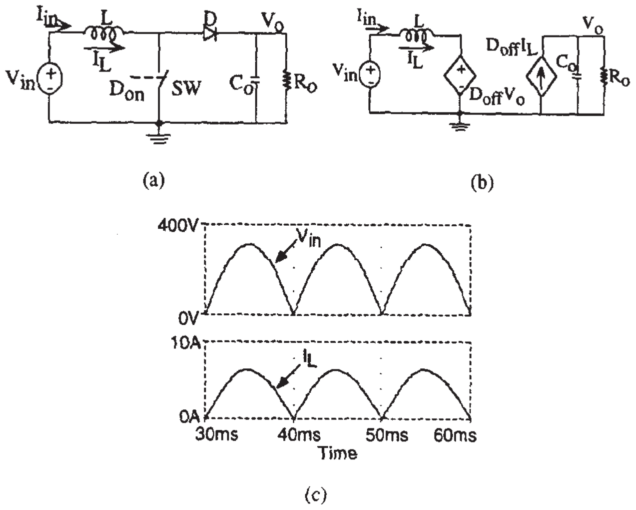

Fig. 1. (a) The Boost converter, (b) its behavioral average model (after [5] and [6]), and (c) results of average simulation when applying this behavioral model, while D_{off} is programmed according to (4).

II. THE BOOST TOPOLOGY

The proposed methodology will first be described in relation to the Boost converter [Fig. 1(a)]. It is assumed that the converter is driven by a duty cycle D_{on} and that it operates under continuous current mode (CCM) conditions. As shown previously [6], [7], the function of the converter can be represented by the behavioral model of Fig. 1(b). One can now apply a power circuit theory corollary, i.e., under stable conditions, the average voltage across a power inductor L must be zero (otherwise, the current will rise to infinity). Assuming that the circuit is stable (see below), this implies [Fig. 1(b)]

$$V_{\text{in}} = D_{\text{off}} V_o \tag{1}$$

where D_{off} is (1-D_{on}). V_{in} is the average input voltage, and V_o is the average output voltage. Averaging is over one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

Since the average input current I_{in} is equal to the average inductor current I_L, (1) can be manipulated to the form

$$\frac{V_{\text{in}}}{I_{\text{in}}} = \frac{D_{\text{off}} V_o}{I_L}. \tag{2}$$

To make the input resistive with an input resistance R_e, we require

$$\frac{V_{\text{in}}}{I_{\text{in}}} = R_e = \frac{D_{\text{off}} V_o}{I_L}. \tag{3}$$

That is, a resistive input will be observed if D_{off} is programmed according to the rule

$$D_{\text{off}} = \frac{R_e}{V_o} I_L. \qquad 0 < D_{\text{off}} < 1 \tag{4}$$

which implies that the input signal to the PWM modulator, used to generate D_{off}, should be proportional to the average current of the inductor. It should be noted that this relationship introduces negative feedback and, hence, helps to insure stable operating conditions.

The control concept of (4) was tested by running a behavioral SPICE simulation [6], [7] on the model of Fig. 1(b). For the results presented in Fig. 1(c), D_{off} was set according to (4), (R_e/V_o) was 0.127 A^{-1}, $V_{\text{in}} = |310\sin(2\pi 50t)|(\text{V})$. where t is time (s). Other parameters were $R_o = 144\ \Omega$. $C_o = 1000\ \mu\text{F}$, and $L = 1$ mH. The equivalent circuit used in the simulation included an independent source and two behavioral depended sources and all the passive components [Fig. 1(b)]. The definition of the behavioral voltage depended source was $(I_L \cdot 0.127 \cdot V_o)$, while that of the current source was $(I_L^2 \cdot 0.127)$ where I_L is the sensed current of the inductor, and V_o is the voltage of the output node, respectively. During the simulation run, the system reached a steady-state output voltage of 380 V, while the input current clearly demonstrates the resistive nature of the converter's input terminals [Fig. 1(c)].

In APFC systems, V_o needs to be stabilized and R_e adjusted as a function of the load and input voltage. One possible way to achieve this is proposed in Fig. 2(a). The voltage error amplifier (*E/A*) should have a slow response, so as not to react within the mains cycle. The multiplier (*M*) generates the programmed voltage that is modulated by the *PWM* modulator to obtain D_{off}. This control scheme was tested by a PSPICE (Microsim Company) cycle-by-cycle simulation. The parameters of the power stage and modulator were as given above. The bandwidth of the *E/A* was 10 Hz, the switching frequency was 50 kHz, and the bandwidth of the low-pass filter [Fig. 2(a)] was 80 kHz. The simulation results [Fig. 2(b)] clearly demonstrate the validity of the approach.

III. EXTENSION TO OTHER PWM TOPOLOGIES

Following the same derivation procedure, the programming rules for other PWM topologies are easy to develop. For example, in the

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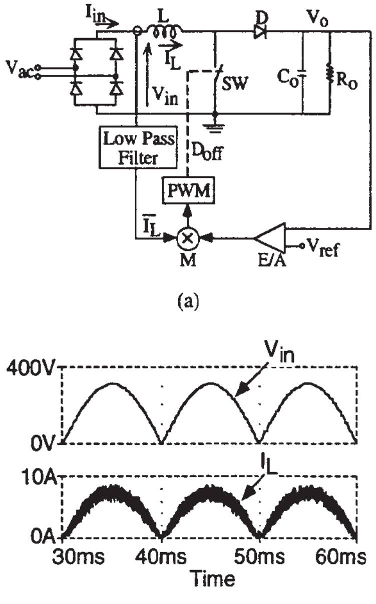


(a)

(b)

Fig. 2. (a) Possible realization of proposed control method and (b) results of cycle-by-cycle simulation of its performance.

Buck topology, the average voltage across the inductor is ($V_{in} \cdot D_{on} \cdot V_o$), while the input current to the converter is ($I_L \cdot D_{on}$). Manipulating these expressions, the programming rule for Buck is found to be

$$D_{on} = \sqrt{\frac{V_o}{I_L R_e}}, \qquad 0 < D_{on} < 1. \tag{5}$$

For Buck–Boost, the programming rule is

$$D_{on} = \frac{V_o + \sqrt{V_o^2 - 4R_e I_L V_o}}{2R_e I_L}, \qquad 0 < D_{on} < 1. \quad V_o \leq 0. \tag{6}$$

Clearly, out of the three basic PWM topologies, the Boost programming rule is the simplest. For the other topologies, a more elaborate modulator will have to be used.

The generic methodology presented above for deriving programming rules to obtain resistive inputs applies the average inductor current as a control signal. However, since the average switch current and average diode current are a function of the inductor's current, the programming rules can be made dependent on the average diode or switch current. For example, since the average switch current (I_{SW}) is related to the average inductor current [6], [7] by

$$I_{in} = \frac{I_{SW}}{1 - D_{off}} \tag{7}$$

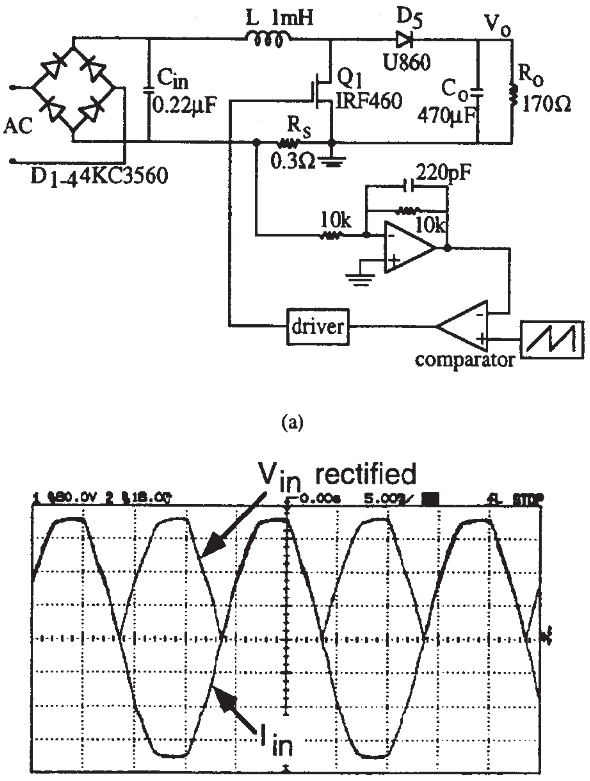
the programming rule for the Boost converter can be modified to

$$D_{off} = \frac{V_o \pm \sqrt{V_o^2 - 4I_{SW} R_e V_o}}{2V_o}, \qquad 0 < D_{off} < 1. \tag{8}$$

This programming rule [3] and the one that applies the average diode current [4] can, thus, be considered private cases of the generic input current shaping methodology presented here.

IV. EXPERIMENTAL

A prototype converter was built [Fig. 3(a)] and tested in open outer loop, namely, without controlling the output voltage [Fig. 2(a)]. In this mode, the output voltage will depend on the input current, which, in turn, is a function of the input voltage and the value of the programmed R_e. The actual implementation [Fig. 3(a)] included a Boost stage and a simple D_{off} programming scheme. The tracking quality obtained experimentally is demonstrated by overlapping the line current and the rectified input voltage [Fig. 3(b)].



(a)

(b)

Fig. 3. (a) Experimental setup and (b) its performance at a 1-kW power level. Vertical scales: 80 V/div and 1.6 A/div. Horizontal scale: 5 ms/div.

V. CONCLUSIONS

The PWM modulation rules developed by the proposed methodology can be used to design APFC circuits and other realizations of input terminals impedances. The main advantage of the circuits developed by this method is the fact that there is no need to sense the input (often noisy) voltage and that the required control circuit is simple.

REFERENCES

[1] *Electromagnetic Compatibility (EMC)*, IEC Standard 1000-3-2, 1995, pp. 1–47.

[2] R. Mamano, "New developments in high power factor circuit topologies," in *Conf. Rec. HPFC*, 1996, pp. 63–74.

[3] D. Maksimovic, Y. Jang, and R. Erickson, "Nonlinear-carrier control for high power factor Boost rectifiers," in *Conf. Rec. IEEE APEC*, 1995, pp. 635–641.

[4] J. Hwang, A. Chee, and W.-H. Ki, "New universal control methods for power factor correction and DC to DC converter applications," in *Conf. Rec. IEEE APEC*, 1997, pp. 59–65.

[5] J. Rajagopalan and F. C. Lee, "A generalized technique for derivation of average current mode control laws for power factor correction without input voltage sensing," in *Conf. Rec. IEEE APEC*, 1997, pp. 81–87.

[6] S. Ben-Yaakov, "SPICE simulation of PWM DC-DC converter systems: Voltage feedback, continuous inductor conduction mode," *Electron. Lett.*, vol. 25, no. 16, pp. 1061–1063, Aug. 1989.

[7] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioral relationships," in *Conf. Rec. IEEE APEC*, 1993, pp. 510–516.