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THE SELF-ADJUSTING CURRENT-FED PUSH-PULL PARALLEL RESONANT INVERTER AS A HIGH FREQUENCY AC BUS DRIVER

Mor Mordechai Peretz and Sam Ben-Yaakov

Power Electronics Laboratory, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev, P.O.Box 653, Beer-Sheva 84105, ISRAEL
Tel: +972-8-6461561; Fax: +972-8-6472949;
Email: sby@ee.bgu.ac.il ; Website: http://www.ee.bgu.ac.il/~pel

ABSTRACT

A self-adjusting sinusoidal power source for high-frequency AC distributed power bus is presented and tested experimentally. The power inverter is based on a Current-Fed Push-Pull Parallel-Resonant Inverter (CFPPRI), which includes a variable inductor and a frequency tracking mechanism to insure soft switching. The power source can drive reactive, non-linear, switched and non-constant loads with a sinusoidal signal at a desirable frequency. The response of the power driver to a 60% to 100% step in the load power was found to stabilize within three high frequency cycles.

1. INTRODUCTION

A distributed power supply system applies a bus that spreads the primary power to the subunits, and on-board switch-mode converters that generate the required local supply voltages. The distributed power supply approach has several advantages over the central power supply solution: it reduces voltage drops due to high ground currents, facilitates isolation and thereby reduces common mode interferences, increases reliability and distributes the power loss. At present, practically all distributed power supply systems apply a DC bus, but similar to the reason why the power line is AC, there are advantages to using a high frequency AC bus (HFAC). The main advantage of an HFAC is the possibility of applying high frequency transformer at the input of the on board converters and thereby simplifying the isolation circuitry.

Notwithstanding the fact that the use of a HFAC bus for distributing power eliminates some of the conversion units, it poses new design challenges [1]: (a) Electromagnetic interference, (b) Bus waveshape – performance and efficiency of the load converters may be dramatically reduced due to a supply signal that is rich in harmonic content, and (c) Point-of-load (POL) – the ability of the power source to drive various types of loads, such as reactive, non-linear and non-constant.

The Self-Adjusting Current-Fed Push-Pull Parallel Resonant Inverter (SA-CFPPRI) was shown earlier [2, 3] to be able to drive reactive loads with a sinusoidal output signal at a predetermined frequency and remain constant (amplitude and waveform wise) even for a non-constant reactive load (inductive and capacitive). This solves the first two challenges of the HFAC bus. IN this study we explored the dynamics of the SA-CFPPRI when loaded by a switched load, as expected in a HFAC distributed power source.

2. THE CURRENT-FED PUSH-PULL PARALLEL RESONANT INVERTER (CFPPRI)

The basic CFPPRI topology [4] (Fig. 1) includes a push-pull stage that consists of two transistors (Q_1, Q_2) fed by a series inductor (L_{in}), and drives a parallel resonant network. The load is fed via a secondary winding that allows for amplitude adjustment by the turns ratio ($n_2/2n_1$).

Steady State Operation: When the gate voltage of Q_1 (V_{GS1}, Fig. 1) goes high and the voltage of Q_2 (V_{GS2}, Fig. 1) goes low, the drain voltage of Q1 (V_{DS1}, Fig. 1) is forced to zero and the tank voltage (V_{DS2} in this case) starts to rise in a sinusoidal shape. When this voltage reaches back to zero, switching occurs ($f_s=f_r$) and a new half cycle begins. In this case the transistors will operate under Zero Voltage Switching (ZVS) conditions (Fig. 2a). In the case that the switching frequency is lower than the resonant frequency (Fig. 2b), one of the antiparallel diodes will start conducting and the operation will include a boost period [4], which will cause distortion in the output voltage and increase conduction losses. If the switching frequency is higher than the resonant frequency (Fig. 2c) the operation will be under hard switching conditions. The functional circuit of the CFPPRI for one-half cycle is represented by the simplified equivalent circuit of Fig. 3a.

Output Voltage in Steady State: Assuming that $f_s=f_r$ and symmetry of one-half cycle, the output voltage will be sinusoidal and can be expressed as:

$$V_{Load}(t) = V_{Lpk}\cos(\omega_r t) \qquad (2)$$

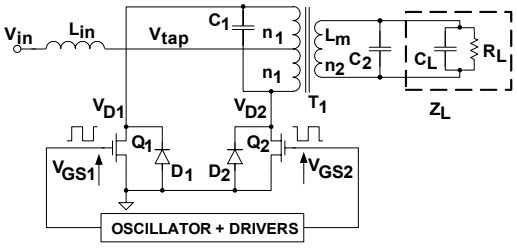

Figure 1. Basic configuration of the CFPPRI loaded by a capacitive load.

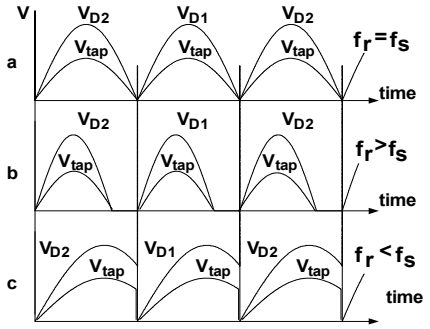

Figure 2. Drain voltages (V_D) and tap voltage (V_{tap}) when the gate-drive frequency matches the resonant frequency (a) and when it is lower (b) or higher (c) than the resonant frequency

where, V_{Lpk} is load peak voltage and ω_r is the resonant frequency ($\omega_r=2\pi f_r$).

After reflecting all components and signals to the primary winding (simplified reflected circuit is shown in fig. 3b) the average center tap voltage (V_{tap}, Figs. 1 and 3) is given by:

$$V_{tapav} = \frac{1}{\pi}\int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{V_{Lpk}}{n}\cos(\omega_r t)dt = \frac{2}{\pi}\frac{V_{Lpk}}{n} \qquad (3)$$

where, n is the turns ratio of the transformer T_1 of fig. 1.

Since the average voltage across the input inductor (L_{in}) must be equal to zero at steady state, it can be stated that:

$$V_{tapav} = V_{in} \qquad (4)$$

where, V_{in} is the input voltage of the inverter.

Combining (3) and (4) and isolating V_{Lpk}, yields the peak output voltage in terms of the input voltage:

$$V_{Lpk} = n\pi\frac{V_{in}}{2}. \qquad (5)$$

Eq. (5) implies that, in steady state, the load voltage is independent of the load value, which is a highly desirable feature for an HFAC distributed power bus driver.

Output Voltage under Transient conditions: Eq. (5) establishes the independence of the output voltage of the load in steady state. However, in the case of switched or non-constant loads, the system, which is of third order (LLC), will enter a transient period in which the output voltage will depend on the network characteristics. Out of symmetry considerations, one-half cycle operation will be analyzed, under the assumption that the next half cycle starts at the end of the previous cycle with no delay and is identical but with a resonant inductor (L_r) current of opposite directions.

The input inductor voltage is expressed by:

$$v_{in} - v_{Lr} = v_{Lin} \qquad (6)$$

or

$$v_{in} - L_r\frac{di_{Lr}}{dt} = L_{in}\frac{di_{Lin}}{dt} \qquad (7)$$

where L_r is the resonant inductance and L_{in} is the input inductance reflected to the primary ($L_{in}=4L_{in}'$).

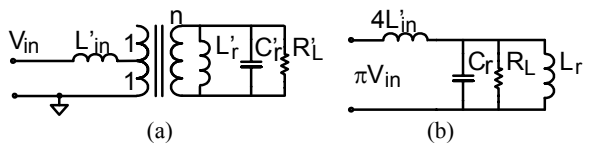

Figure 3. CFPPRI simplified circuit. (a) One-half cycle operation and (b) reflected to the primary.

Integrating (7) and isolating i_{Lin}, yields:

$$i_{Lin}(t) = \frac{v_{in}}{L_{in}}t - \frac{L_r}{L_{in}}\left(i_{Lr} - I_{Lr}(0)\right) + I_{in}(0) \qquad (8)$$

where $I_{Lr}(0)$ and $I_{in}(0)$ are the initial conditions of the resonant inductor and the input inductor respectively.

Applying KCL we derive:

$$i_{in} = i_{L_r} + i_{C_r} + i_{R_L} \qquad (9)$$

where

$$v_{Lr} = v_{Cr} = v_{RL} = L_r\frac{di_{Lr}}{dt}\ ,\ \ i_{RL} = \frac{V_L}{R_L} = \frac{L_r}{R_L}\frac{di_{Lr}}{dt}$$

$$i_{C_r} = C_r\frac{dv_{C_r}}{dt} = L_rC_r\frac{d^2i_{L_r}}{dt^2}.$$

Combining (8) and (9) and after some manipulations, the complete differential equation of the CFPPRI for one-half cycle is given by:

$$\omega^2{}_n\left(\frac{v_{in}}{L_{in}}t + \frac{L_r}{L_{in}}I_{L_r}(0) + I_{in}(0)\right) = i''_{L_r} + 2\alpha\cdot i'_{L_r} + \left(\omega^2{}_nK^2\right)\cdot i_{L_r} \qquad (10)$$

where $\omega_n = 1/\sqrt{L_rC_r}$ is the natural frequency, $\alpha = \omega_n/2Q$ is the damping coefficient, $Q = R_L/Z_r = R_L/\sqrt{L_r/C_r}$ is the quality factor and $K = \sqrt{1+L_r/L_{in}}$ is the error adjustment to the resonant frequency ($\omega_r = \omega_rK$) due to small input inductance value.

Solving (10) yields the expression for the resonant inductor current, $i_{Lr}(t)$:

$$i_{Lr}(t) = Ce^{-\alpha t}\cos(\omega_r t - \phi_1) + D_1t + D_0 \qquad (11)$$

where

$$C = \sqrt{A^2+B^2} \quad ; \quad \phi_1 = tg^{-1}\left(\frac{A}{B}\right)$$

$$B = i_{Lr}(0) - D_0 \quad ; \quad A = \frac{B}{2Q} - \frac{D_1}{\omega_r}$$

$$D_1 = \frac{v_{in}}{L_{in}}\frac{1}{K^2}\ ;\ D_0 = \left(\frac{L_r}{L_{in}}I_{Lr}(0) + I_{in}(0) - \frac{v_{in}}{L_{in}}\frac{1}{K^2}\frac{1}{\omega_rQ}\right)\frac{1}{K^2}.$$

Taking the derivative of (11) and multiplying by L_r will yield the capacitor voltage, $v_{Cr}(t)$:

$$v_{Lr}(t) = v_{Cr}(t) = L_r\frac{di_{Lr}}{dt} =$$

$$= L_r\left(-\alpha Ce^{-\alpha t}\cos(\omega_r t - \phi_1) + \omega_rCe^{-\alpha t}\sin(\omega_r t - \phi_1) + D_1\right) \qquad (12)$$

or

$$v_{Cr}(t) = L_r\left(Ee^{-\alpha t}\cos(\omega_r t - \phi_2) + D_1\right)$$

where

$$E = -\sqrt{(\alpha C)^2 + (\omega_r C)^2} \quad ; \quad \phi_2 = \phi_1 - tg^{-1}\left(\frac{\omega_r}{\alpha}\right).$$

Normalizing (11) by considering V_{in} and $Z_r = \sqrt{L_r / C_r}$ as the base values:

$$i_{Lr\text{-}pu}(t) = i_{Lr}(t)\frac{Z_r}{V_{in}} = \left(Ce^{-\alpha t}\cos(\omega_r t - \phi_1) + D_1 t + D_0\right)\frac{Z_r}{V_{in}} =$$

$$= C^* e^{-\alpha t}\cos(\omega_r t - \phi_1) + D_1{}^* t + D_0{}^* \qquad (13)$$

where

$$D_1{}^* = D_1\frac{Z_r}{V_{in}}\ ,\ D_0{}^* = D_0\frac{Z_r}{V_{in}}\ ,\ B^* = B\frac{Z_r}{V_{in}},$$

$$A^* = A\frac{Z_r}{V_{in}}, C^* = C\frac{Z_r}{V_{in}}\ ,\ \phi_1{}^* = \phi_1\frac{Z_r}{V_{in}}.$$

The normalized capacitor voltage is obtained by considering V_{in} as the base value:

$$v_{Cr\text{-}pu}(t) = v_{Cr\text{-}pu}(t)\frac{1}{V_{in}} = \frac{L_r}{V_{in}}\left(Ee^{-\alpha t}\cos(\omega_r t - \phi_2) + D_1\right)\frac{Z_r}{Z_r} =$$

$$= K\left(E^* e^{-\alpha t}\cos\left(\omega_r t - \phi_2{}^*\right) + \frac{K^2 - 1}{K^3}\right) \qquad (14)$$

where

$$E^* = -\sqrt{\left(\frac{C^*}{2Q}\right)^2 + \left(C^*\right)^2} \qquad ; \qquad \phi_2{}^* = \phi_1{}^* - \mathrm{tg}^{-1}(2Q).$$

Normalized input current:

$$i_{Lin\text{-}pu}(t) = i_{Lin}(t)\frac{Z_r}{V_{in}} =$$

$$\omega_n\left(K^2 - 1\right)\cdot t - \left(K^2 - 1\right)\left(i_{Lr\text{-}pu} - I_{Lr\text{-}pu}(0)\right) + I_{in\text{-}pu}(0). \qquad (15)$$

Continuous operation can be analyzed by considering the initial conditions of the next cycle as the last state of the previous one and repeating the calculations for the next cycle with the proper notation as was described above. Fig. 4 shows the normalized cycle-by-cycle waveforms of the CFPPRI for the case of switched load (numerical calculations were carried out by MATLAB 6).

Fig. 5 shows the output voltage sag due to a step perturbation of the load as a function of the quality factor for several inductors ratios. Fig. 6 shows the delay time till the overshoot maxima that occurs after a load step was applied.

The sensitivity of the CFPPRI to frequency deviation, due to interconnecting cable capacitances and load reactance, can be eliminated by incorporating a frequency tracking mechanism, along with a variable inductor and introduce a Self-Adjusting CFPPRI [1, 2] that will also provide the ability of driving the load with a predetermined frequency, controlled by the user.

3. THE SELF-ADJUSTING CURRENT-FED PUSH-PULL PARALLEL RESONANT INVERTER (SA-CFPPRI)

Since the details of the SA-CFPPRI were given earlier [2, 3], we present here only a brief description of this power source.

The SA-CFPPRI is built around a self-oscillating

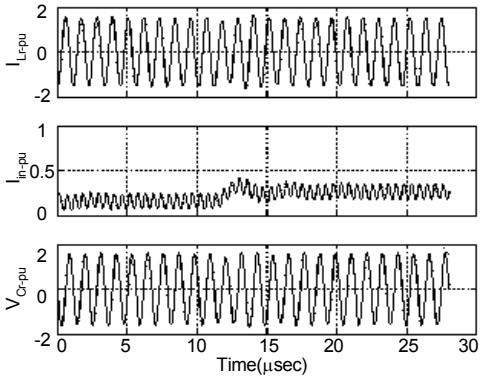

Figure 4. Cycle-by-Cycle step response waveforms, the load is switched form 100% to 60%.

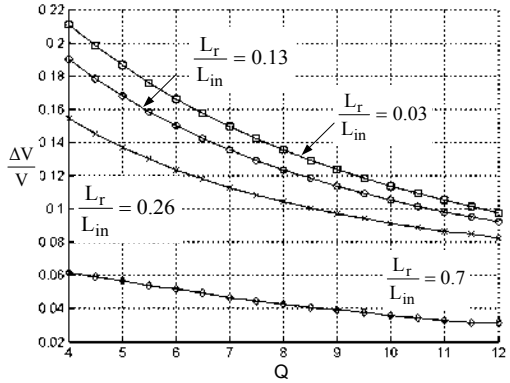

Figure 5. Output voltage sag for a 100% to 60% step of the load as a function of Q for several ratios of K (L_r/L_{in}).

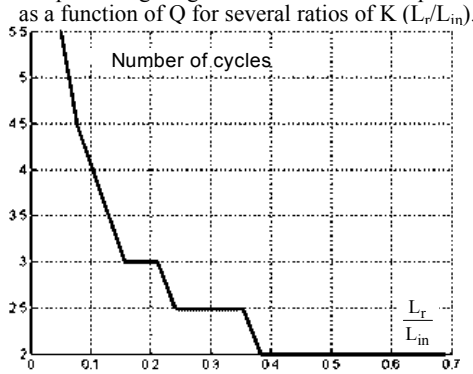

Figure 6. Number of switching cycles that passes from a step perturbation of the load to overshoot of the output voltage as a function of K (L_r/L_{in}).

inverter (Fig. 7) that comprises a Soft Switching Control (SSC) assembly. The SSC keeps the inverter at the resonant frequency by switching the drive whenever the center tap voltage (V_{tap}) reaches zero [5, 6]. When locked, the SSC ensures zero voltage switching of the SA-CFPPRI while the frequency of operation is determined by the equivalent capacitance and inductance of the resonant tank (L_r, C_2, C_3 and C_L). Frequency stabilization is obtained by a current controlled variable inductor T1 (Fig. 7). This current is stabilized, in present design, by a Buck type converter that operates in closed loop around the amplifier A1. Frequency tracking of the SA-CFPPRI is then assured by incorporating a phase comparator that

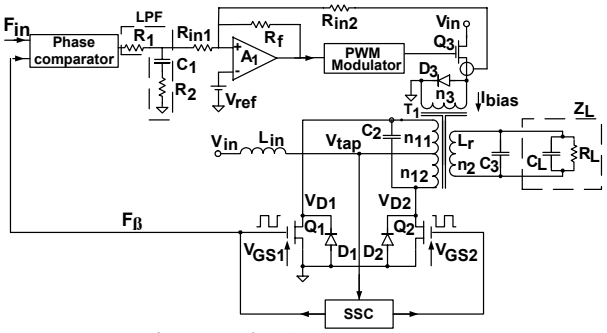

Figure 7. The SA-CFPPRI system.

generates an error signal as a function of the phase difference between the desired frequency F_{in} and the running frequency of the PPRI, F_{β}.

4. THE SA-CFPPRI PERFORMANCE UNDER SWITCHED LOAD CONDITIONS

A prototype SA-CFPPRI was previously simulated and tested experimentally for the ability to maintain a constant output signal under load changes [2, 3]. In this study we tested the performance of the SA-CFPPRI when connected to a switched load. The load circuit setup consists of two resistors connected in series while one of the resistors is paralleled with an IRF840 power MOSFET. The resistance values were chosen to cause a step in the output power from a full power of 5W (when the switch is turned on) to 60% of the full output power – 3W (when the switch is turned off). The target parameters of the experimental unit were: Input voltage: 11VDC; Output voltage: Vout = 160 Vrms; Load capacitance: C_L = 2.1nF; Output frequency: 93 kHz.

Fig. 8 shows the experimental response of the SA-CFPPRI to a 60% to 100% step in the output power. The output signal is stabilized after three HF cycles, a voltage dropout of 10% was measured at the first half cycle after the step was applied. No steady state error was observed.

5. DISCUSSION AND CONCLUSIONS

The SA-CFPPRI was shown to be able to keep a stable sinusoidal output signal even when the load power changes, and thus satisfies the demand of a power source for ac distributed power system bus. Another benefit of the proposed power source is the ability to maintain a constant output frequency when the connected to reactive loads.

The normalized analysis presented here, provide the designers a useful tool in designing and optimizing features of the HFAC bus driver and CFPPRI topologies when feeding switched loads.

The voltage sag was shown to be dependent on the quality factor (Q) inversely, that is, high Q will minimize the voltage sag. However, one should be aware that in a high Q system the reactive current that circulates in the

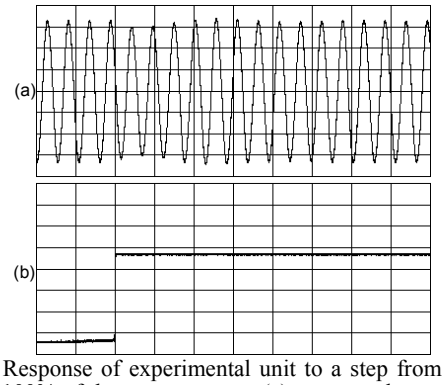

Figure 8. Response of experimental unit to a step from 60% to 100% of the output power. (a) output voltage, 70V/div and (b) V_{GS} of Q_L of Fig. 2, 5V/div ;horizontal scale: 20μs/div.

resonant tank would cause extra power losses.

The proposed topology is classified as underdamped system, since it is of high Q (Q>5). This implies that for a step perturbation of the load the CFPPRI will oscillate. However, the results of the present study show that the oscillations will be negligibly small compared to the signal, after the first overshoot occurs. That is, the settling time is practically equal to the delay until the first overshoot occurs.

Considering the above, the SA-CFPPRI as a HFAC bus driver provides the ability of hot-plug-in That is, loads may be taken in and out, while the driver the driver maintains a constant, sinusoidal supply signal.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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