Modular Design of APFC: A Feasibility Study

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Abstract - The feasibility of producing a modular Active Power Factor Correction (APFC) system was studied analytically and experimentally. It is shown that the novel control scheme that does not need the sensing of the input voltage is highly compatible with the modular concept. Modularity is achieved by aggregating practically all the electronic in an IC or hybrid unit that may also include the power switch. This unit plus a line rectifier, inductor and bus capacitor are all that it takes to form an APFC system. This plug and play solution will greatly simplify and reduce the cost of the design and manufacturing of APFC front ends.

I. Introduction

Conventional embodiment of CCM APFC systems [1] includes a controller that senses the input voltage and the line current (Fig.1). The shape of a rectified power line voltage, obtained via a divider comprised of resistors R_1 and R_2 from the input voltage V_{in}, is used as the reference for the desired shape of the input current. The controller also receives a signal that is proportional to the input current. The current level is adjusted for any given load by monitoring output voltage V_{out} via a divider comprised of resistors R_3 and R_4, and by multiplying the reference signal of the current control loop by the deviation from the desired outpu voltage level,

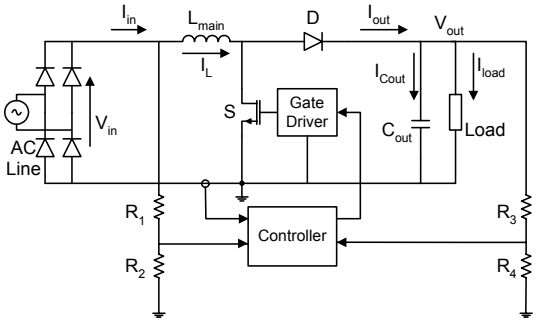

Fig. 1. Conventional CCM APFC approach.

so as to trim the effective reference signal to the load.

A major drawback of the conventional implementation of the APFC is the need for sensing the input voltage, namely the line voltage after rectification. Due to the switching effects, the input voltage is normally noisy and is susceptible to interference pick-up that may distort the reference signal and hence the input current. Also, the extra pin required for input voltage sensing will increase the number of pins of a modular device built in the conventional APFC scheme. Furthermore as experience engineers learned the hard way, designing an APFC system around a conventional controller is no easy task. Making the inner (current) loop stable is tricky and fighting the ground loops is exhausting.

Following the trend of “Smart Power”, it will be highly advantageous to have an APFC system of

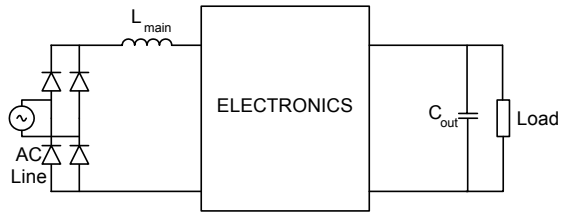

Fig. 2. Modular APFC approach.

a modular design in which all the electronics is packaged together in an IC or module (Fig. 2). This study investigated the feasibility of the "Smart Power" concept for an APFC switch/controller.

II. The control concept

Since the analysis of the control concept has been published earlier [2-4] we repeat here, for the sake of brevity, only the essentials. The proposed APFC method is based on the Boost topology operating in the Continuous Conduction Current Mode (CCM). The system (Fig. 3) includes a power stage and a control scheme that senses the input current and produces a Doff duty cycle proportional to the average value of this current. The outer loop is used to trim the proportionality constant (between the input current and Doff) to accommodate any given load. The principle of operation can be understood by considering the average model of Fig. 4 that represents the power stage (Fig. 4a) and its average model according to [5, 6].

Assuming that the circuit is stable (as will be shown below), this implies (Fig. 4b):

$$V_{in}(av) = D_{off} V_o(av) \qquad (1)$$

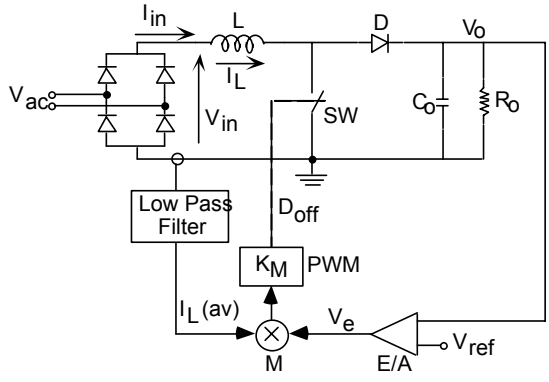

Fig. 3. Implementation of an APFC control scheme with no sensing of input voltage.

where D_{off} is (1-D_{on}), $V_{in}(av)$ is the average input voltage and $V_o(av)$ is the average output voltage. Averaging is over one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

Since the average input current $I_{in}(av)$ is equal to the average inductor current $I_L(av)$, equation (1) can be manipulated to the form:

$$\frac{V_{in}(av)}{I_{in}(av)} = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (2)$$

To make the input resistive with an input resistance R_e, we require:

$$\frac{V_{in}(av)}{I_{in}(av)} = R_e = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (3)$$

That is, a resistive input will be observed if D_{off} is programmed according to the rule:

$$D_{off} = \left(\frac{R_e}{V_o(av)}\right) I_L(av) \qquad 0 < Doff < 1 \qquad (4)$$

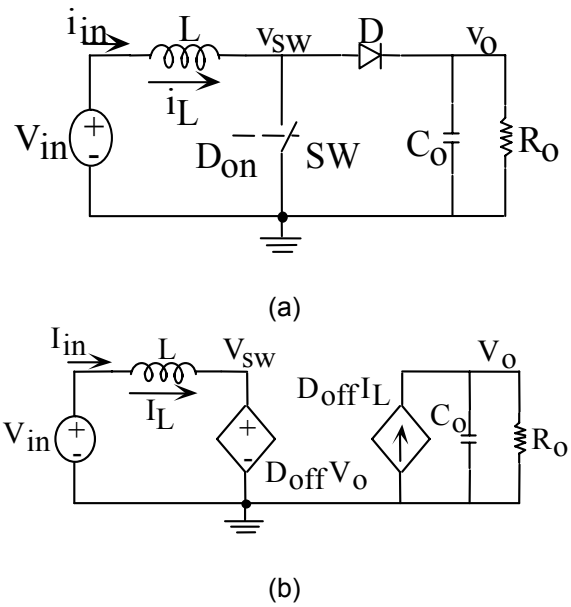

Fig. 4. The Boost converter (a) and its behavioural average model (b) (after [5,6]).

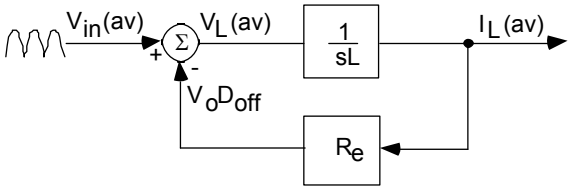

Fig. 5. Simplified block diagram of current control loop.

The stability of the circuit can be appreciated by considering the simplified block diagram of Fig. 5. In this control scheme the voltage imposed on the inductor (V_L) is equal to the input voltage minus the average voltage at the switch (Fig. 4b). The summing junction reconstructs the total voltage imposed on the inductor (L) while the feedback path represents the D_{off} programming according to (4). This block diagram representation assumes that the output voltage (V_o) is constant with negligible ripple and that R_e is set to a given constant value. Under these conditions, the system (Fig. 4) is linear and the loop-gain (βA) is found to be:

$$\beta A = (R_e)(\frac{1}{sL}) = \frac{R_e}{sL} \qquad (5)$$

which represents a bandwidth of $R_e/2\pi L$ and a phase margin of 90^0. This implies that the 'inner' current feedback loop is unconditionally stable for any input or output voltages - under the assumption that V_o is constant. But as the more analysis given below shows, this conclusion is also valid for practical cases.

The closed loop response (input current as a function of input voltage) is clearly:

$$\frac{I_L(av)}{V_{in}(av)} = \frac{1}{R_e}\frac{1}{1+s\frac{L}{R_e}} \qquad (6)$$

where $I_L(av)$ and $V_{in}(av)$ are the low frequency component of the inductor (and input) current and the low frequency component of the input voltage respectively. This result implies that the tracking bandwidth is $R_e/2\pi L$ as would be expected from (5).

In practical APFC applications for 50/60 Hz power line, the tracking bandwidth (BW_{Iin}) should be at least 1kHz [7] or, in general:

$$\frac{R_e}{2\pi L} = (BW_{I_{in}}) \qquad (7)$$

This constraint can now be checked against other design considerations and in particular the size of the inductor required to keep the current ripple within reasonable limits. Maximum ripple is reached at D_{on} = 0.5 that is when $V_{in}(av)$ = 1/2 $V_o(av)$. The ripple (ΔI) at this point will be:

$$(\Delta I)_{D_{on}=0.5} = \frac{V_{in}(av)}{2f_s L} \qquad (8)$$

where f_s is the switching frequency. The ripple ratio ($\Delta I/I_{in}(av)$) will be:

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\frac{V_{in}(av)}{2f_s L}}{\frac{V_{in}(av)}{R_e}} = \frac{R_e}{2f_s L} \qquad (9)$$

Combining (7) and (9) we obtain:

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\pi}{f_s}(BW_{I_{in}}) \qquad (10)$$

or:

$$(BW_{I_{in}}) = \frac{1}{\pi} f_s \left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} \qquad (11)$$

which implies that for a design of say $\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = 0.1$ (that is, maximum current ripple is 10% of the nominal current value), the tracking bandwidth will be about $f_s/30$. This is obviously more than enough for modern switch mode systems in which f_s>50kHz. For higher ripple ratios the bandwidth will be even larger.

It should be pointed out that the relevant term in (7) and hence in (11) is Re/L. This implies that the proposed APFC control scheme has a natural scaling capability. That is, in practice one would choose L to be proportional to Re (the equivalent input resistance that defines the

power level) and hence the loop gain will be the same for APFC stages designed for different power levels. This implies that there is no need to trim the phase compensation of the inner loop for each power level design. This makes possible the design of a universal controller that will fit power levels.

The dynamics of the proposed control scheme was thoroughly studied and already described in earlier publications [4]. For example, it was shown that the inner loop is well behaved (Fig. 6) and that a good current tracking is obtained over the required frequency range (Fig. 7).

To further explore the salient differences between the proposed approach and the 'classical' CCM implementation we compare the two when represented by a control-type block diagrams (Fig. 8). Only the parts associated with the current tracking are depicted. In each case there would be a need for an outer loop amplifier to keep the output voltage constant under variable operating conditions. The output of that error amplifier (V_{ev}) is used to drive the inner current loop. The two block diagrams are approximate. Both assume that the output voltage has no ripple component. We will also neglect here the ripple on V_{ev} and possible feedforward circuits [8, 9]. In the conventional control scheme shown in Fig. 8a, we recognize an inner current loop and a multiplier that generates the reference to the inner loop. The feedback loop is composed of two parts: the inductor that sees two opposing voltages, $V_{in}(av)$ and V_oD_{off} [5, 6] and a current error amplifier A_I. The latter is taken to include the modulator transfer function, sensing resistor and amplifier gain. The drive signal of this inner loop is a reference current I_{ref} which is generated by multiplying the rectified input voltage by the output of the outer loop error amplifier (V_{ev}). On the other hand, the proposed control scheme uses the input voltage $V_{in}(av)$ as the excitation signal of the inner current loop (Fig. 8b). In this case, the output of the outer loop operational amplifier (V_{ev}) modulates the effective input resistance (R_e). Nominal value is assumed to be R_{eo} and for any other operating condition V_{ev} will change the input resistance so as to keep V_o at the desired level. For the conventional control scheme (Fig. 8a) $V_{in}(av)$ is in fact a disturbance.

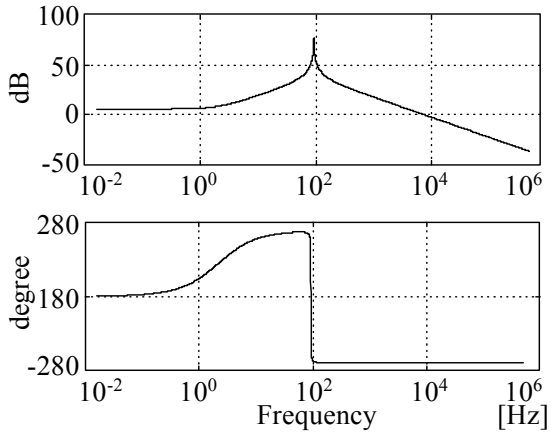

Fig. 6. Loop gain of the current control loop.

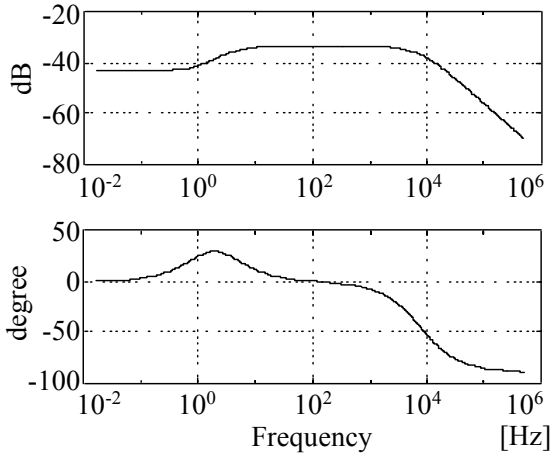

Fig. 7. Transfer function of the current control loop.

However, due to the high loop gain provided by A_I, which is built around an operational amplifier, the conventional current loop can suppress this disturbance as well as that caused by the output ripple. In the proposed control scheme (Fig. 8b), the magnitude of loop gain is evidently smaller (6), but if the interaction between the inductor L and output capacitor Co is taken into account (Fig. 6) one finds that the increase in the loop gain due to the passive components is rather significant. As it happens, practical value of L and C_o will have a resonant frequency around the low frequency range. A theoretical analysis of this question is beyond the scope of this paper.

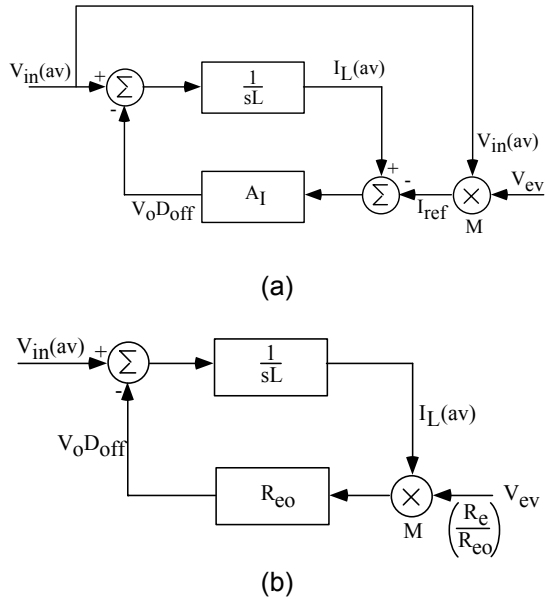

Fig. 8. Block diagram of a conventional (a) and proposed (b) power factor correction control.

But examination of practical examples clearly show that the resonant range is as pointed out. For example, a normal engineering choice is 1 mF for a 1kW APFC while the inductor will be in the range 0.5mH to 1mH for this power range (depending on the switching frequency). This will result in resonant frequency of 160 Hz.

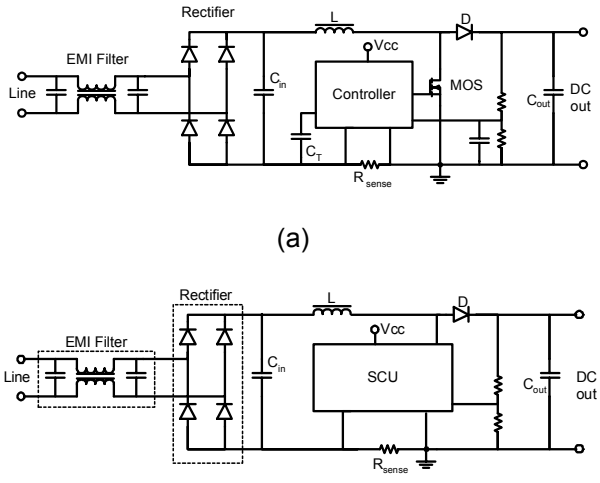

Fig. 9. Implementation of proposed control scheme is in a “discrete” form (a) and in an IC form (b).

Damping will move the resonant frequency somewhat but still, it is expected to be in the right range.

The high loop gain due to the passive resonant phenomena explains the excellent tracking and the rejection of the disturbance due to the output ripple. In the conventional case, the rejection is due to the high loop gain provided by A_I (Fig. 8a). But the high gain of the operational amplifier plus the extra phase shifts of the phase compensation network may deteriorate the phase margin. Furthermore, the introduction of a very high gain operational amplifier may render the system sensitive to switching noise. In the light of the above, it appears that the lack of an operational amplifier in the inner current loop is a significant advantage.

III. The modular approach

The proposed modular approach of the APFC is made possible by the following features of the concept:

1. No sensing of the input voltage is required. This reduces the number of pins and eliminates the interferences due to the noise that is typically found in conventional AFC approaches.
2. The dynamic robustness of the circuit that does not require trimming of inner loop per application.
3. The inherent current limiting capability stemming from the fact that a high input current will automatically increase Doff.

Based on these advantages the proposed control concept can be implemented in an APFC system based on a controller plus switch (Fig. 9a) or a Self Contained Unit (SCU) that includes both (Fig. 9b).

IV. Experimental

To explore the concept developed above, a prototype converter was built and tested in open and closed outer loop. The actual implementation (Fig. 10) included a PCB on which all the control components were placed. The tracking quality obtained experimentally is demonstrated by comparing the line current to the rectified input voltage (Fig. 11). The measured harmonics were low, easily complying with the EN61000-3-2 standard (Fig.12).

V. Conclusions

The present study suggests that the "Smart Power" approach to APFC construction is feasible and it can lead to great simplification of APFC system design and integration - to a "plug and play" level. For low power systems, the approach can lead to an APFC IC that will greatly simplify and reduce the cost of the APFC stage. An artist concept of possible implementations is shown in Fig. 13. One can thus conceive a line of devices that will cover the full power range of one phase applications (Fig. 14). Power Electronics designers will surely welcome such devices.

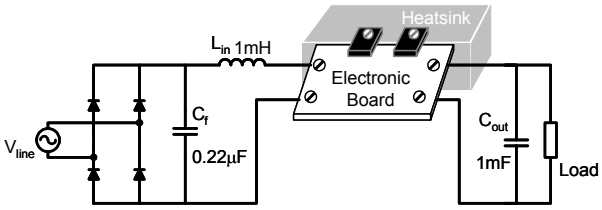

Fig. 10. Experimental set up.

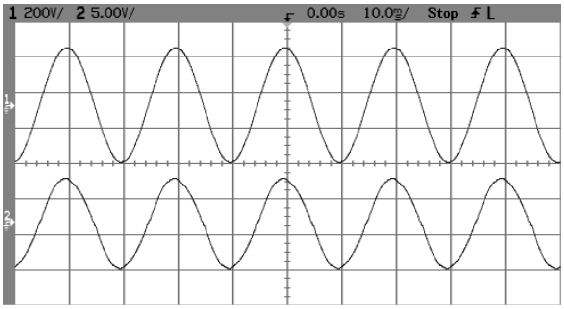

Fig. 11. Experimental results. Upper trace: line voltage (230V_{rms}). Lower trace: input current (5A/div). Horizontal scale: 10mS/div.

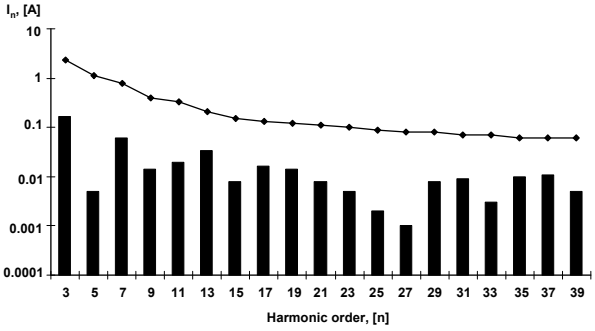

Fig. 12. Compliance with EN61000-3-2 standard at the 1kW level. Line: standard limits. Bars: measured harmonics. Notice the logarithmic scale.

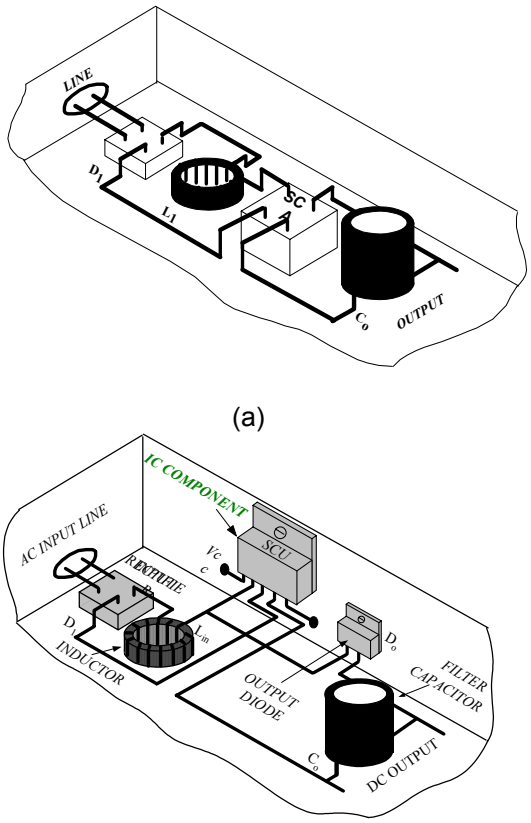

Fig. 13. Modular implementation of proposed APFC technology. (a) Hybrid. (b) IC, monolithic or multichip.

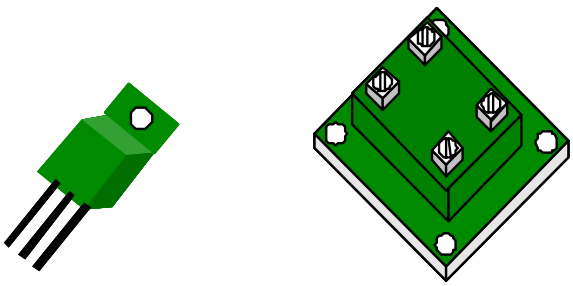

Fig. 14. Modular APFC products according to proposed APFC control.

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