A Novel Three-Phase Rectifier with Reduced THD

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Abstract- A high power three-phase rectifier that does not require a passive phase shifter (e.g. polyphase multi-winding transformer) was studied analytically and by simulation. The proposed rectifier includes 6 uni-directional switches and 24 diodes that are used to realize two three-phase bridges. The outputs of the bridges are connected in parallel via two blocking reactors. One of the bridges is operating with a positive phase delay of 15^{o} while the other is operated with a negative delay of 15^{o}. Analytical derivations, confirmed by simulation, predict that THD of the proposed rectifier's line current will be about 17% in a wide range of load currents. It is suggested that the proposed rectifier is advantageous in high power application.

1. Introduction

A number of methods for reducing the input current harmonics in three-phase rectifiers have been proposed in the past [1-10]. One of the approaches is the phase-shift family that is based on parallel or separate operation of rectifier bridges that are fed by a multi-winding polyphase transformer or auto-transformer [6-10]. A major drawback of such low frequency methods is the relatively large weight and size of the transformer or auto-transformer elements.

The rectifier topology proposed in this paper includes two rectifier bridges that operate in parallel. However, we eliminated the need for a multi-winding polyphase transformer or auto-transformer. Instead, 6 uni-directional switches (such as BJT, MOSFET, IGBT or GTO) and 24 diodes that are switched at low frequency accomplish the phase shift function. Since the low frequency transformers are eliminated, the weight and size of the high power rectifier will be much lower than in the traditional approaches.

II. The Proposed Topology of the Rectifier and Principle of Operation

The rectifier (Fig. 1) consists of two three-phase controlled bridges (Bg1 and Bg2) having a common input which is connected to the feeding ac network. The outputs of the rectifier bridges are connected in parallel via two blocking reactors (BL1 and BL2), the purpose of which is to reduce the interaction between the bridges. The load circuit (including resistor R_o and filter capacitor C_o) is connected between the center taps p1 and p2 of the blocking reactors, in series with a filter reactor L_o.

The principle of operation of proposed rectifier is described in this section under the following main assumptions: ideal switches and diodes, infinity high inductances L_o, BL1, BL2, ideal feeding ac network with zero inductance. Under these assumptions, the output current of the rectifier (I_o) does not include any ripple, there is no interaction between the two rectifier bridges and commutation processes within the rectifier bridges proceed instantly.

Voltage waveforms of the bridges are presented in Fig.2. The parameter ϑ is normalized time ($\vartheta=2\pi ft$, f is line frequency and t is the time), v_A, v_B, v_C are the phase input voltages, v_{g1}-v_{g6} are control pulses of the switches and v_{o1}, v_{o2} are the output voltages of the bridges.

Every switch is turned on twice during the line period (with the phase shift π) and duration of each control pulse is $2\pi/3$. One of the bridges (Bg1) is operating with a negative delay angle: $\alpha_1<0$, while the other one (Bg2) is operating with a positive delay angle: $\alpha_2>0$ (Fig. 2). Both delay angles have the same absolute value:

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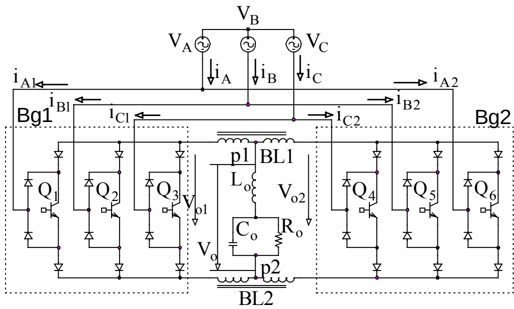

Fig.1. Topology of proposed rectifier.

$$|\alpha_1| = |\alpha_2| = \alpha \qquad (1)$$

The waveforms of the output voltages of the bridges v_{o1} and v_{o2} (Figs. 2,3) are indigenous to an elementary controlled rectifier.

The output voltage of the whole rectifier v_o (Fig. 3) is a function of v_{o1} and v_{o2}:

$$v_o = \frac{v_{o1} + v_{o2}}{2} \qquad (2)$$

The expression for average output voltage of the bridges and of the whole rectifier is the same as for the traditional three-phase bridge rectifier operating with the delay angle α:

$$V_{o.av} = \frac{3}{\pi} \int_{-\frac{\pi}{6}+\alpha}^{\frac{\pi}{6}+\alpha} V_m \cos\vartheta d\vartheta = 0.955 V_m \cos\alpha \qquad (3)$$

where V_m is the peak line voltage.

The waveforms of phase A input currents of the bridges (i_{A1} and i_{A2}) and of the whole rectifier (i_A) are presented in Fig. 4. The phase input currents of the bridges are rectangles with the duration $2\pi/3$ and with the height $I_o/2$, while the angle between the currents of the different bridges for the same phase is equal to 2α (Fig. 4). The sum of these currents is the line input current of the whole rectifier:

$$i_{A1} + i_{A2} = i_A \qquad (4)$$

Thus, the input current is a two-step symmetrical waveform where the duration of lower level is $2\pi/3+2\alpha$, while the superimposed higher upper step has a total duration of $2\pi/3-2\alpha$ (Fig. 4).

The rms values of the rectifier line input current and of its first harmonic (I_{rms} and $I_{(1)rms}$) were derived by analyzing waveform i_A (Fig. 4):

$$I_{rms} = I_o \sqrt{\frac{2}{3} - \frac{\alpha}{\pi}} \qquad (5)$$

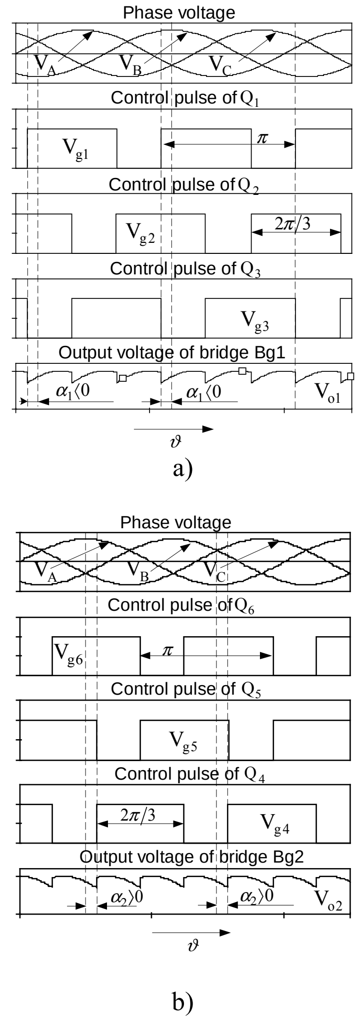

Fig.2. Voltage waveforms of rectifier bridges: (a) Bg1 and (b) Bg2.

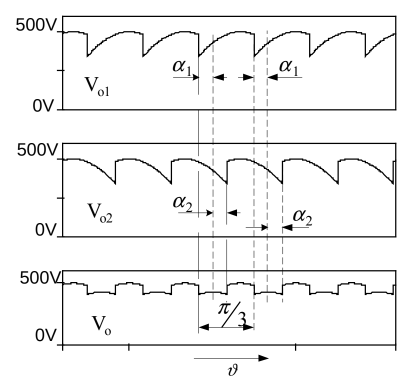

Fig. 3. The output voltage (v_o) as the average of the output voltages of the bridges (v_{o1}, v_{o2}).

$$I_{(1)rms} = \frac{2}{\pi}\sqrt{\frac{3}{2}}\, I_o \cos\alpha \qquad (6)$$

The total harmonic distortion can be expressed as:

$$THD = \frac{\sqrt{I_{rms}^2 - I_{(1)rms}^2}}{I_{(1)rms}} \qquad (7)$$

and from (5) , (6) and (7) we find:

$$THD = \sqrt{\frac{\pi^2}{6\cos^2\alpha}\left(\frac{2}{3} - \frac{\alpha}{\pi}\right) - 1} \qquad (8)$$

This function is plotted in Fig. 5. It implies that the minimum THD value (16.88%) corresponds to a delay angle α_{opt}=15^o which is therefore considered to be the optimal one.

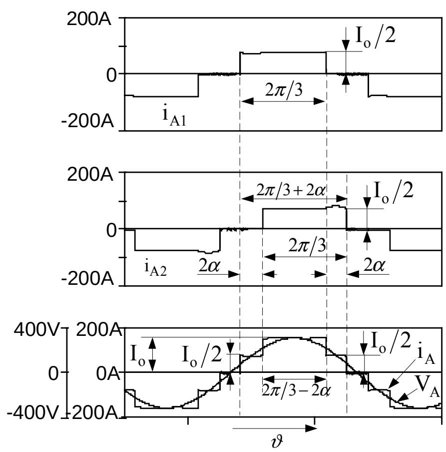

Fig.4. Line current (i_A) as the sum of phase currents of the bridges (i_{A1}+i_{A2}); v_A -voltage of the same phase.

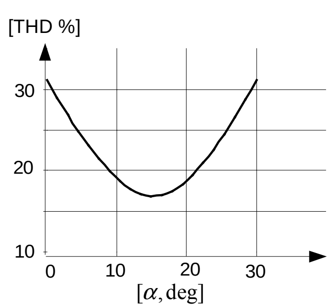

Fig.5. THD as a function of the delay angle α.

It should be noted that the expected THD_{min} is relatively high, but it is about twice lower than the THD corresponding to the basic three-phase (6-pulse) rectifier bridge (31.09%) and it is only 1.1 times higher than the THD corresponding to the traditional 12-pulse rectifier (15.23%).

III. THE EFFECT OF INTERACTION BETWEEN THE RECTIFIER BRIDGES ON THD

Under practical operating conditions, the inductances of the blocking reactors (BL1 and BL2, Fig. 1) have finite values. Therefore, interaction processes between the rectifier bridges will take place during the time intervals within the delay angles α_1 and α_2. During these periods, the external terminals of the blocking reactor BL1 or BL2 are connected through the conducting switches to different phases of the feeding ac network.

We consider the time interval $\vartheta_1\vartheta_2$ (Fig. 6) when the conducting switches Q_2 and Q_6 connect the left terminal of BL2 to the phase B and the right terminal of BL2 - to the phase A and when the phase voltage v_B is rising while the phase voltage v_A is decreasing. The middle of this interval, defined as ϑ=0, is the intersection instant of the waveforms v_A and v_B. The line input voltage v_A-v_B is described in this case by a simple equation:

$$v_A - v_B = -V_m \sin\vartheta \qquad (9)$$

and the boundaries of the interval will be at: ϑ_1=-15^o and ϑ_2=15^o.

Taking into account (9) we obtain from Kirchoff's low:

$$-V_m \sin\vartheta = X_s \frac{di_s}{d\vartheta} \qquad (10)$$

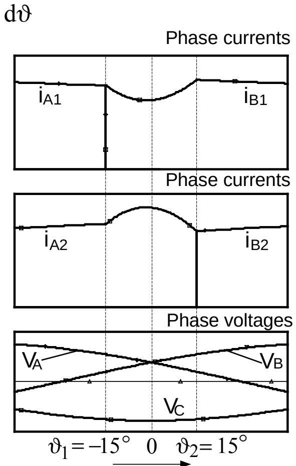

Fig. 6. Waveforms of phase currents of the first (i_{A1}, i_{B1}) and second (i_{A2}, i_{B2}) bridge when the interaction between the bridges is substantial; v_A, v_B, v_C - phase voltages.

where i_S is the circulating current flowing from the phase A of the bridge Bg2 into the phase B of the bridge Bg1 through BL2; $X_S=2\pi fL_S$ is reactance of the circulating circuit, i.e. it is practically the reactance of the blocking reactor including the effect of coupling between the two sections.

Integrating (10) and applying the initial conditions: $i_S=0$ at $\vartheta_1=-15^o$ and at $\vartheta_2=15^o$ results in the following expression for the circulating current:

$$i_S = \frac{V_m}{X_s}(\cos\vartheta - \cos 15^o) \quad (11)$$

The peak value of the circulating current corresponds to $\vartheta=0$:

$$I_{s.pk} = \frac{V_m}{X_s}(1-\cos 15^o) = \frac{0.034V_m}{X_s} \quad (12)$$

The average value of this current is found to be:

$$I_{s.av} = \frac{3}{2\pi}\int_{-\frac{\pi}{12}}^{\frac{\pi}{12}} \frac{V_m}{X_s}\left(\cos\vartheta - \cos\frac{\pi}{12}\right)d\vartheta = \frac{0.00567V_m}{X_s} \quad (13)$$

The circulating current i_S is added to the main component of the phase current of the "lagging" bridge Bg2 and is deducted from the main component of the phase current of the "leading" bridge Bg1 (Fig. 6). Therefore the lower steps of the waveforms of the rectifier input current will be convexed and concaved (Fig. 7) resulting in an increase of THD.

As a first approximation we assume that the main components of phase currents of "lagging" and "leading" bridges during the interval $\vartheta_1\vartheta_2$ by $L_o=\infty$ are equal to the average output currents of the bridges $I_{o1.av}$ and $I_{o2.av}$ and have identical values:

$$I_{o1.av}= I_{o2.av} = I_O/2 \quad (14)$$

where I_O is the output current flowing through the load resistance R_o

$$I_O = \frac{V_{o.av}}{R_O} \quad (15)$$

As (11) implies, the circulating current i_s does not depend on the load current I_o.

Applying (3), (12) and (15) we obtain:

$$\frac{I_o}{I_{s.pk}} = 27.1 * \frac{X_s}{R_o} \quad (16)$$

Hence, the larger is I_O, compared to $I_{S.pk}$ (i.e. the higher is X_s, compared to R_o), the weaker will be the harmful effect of $I_{S.pk}$ on the THD. This is shown in Fig. 8 which was calculated using the "Mathematica" [11] software (solid line) and was confirmed by PSPICE simulation [12] carried out for different values of R_o and X_s (dashed line). It is thus clear that the proposed rectifier will be more effective at high load currents I_o. The issue of the THD of the input current is further discussed in Section 4.

Now we remove assumption (14) and find the influence of the average circulating current $I_{s.av}$ on the average output currents of the rectifier bridges $I_{o1.av}$ and $I_{o2.av}$. The output characteristics of the bridges can be described by the equations:

$$V_{o1.av}=0.955V_m\cos\alpha - (I_{o1.av}-I_{s.av})R_s \quad (17)$$

$$V_{o2.av}=0.955V_m\cos\alpha - (I_{o2.av}+I_{s.av})R_s \quad (18)$$

where $V_{o1.av}$ and $V_{o2.av}$ are the average output voltages of the bridges and R_s is the resulting 'on'-resistance of the conducting switches and diodes. Taking into account that

$V_{o1.av}= V_{o2.av} =V_{o.av}$

$I_{o1.av} +I_{o2.av} =I_o$

we obtain from (17) and (18):

$$I_{o1.av} = \frac{I_o}{2} + I_{s.av} \quad (19)$$

$$I_{o2.av} = \frac{I_o}{2} - I_{s.av} \quad (20)$$

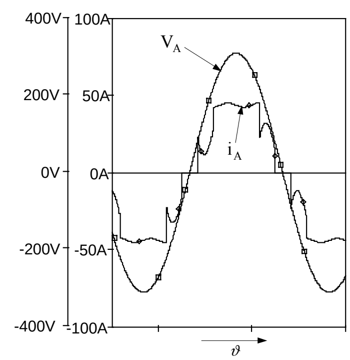

Fig. 7. The waveform of the line current of the rectifier (i_A) when the interaction between the bridges is substantial; v_A - voltage of the same phase.

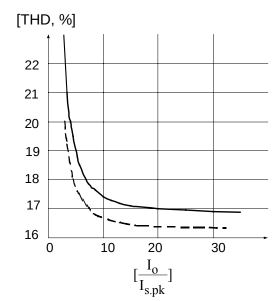

Fig. 8. THD as a function of the ratio between the load current I_o and the peak of circulating current $I_{S.pk}$: solid line-calculation results using "Mathematica" software, $L_O=\infty$; dashed line- PSPICE simulation results, L_o=0.4H, R_o=3 … 200Ohm, X_s=12.56 … 50.24 Ohm, V_m=537V.

We see that the average output current of the "leading" bridge ($I_{o1.av}$) is higher than $I_o/2$ and the average output current of the "lagging" bridge ($I_{o2.av}$) is lower than $I_o/2$. The difference between $I_{o1.av}$ and $I_{o2.av}$ is $2I_{s.av}$. Analyzing (12), (13), (16) and Fig. 8, we find that high $I_o/I_{s.pk}$ ratios are needed for achieving low THD,

$$2I_{s.av} << I_o \quad (21)$$

Under these conditions inequality of average output bridge currents is practically insignificant and therefore assumption (14) can be used in the design.

The influence of finite values of the output inductance L_o upon THD was studied by simulation (Fig. 9). Increase of L_o by a constant impedance ratio X_s/R_o provokes reduction of THD due decrease of the ripple of the current flowing through L_o. The plot (Fig. 9) can be used for the selection the ratios fL_o/R_o and X_s/R_o. It is seen that THD<17% can be obtained only for $fL_o/R_o<0.04$. By setting fL_o/R_o near this boundary, the ratio X_s/R_o should be higher than 0.5. The ratio X_s/R_o can be reduced up to 0.25 if $fL_o/R_o \approx 0.1$. Note that graphs (Fig. 9) corresponding to $fL_o/R_o=0.1$ and to $fL_o/R_o=\infty$ practically coincide. Therefore, the selection $fL_o/R_o>0.1$ is undesirable.

In practical cases, the inductance of the ac feeding network is not zero and therefore capacitor filter should be connected to the input terminals of the rectifier. This will help to achieve fast commutation processes within the bridges.

IV. HIGH-FREQENCY CHOPPERS AND CONVERTERS BASED ON THE PROPOSED RECTIFIER

The proposed rectifier (Fig. 1) could be easily transformed into a chopper to facilitate output voltage regulation. In this case, diodes D_{o1} and D_{o2} need to be connected between the output terminals of the rectifier bridges (Fig. 10). The chopping effect is achieved by driving the control gates of the switches by a high frequency PWM signal of a fixed duty cycle (D). In this case the output voltage will be

$$V_{o.av}=0.922DV_m \quad (22)$$

The simulations of the chopper (Fig. 10) were run for the following conditions: peak line voltage V_m=380V, line frequency f=50Hz, modulation frequency f_m=10kHz, duty cycle D=0.8, load resistance R_o=3Ω, capacitance of the output filter C_o=100uF, inductance of the output filter L_o=20mH, inductance of the blocking reactors (including the coupling effect) L_s=4mH.

The voltage and current waveforms of the simulation results are presented in Fig. 11. THD of the input current (up to the 90th harmonics) was found to be 16.63%. The normalized peaks of individual harmonics of the input current (relative to the peak of the first harmonic) were found to have the following values: $I_{(5)}$=8.99%, $I_{(7)}$=3.50%, $I_{(11)}$=7.08%, $I_{(13)}$=7.25%. Note that according to the standard IEC1000-3-4

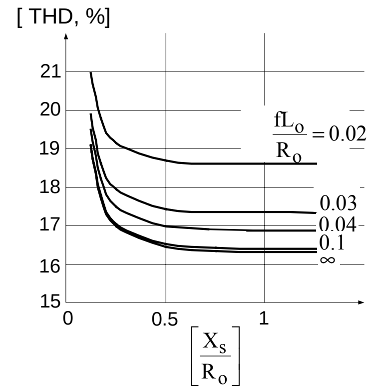

Fig. 9. THD of the phase current as a function of impedance ratios fL_o/R_o and X_s/R_o (simulation results).

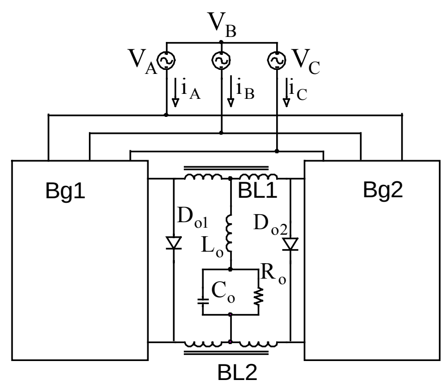

Fig. 10. High-frequency chopper based on proposed rectifier.

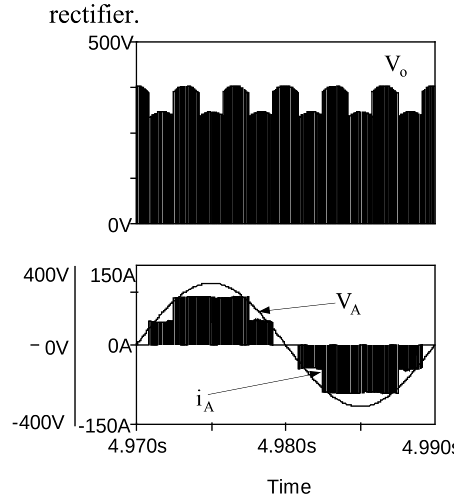

Fig. 11. Simulated voltage and current waveforms of the chopper (Fig. 10): v_O - output voltage of the rectifier, v_A - input voltage (phase A), i_A -input

the limits for a high power system (16-75A/phase) with a short circuit ratio R_{scc}=66, is as follows: THD=17%, $I_{(5)}$=12%, $I_{(7)}$=10%, $I_{(11)}$=9%, $I_{(13)}$=6%. Consequently, according to the simulation results the THD and individual harmonics of proposed rectifier comply with the standard requirements for R_{scc} >66.

V. Discussion and Conclusions

The proposed rectifier topology emulates the function of the 12-pulse rectifier by applying switches that are operated at twice the line frequency. The necessary phase shift is obtained by introducing delays in the two bridges. This arrangement eliminates the need for a polyphase transformer that is traditionally used to generate the 12 pulse waveforms. Replacing the filter inductor L_o by an active HF PWM converter can achieve further reduction in the size of the magnetics. The converter needs to be connected between terminals p1 and p2 of BL1 and BL2 (Fig.1) and could be of the Buck or Boost type. The control of the converter would be simple: it needs to be controlled as a constant current source. In this case the top of the phase current (Fig. 4) will be flat with a low inductance filter. More precise current waveform can be achieved by adding a feedback loop that will force the top of the current to follow the phase voltage.

The proposed rectifier was shown to reduce line harmonics to a THD level of about 17%. The basic topology will be especially beneficial in very high power applications where the size and weight reduction (as compared to the passive approaches) will be significant. Compatibility to very high power is further enhanced by the fact that the switches need to be operated at low frequency. Additional size reduction can be achieved by including a high frequency chopper or converter.

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