Generic Average Modeling and Simulation of Discrete Controllers

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Abstract **- A methodology is developed for average modeling of discrete controllers for PWM power conversion systems. The method applies a section of a transmission line to emulate the basic delay inherent to the discrete sampling and control algorithms. It is shown how the simple delay line model can be used to build an average model of a Zero Order Hold (ZOH) function that can be run on general purpose circuit simulator. The model is compatible with DC, AC (small signal) and time domain (large signal) analyses. The method is further demonstrated by developing an average model of a digital PID controller for a Boost converter and running large and small signal analyses of the closed loop system. Based on the proposed modeling and simulation approach, a procedure is suggested for the design of discrete controllers for switch mode systems.**

I. INTRODUCTION

The current proliferation of low cost microcontrollers and Digital Signal Processors (DSP), makes digital control of power conversion systems a reality that can not be overlooked. The new emerging digital capabilities call for the development of simulation tools to help expedite the adaptation of discrete control in switch mode power systems both in the research and industrial environments. Available simulation tools are either based on event simulation (e.g. MATLAB) or on continuous circuit simulation (e.g. PSPICE). Both methods apply, in principle, to large signal (time domain) analysis. However, classical control design methods in power electronics are still based on small-signal, frequency domain methods. Consequently, a simulation method for digital control applications should include the capability of frequency domain (small signal) analysis.

As was previously demonstrated [1] both large signal (time domain) and small signal (frequency domain) analyses of switch mode systems can be carried out in the MATLAB/SIMULINK environment. Applying the behavioral average modeling methodology on the power stage [1-5] and then extracting the state space equation of the resulting continuous model can accomplish this. This "average" state space presentation of the system can then be run in the MATLAB environment. However, many investigators and designers in the field find the SPICE environment more useful and friendly when it comes to simulation of power conversion systems. So it would be advantageous to have the capability of running AC analysis of digitally controlled power systems on a general-purpose circuit simulator.

The objective of the present study was to develop the methodology that will enable the simulation of digitally controlled power conversion systems on general-purpose circuit simulators such as SPICE derived packages. The main goal was to find a way to facilitate small signal (frequency domain) analysis so that issues of power stage transfer function, loop gain and phase margin can be easily and quickly examined. To achieve this, one has to translate the discrete sampling and delay functions into a continuous function and then model it by elements that are compatible with the simulators. By compatibility we mean the capability to carry out DC (steady state), large signal (time domain) and small signal (frequency domain) analysis without having to first derive the small signal transfer functions. This was accomplished in present study by describing the delay and Zero Order Hold (ZOH) functions by a continuous model built around a transmission line. The delay is the major reason for the discrepancy between the continuous control and discrete control schemes. The phase shift introduced by the delay may have a deteriorating effect on the closed loop system. This is one of the subjects that can be studied by simulation.

This paper describes the methodology for deriving a continuous model of the discrete delay and demonstrates its

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application in the simulation of a digitally controlled Boost converter operating in closed loop.

II. CONTINUOUS MODEL OF THE DISCRETE DELAY FUNCTION

The pure delay function (H_{delay}) is described by the Laplace transform expression:

$$H_{delay}(s) = e^{-sT_s} \qquad (1)$$

where T_s is the sampling period.

The term e^{-sT_s} represents pure delay and can be emulated by a section of a transmission line. The pure delay can be emulated by a delay line with a delay of T_s as shown in Fig. 1. The buffers at the inputs and outputs are used to avoid loading at the input side and to retain the matched 50Ohm loading of the delay line. Sampling period is put as parameter. For Fig. 1, the sampling rate is 10k Samples/Sec.

III. CONTINUOUS MODEL OF ZOH

The ZOH transfer function (H_{ZOH}) can be described by the Laplace transform expression:

$$H_{ZOH}(s) = \frac{1 - e^{-sT_s}}{sT_s} \qquad (2)$$

The numerator of (2) will thus be the original signal plus an inverted delayed signal. The denominator is an integration function. Consequently, the equivalent circuit of Fig. 2 can emulate (2). This average model of the ZOH function (ZOH-AVM) can then serve as a building block for describing in the continuous domain a digital controller. It is important to emphasize that the model of Fig. 2 is fully compatible to general-purpose circuit simulators. Furthermore, the model can be applied as-is in DC (steady state), TRAN (large signal, time domain) and AC (small signal, frequency domain) analyses.

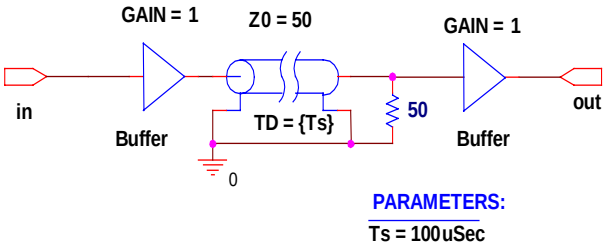


Fig. 1. Continuous equivalent circuit of a pure discrete delay.

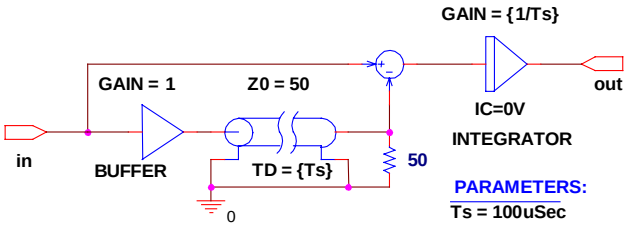


Fig 2. Average model of the ZOH function (ZOH-AVM).

The linearization, required for AC analysis, is done automatically by the simulator and is transparent to the user.

IV. DISCRETE PID CONTROLLER

One of the most popular control schemes used in power electronics is PID. It involves a proportional gain to increase the loop gain, a derivative term (a zero and hence phase advance) and an integration term (pole, phase lag). The discrete form (in Z transform) of the PID controller (H(z)) is thus:

$$H(z) = K_p + K_d \frac{1 - z^{-1}}{T_s} + K_i \frac{T_s}{1 - z^{-1}} \qquad (3)$$

where K_p, K_d and K_i are the proportional, differential and integral coefficients, respectively.

The transfer function H(z) is the ratio between the discrete output signal y(z) and the input signal x(z):

$$H(z) = \frac{y(z)}{x(z)} \qquad (4)$$

Substitute (3) into (4) and rearranging we get:

$$y(z)\left(1 - z^{-1}\right) = x(z) * \left[\left(K_p + \frac{K_d}{T_s} + K_i T_s\right) - \left(K_p + \frac{2K_d}{T_s}\right) z^{-1} + \frac{K_d}{T_s} z^{-2}\right] \qquad (5)$$

which translate into the difference equation:

$$y(n) = y(n-1) + \left(K_p + \frac{K_d}{T_s} + K_i T_s\right) x(n) - \left(K_p + \frac{2K_d}{T_s}\right) x(n-1) + \frac{K_d}{T_s} x(n-2) \qquad (6)$$

Applying the ZOH-AVM model we can now convert (6) into a SPICE compatible discrete PID block (Fig. 3).

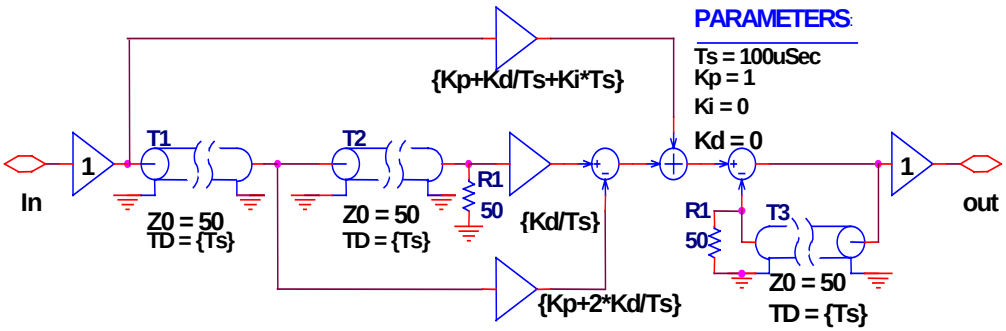


Fig 3. Digital PID Average Model (D_PID_AVM).

It should be pointed out that the average model of Fig. 3 is a continuous (analog) circuit that emulates the average behavior of the digital controller. In particular, it reproduces the phase shifts caused by the inherent delays of the digital PID algorithm. The realization of this model requires behavioral dependent sources and delay lines that are standard elements in all modern circuit simulators. Hence, the circuit is SPICE compatible in all respects. That is, it can be used to run DC, AC and TRAN analyses. Of particular interest is the small signal, frequency domain analysis (AC) that can be used to examine small signal transfer functions and as such to assist in the design of the controller. The usefulness of the circuit is enhanced by the fact that the circuit of Fig. 3 processes only the low frequency components and is blind to the switching frequency. This shortens considerably the simulation time.

By combining the behavioral model of the digital PID controller (Fig. 3) with the behavioral model of the PWM converter [1 – 5] one can easily test the performance of a switch mode converter in open and closed loop configuration. A pre-requisite to this is, of course, a complete design of both the power stage and the controller. That is, all the parameters of PID controllers (Fig. 3) need to be first evaluated. This could be done on a pure analytical basis or by applying a simulation assisted tuning procedure. The latter, which is proposed here, is quicker and easier to carry out in the industrial environment. The proposed methodology is based on two basic steps: (1) An approximate design in the frequency domain assuming that the controller is analog (opposed to a discrete controller). (2) Trimming the design by simulation while using the continuous model of the digital PID controller (Fig. 3).

V. ELEMENTS OF CONTROLLER DESIGN

The methodology proposed here is based on the notion that the system can be broken into two components, power stage A(f) and controller β(f), that are connected to form the close loop (Fig. 4). In this representation the power stage includes all the interfaces (PWM modulator, voltage divider) and internal feedback (peak or average current mode) if any. The objective of the controller design can be defined as follows. Given A(f), find β(f) such that the cross over frequency (of the loop gain) and the phase margin will be as specified. The problem can be represented in a convenient way by applying the A(f) and 1/ β(f) Bode plots [6]. In this case (Fig. 5), the A(f) plot is kept constant while the 1/ β(f) plot is adjusted so as to obtain the desired cross over frequency and phase margin. Crossover frequency is at the intersection of the two plots while the phase margin is the phase of βA when βA=1.

The proposed computer aided design of a controller is based on behavioral simulation. To this end the model of the power stage and interfaces need to be extracted [1-5]. Next, there is a need for a first guess of the controller. And finally, a plot similar to Fig. 5 is generated by simulation and the controller is tuned to achieve the target cross over frequency and phase margin. In the case on hand (digital PID) controller, we start by guessing the parameters of an analog PID controller.

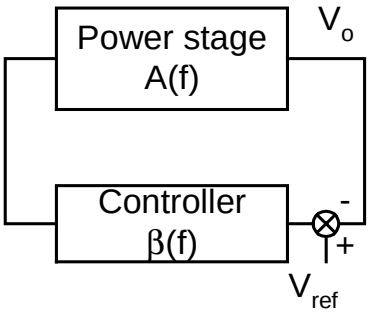


Fig. 4. Basic feedback loop in switch mode converters.

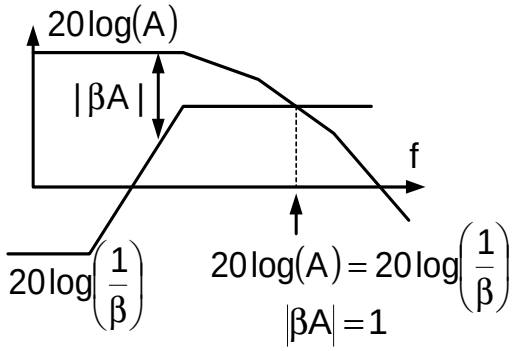


Fig. 5. Bode plot design of loop gain based on a fixed A(f) and adjustable 1/β(f)

VI. THE ANALOG PID CONTROLLER

The PID continuous equation is defined as:

$$H(s) = k_p + k_d s + k_i \frac{1}{s} \tag{7}$$

By replacing s by jω one gets the frequency domain presentation:

$$H(\omega) = k_p + k_d j\omega + k_i \frac{1}{j\omega} \tag{8}$$

For low frequencies where $\omega << \frac{k_p}{k_d}$ we can approximate $H(\omega)$ by:

$$H_l(\omega) \cong \frac{k_i\left(1+\frac{j\omega}{\omega_{z1}}\right)}{j\omega} \tag{9}$$

where

$$\omega_{z1} = \frac{k_i}{k_p} \tag{10}$$

For high frequencies where $\omega >> \frac{k_i}{k_p}$ we can approximate $H(j\omega)$ by

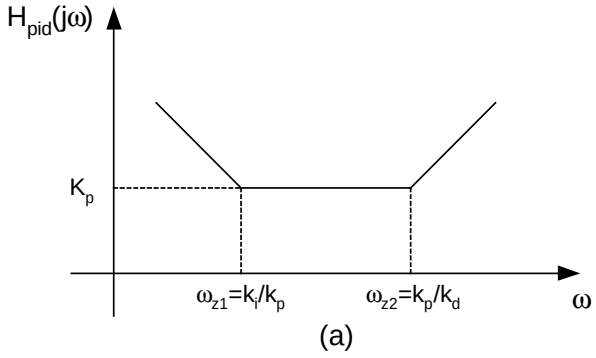
$$H_h(j\omega) \cong k_p\left(1+\frac{j\omega}{\omega_{z2}}\right) \tag{11}$$

where

$$\omega_{z2} = \frac{k_p}{k_d} \tag{12}$$

For cases where $\omega_{z1} < \omega_{z2}$, the Bode diagrams will have the form shown in Fig 6a. In cases where $\omega_{z2} < \omega_{z1}$, the Bode diagram will have the form as shown in Fig. 6b.

Based on the above observation the suggested starting point, for the design of the analog PID controller, is as follows. First we obtain by behavioral average simulation the small signal transfer function of the power stage [1-5]. We then assume that the intersection of the power stage plot A(f) and the controller 1/β(f) plot is as shown in Fig. 7a, in this case $1/\beta(f) = 1/H_{pid}(\omega)$. The target cross over frequency is ω_c. For this case the gain at the flat top of $1/H_{pid}(\omega)$ is $1/k_p$. By this we extract the initial value of k_p. We then choose ω_{z2} to be equal to ω_c and fix ω_{z1} one decade lower that ω_c to avoid additional phase shift due to the pole at the origin (see Fig. 7a). Once these initial parameters are extracted, they are inserted in the **digital** PID model and the loop gain of the system (power stage plus controller) is examined and tuned by simulation. Note that the digital PID will add some phase shift so the final A(f)-1/β(f) plot (Fig. 7b) may be different from the initial one (Fig. 7a). The proposed guidelines for adjusting the PID controller are as follows. By moving ω_{z2} to the left (toward lower frequencies) while still keeping the crossover frequency at ω_c we can increase the phase margin and hence improve stability. Moving ω_{z1} to the right (higher frequencies) will increase the low frequency gain but will



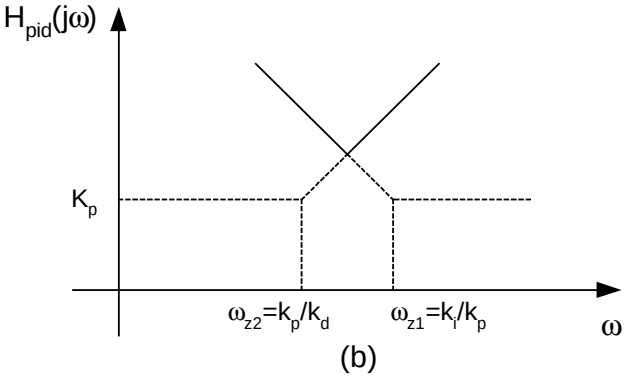


Fig 6. Bode diagrams of PID controller. (a) For $\omega_{z1}<\omega_{z2}$.. (b) For $\omega_{z2}<\omega_{z1}$.

deteriorate the phase margin due to the added phase delay. Therefore, this adjustment should be accompanied with a shift to the left of ω_{z2}. The tuning can be accelerated by applying the 'performance analysis' tool. With this procedures (that is available in modern circuit simulators) the locations of the break points can be automatically stepped over a given range while the AC analysis is repeated for each selection. The final Bode diagrams could look like the one shown in Fig. 7b. In this case we assumed a second order system (a slope of –40db/dec) and that the controller is providing a phase advance to the feedback loop. This procedure was used to tune the digital PID controller of a Boost converter discussed below.

VII. BEHAVIORAL AVERAGE MODEL OF DIGITALLY CONTROLLED BOOST CONVERTER

We applied the proposed tuning procedure on a benchmark Boost converter described in [7]. Fig. 8 (in PSPICE presentation) is a circuit diagram of the switched Boost converter. This circuit is applicable for time domain analysis (so-called cycle-by-cycle) only and is used as a reference circuit. The block U1 is a detailed circuit of a PWM modulator including ramp generator, comparator etc.

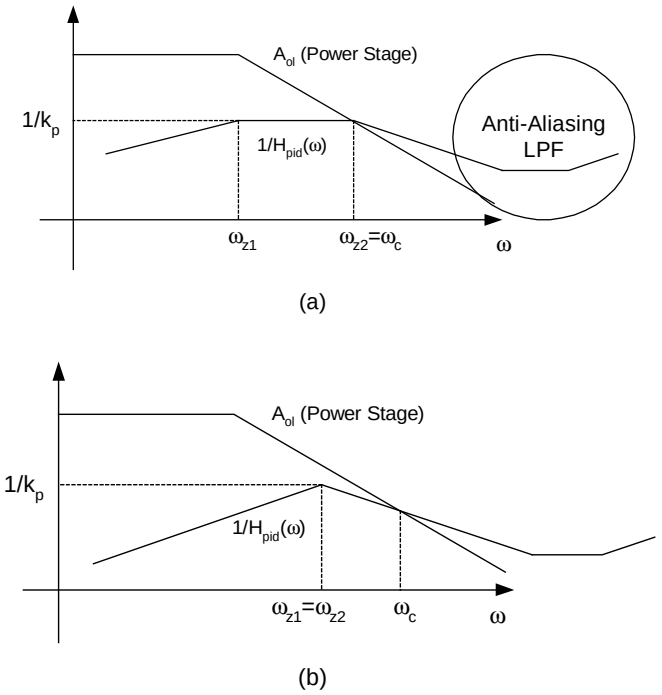


Fig 7. Suggested design steps for the digital PID. (a) Starting point. (b) Final (optimized) point.

U2 is a complete time domain realization of a digital PID controller including the full circuit of a ZOH (Fig. 9). In Fig. 8 we use an ideal switch S2 that is run at a switching frequency of 25KHz [2]. Switch S1 is used to test the dynamic response under a step load change.

Applying the methodology of behavioral modeling and simulation [1-5] and the proposed continuous model of the digital PID, we can now build a SPICE compatible behavioral model of the Boost system (Fig. 10). In this circuit we have included an extra summing point for the small signal excitation V3. This is used to examine the loop gain (magnitude and phase), which is equal to v_o/v_f (see nodes in Fig. 10).

The average model of Fig. 10 is fully compatible with general-purpose circuit simulators and can be used as-is to run not only DC and transient analysis but also AC analysis.

VIII. SIMULATION RESULTS

The performance of the ZOH-AVM (Fig. 2) was checked by simulation against the discrete time domain analysis of the ZOH function realized by a switch S3 (see Fig. 9). The results (Fig. 11) show that the response of the average model is indeed a smooth average of the stepped ZOH function.

The capability of the average model to carryout AC (small signal) analysis is demonstrated in Fig. 12 which is the loop gain (amplitude and phase) of the average model of Fig. 10. As can be seen, in this particular voltage mode control PID design, the cross over frequency is 197Hz and the phase margin is 49^0.

Comparison between the switched circuit simulation (cycle-by-cycle) and the average circuit simulation for a load step is shown in Fig. 13. The first portion of the traces is a power-on transient in which a relative large deviation is observed between the two simulation runs. Around the operating point the disagreement is rather small.

IX. DISCUSSION AND CONCLUSIONS

The average modeling methodology was found to emulate to a practical degree the behavior of a digitally controlled Boost converter. Following the procedure described here, the method could be applied to any PWM topology. Although the degree of matching between complete (switched) time domain simulation and average simulation was not found to be perfect, average simulation can still be useful as an initial tool to approach the design goals of the digital controller. It is therefore concluded that the proposed simulation approach could ease and accelerate the design stages of a digital controller for switch mode power systems.

The suggested procedure of a discrete controller design will involve:

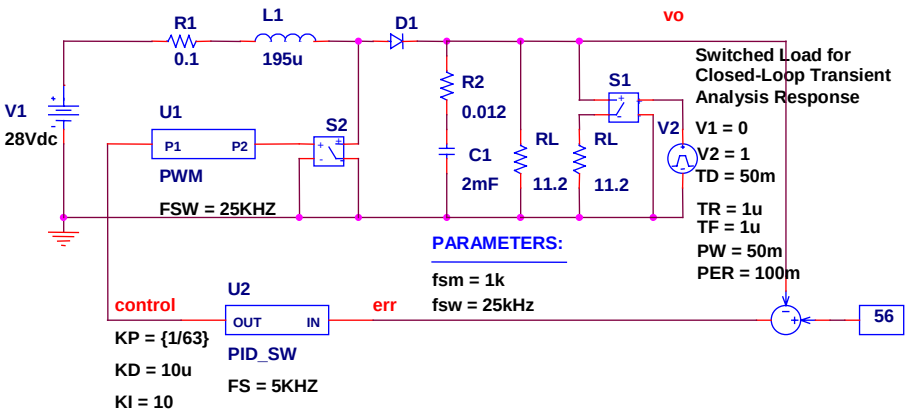


Fig 8. Schematics (PSPICE compatible) of a switched Boost converter [2] with digital PID control (including sample and hold). Sampling period $T_s=1/F_S=$ 200uS.

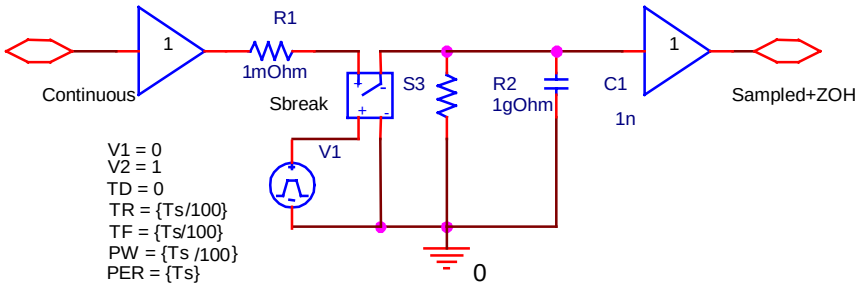


Fig 9. Switched ZOH model.

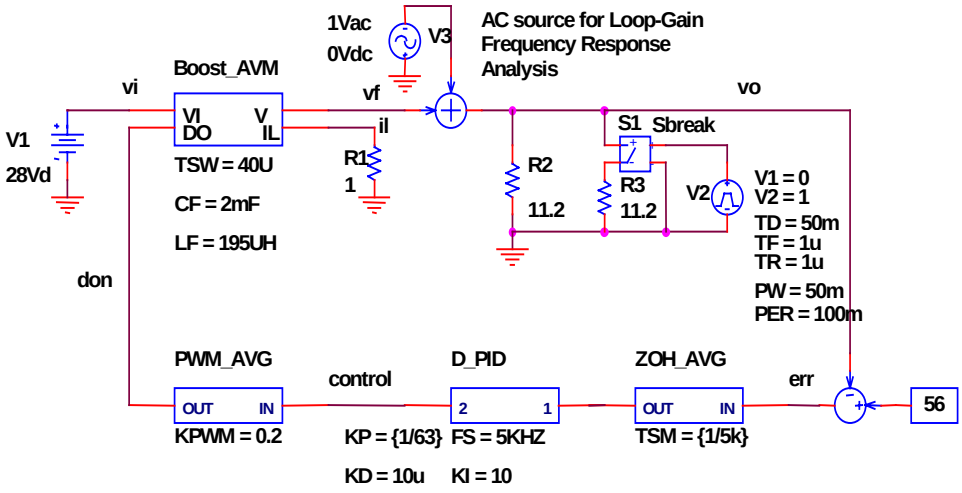


Fig 10. Behavioral model of the digitally controlled Boost converter shown in Fig.8.

1. Extracting the small signal response of the power stage by AC analysis of the average model of converter.
2. Designing a first guess continuous controller in the frequency domain.
3. Translating the continuous controller to a discrete controller.
4. Simulating the loop gain of digitally controlled power stage by the proposed average modeling method.
5. Examining by simulation the cross-over frequency and phase margin.
6. Applying average simulation to trim the digital controller for the desired performance in terms of cross over frequency and phase margin.

Following the concepts discussed here, continuous model of other digital control methods could be easily developed. The modeling concept is applicable to single state-space variable feedback (voltage mode) and to the two state-variable feedback (current mode).

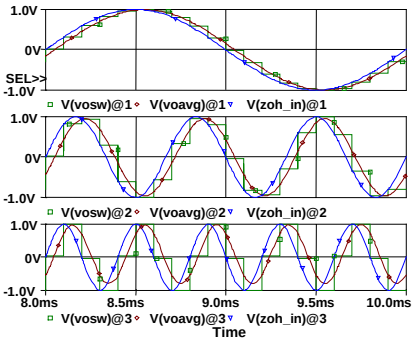


Fig 11. Typical waveforms of ZOH-AVM as compared to discrete ZOH for three different frequencies: 500Hz, 1.5kHz and 2.5kHz. Input voltage: continuous, leading. Output of discrete ZOH: stepped. Output of ZOH-AVM: continuous, lagging.

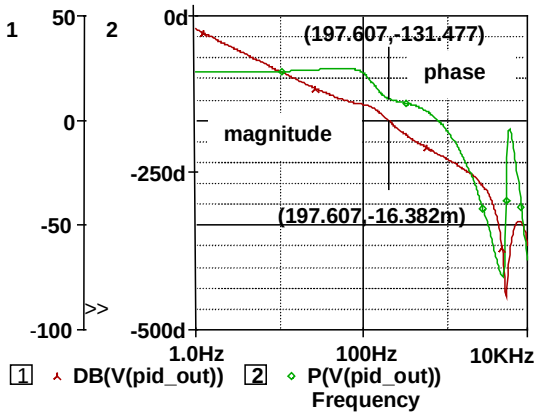


Fig. 12. Open loop frequency response of Boost converter with digital PID control as obtained by average simulation.

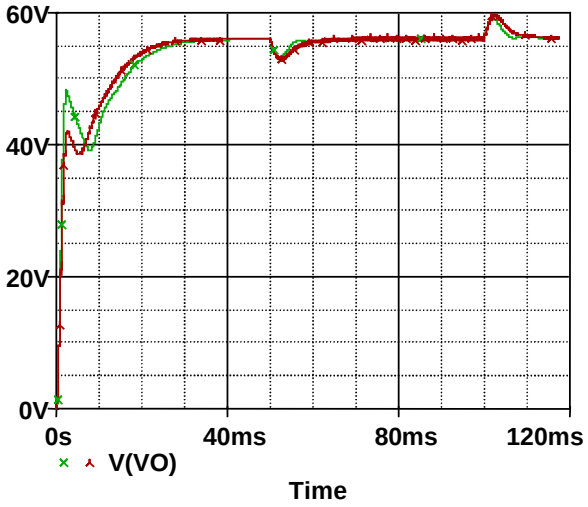


Fig. 13. Time-domain dynamic response of switched (stars) and averaged (crosses) simulation of the closed loop Boost converter.

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