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THE DYNAMICS A PWM BOOST CONVERTER WITH RESISTIVE INPUT

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Abstract - An average modeling methodology is proposed for deriving PWM programming rules that cause DC-DC converters to look resistive at the input terminals. The proposed approach was verified by average and cycle-by-cycle simulation. The study investigated the large and small signal response issues and in particular the inner loop gain and outer loop response. It is demonstrated that the proposed method can be useful in the design of robust Active Power Factor Correctors with low THD.

I. INTRODUCTION

The current interest in Active Power Factor Correction (APFC) [1-6] prompts investigators to look for improved methods to shape the input current of PWM converters. Two groups of solutions have been proposed hitherto: those that rely on direct current feedback [2] and those that apply indirect input current control [3-5]. Here we present an average modeling methodology that can help to derive indirect control schemes for input current shaping of PWM converters. The average models developed are then used to study the large and small signal responses of a Boost converter applied in APFC application.

II. THE BOOST TOPOLOGY

The proposed methodology will first be described by a simple intuitive reasoning in relation to the Boost converter (Fig. 1a). It is assumed that the converter is driven by a duty cycle D_{on} and that it operates under Continious Conduction Mode (CCM) conditions. As shown previously [7, 8], the function of the converter can be represented by the behavioral model of Fig. 1b. One can now apply a power circuit theory corollary: under stable conditions, the average voltage across a power inductor L must be zero (otherwise the current will rise to infinity).

Assuming that the circuit is stable (as will be shown below), this implies (Fig. 1b):

$$V_{in}(av) = D_{off} V_o(av) \qquad (1)$$

where D_{off} is $(1-D_{on})$, $V_{in}(av)$ is the average input voltage and $V_o(av)$ is the average output voltage. Averaging is over one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

Since the average input current $I_{in}(av)$ is equal to the average inductor current $I_L(av)$, equation (1) can be manipulated to the form

$$\frac{V_{in}(av)}{I_{in}(av)} = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (2)$$

To make the input resistive with an input resistance R_e, we require:

$$\frac{V_{in}(av)}{I_{in}(av)} = R_e = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (3)$$

That is, a resistive input will be observed if D_{off} is programmed according to the rule:

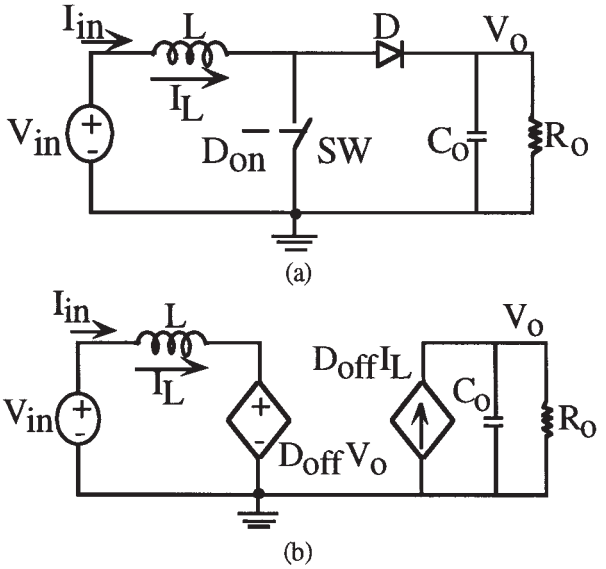

Fig. 1. The Boost converter (a) and its behavioral average model (b) (after [7,8]).

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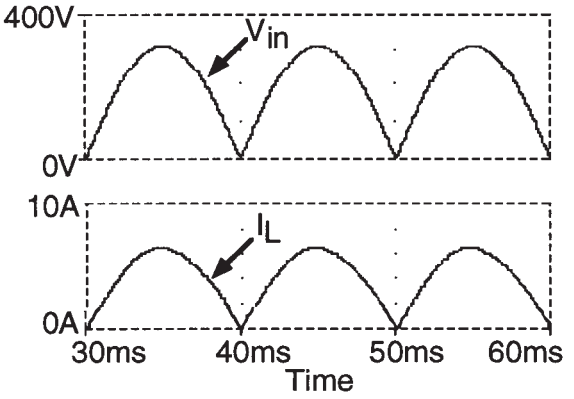


Fig. 2. Results of average simulation of proposed control on the behavioral model of Fig. 1b.

$$D_{off} = \left(\frac{R_e}{V_o(av)}\right) I_L(av) \quad , \quad 0 < D_{off} < 1 \qquad (4)$$

It should be noted that this relationship introduces negative feedback and hence helps to insure stable operating conditions (as is shown in the more rigorous analysis given below).

The control concept of (4) was tested by running a behavioral SPICE simulation [7, 8] on the model of Fig. 1b. The results presented in Fig. 2 are for a typical 1kW APFC stage. D_{off} was set according to (4), $\left(\frac{R_e}{V_o(av)}\right)$ was $0.127A^{-1}$, $V_{in}(av)=|310\sin(2\pi 50t)|$ (Volts), where t is time (Sec). Other parameters were: $R_o=144\Omega$, $C_o=1000\mu F$, L=1.1mH. The system reached a steady state output voltage of 380V while the input current clearly demonstrates the resistive nature of the converter's input terminals (Fig. 2).

In active power factor correction systems V_o need to be stabilized and R_e adjusted as a function of the load voltage and input current. One possible way to achieve this is proposed in Fig. 3. The voltage error amplifier (E/A) should have a slow response so as not to react within the mains cycle. The multiplier (M) generates the programmed voltage that is modulated by the PWM modulator to obtain D_{off}. This control scheme was tested by a PSPICE (Microsim Co.) cycle-by-cycle simulation. The parameters of the power stage and modulator were as given above. The bandwidth of the error amplifier (E/A) was 10 Hz, switching frequency: 50kHz, bandwidth of low pass filter (Fig. 3a): 80kHz. The simulation results (Fig. 3b) clearly demonstrate the validity of the approach.

III. DYNAMIC RESPONCE

1. Current tracking: approximate analysis

The dynamic response of the proposed converter can be studied by the simplified control block diagram presented in Fig. 4 which describes the left mesh of Fig. 1b. The summing junction reconstructs the total voltage imposed on the inductor (L) while the feedback path represents the D_{off} programming according to (3), (4). This block diagram representation assumes that the output voltage (V_o) is constant with negligible ripple and that R_e is set to a given constant value. Under these conditions, the system (Fig. 4) is linear and the loop-gain (βA) is found to be:

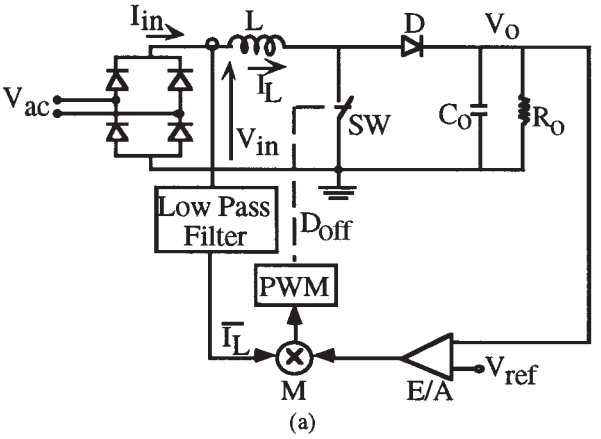
$$\beta A = (R_e)\left(\frac{1}{sL}\right) = \frac{R_e}{sL} \qquad (5)$$

which represents a bandwidth of $R_e/2\pi L$ and a phase margin of 90^0. This implies that the 'inner' current feedback loop is unconditionally stable for any input or output voltages - under the assumption that V_o is constant. But as the more analysis given below shows, this conclusion is also valid for practical cases.

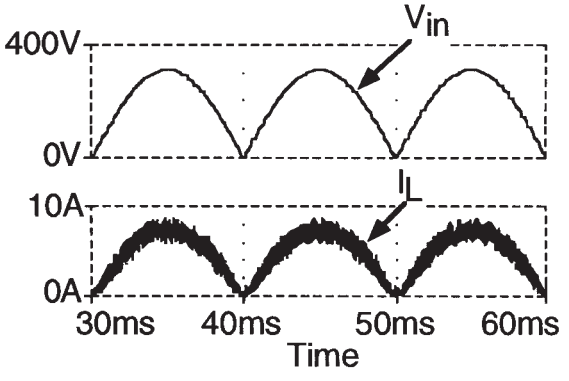
The closed loop response (input current as a function of input voltage) is clearly:

$$\frac{I_L(av)}{V_{in}(av)} = \frac{1}{R_e}\frac{1}{1+s\frac{L}{R_e}} \qquad (6)$$

where $I_L(av)$ and $V_{in}(av)$ are the (low frequency component) inductor (and input) current and the (low frequency



(a)



(b)

Fig. 3. Possible realization of proposed control method (a) and results of cycle-by-cycle simulation of its performance (b).

component) input voltage respectively. This result implies that the tracking bandwidth is $R_e/2\pi L$ as would be expected from (5).

In practical APFC applications for 50/60 Hz power line, the tracking bandwidth (BW_{Iin}) should be at least 1kHz [10] or, general:

$$\frac{R_e}{2\pi L} = (BW_{I_{in}}) \tag{7}$$

This constraint can now be checked against other design considerations and in particular the size of the inductor required to keep the current ripple within reasonable limits. Maximum ripple is reached at D_{on} = 0.5 that is when $V_{in}(av) = 1/2\ V_O(av)$. The ripple ($\Delta I$) at this point will be:

$$(\Delta I)_{D_{on}=0.5} = \frac{V_{in}(av)}{2f_s L} \tag{8}$$

where f_S is the switching frequency. The ripple ratio ($\Delta I/I_{in}(av)$) will be:

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\frac{V_{in}(av)}{2f_s L}}{\frac{V_{in}(av)}{R_e}} = \frac{R_e}{2f_s L} \tag{9}$$

Combining (7) and (9) we obtain

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\pi}{f_s}(BW_{I_{in}}) \tag{10}$$

or:

$$(BW_{I_{in}}) = \frac{1}{\pi} f_s \left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} \tag{11}$$

which implies that for a design of say $\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = 0.1$, the tracking bandwidth will be about $f_S/30$. This is obviously more than enough for modern switch mode systems in which f_S>50kHz. For higher ripple ratios the bandwidth will be larger.

Bandwidth limitation might be a problem only when the input inductor becomes very high. But this is also the case in conventional CCM APFC [11]. It is also interesting to note that the inner current loop bandwidth is linear with R_e (7). Hence, when the load power drops and hence R_e becomes larger, the possible bandwidth gets in fact larger. That is, once designed for maximum output power, tracking is assured for lower power levels as long as CCM is maintained. Hence, in most applications applying the proposed control scheme, the inner loop bandwidth will have to be limited in order to avoid subharmonic instabilities.

The analysis of Discontinuous Current Mode (DCM) operation is beyond the scope of this paper and will be discussed in a subsequent publication.

2. Current tracking: small signal response

A more rigorous analysis of the current tracking raises two issues: (a) for a finite output capacitor V_O can not be assumed to be constant and (b) for a nonconstant V_O the system is nonlinear. To overcome these problems the system was linearized around a given operating point by differentiating the average model of Fig. 1b [9]. The inner loop gain was derived by the model shown in Fig. 5 in which all the DC values (e.g. V_{in}) were subtracted. The loop gain is obtained under the assuming that d_{off} drives the system is an independent variable and then calculating the dummy dependent variable d'_{off}. The inner (current) loop gain (βA) is thus equal to d'_{off}/d_{off} (Fig. 5). Following this method, the inner loop gain was found to be:

$$\beta A = \frac{sC_oR_oR_e + R_e + D_{off}^2 R_o}{s^2 LC_oR_o + sL + D_{off}^2 R_o} \tag{12}$$

where capital D_{off} denote the steady state values.

For C_O-> ∞ the function reduces to (5) found earlier for the case V_O = constant.

The exact solution of the loop gain (12) includes a zero (f_Z) at :

$$f_z = \frac{1}{2\pi}\left(\frac{1}{C_oR_o} + \frac{D_{off}^2}{C_oR_e}\right) \tag{13}$$

and a complex pole (f_p) at:

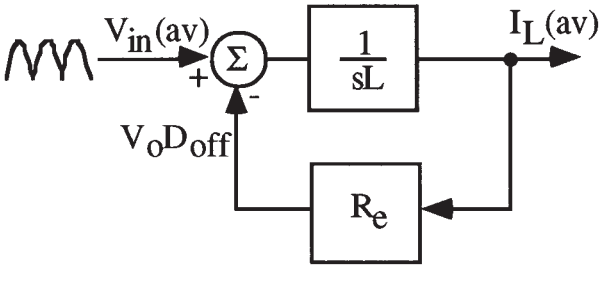


Fig. 4 . Simplified block diagram of proposed APFC control scheme.

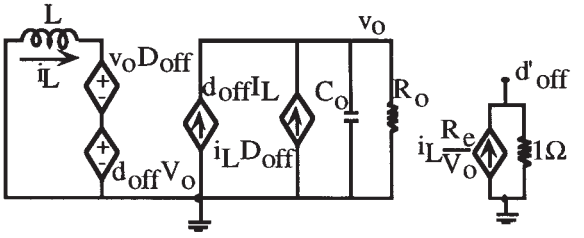


Fig. 5. Average behavioral small signal model for deriving inner loop gain.

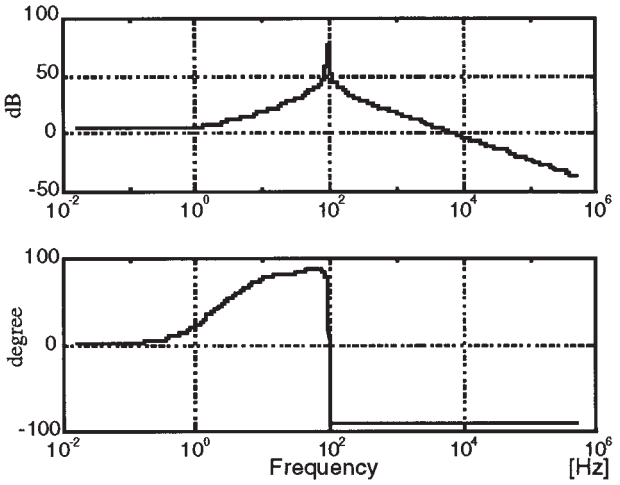


Fig. 6. Inner (current) loop gain for the boost stage drawn from (12) for the parameter values given in Section II. Upper trace: amplitude. Lower trace: phase.

$$f_p = \frac{D_{off}}{2\pi\sqrt{LC_o}} \tag{14}$$

To preserve a safe phase margin, the double pole should be at a lower frequency than the cross over of βA (12). That is, the ratio between the crossover frequency of βA ($R_e/2\pi L$) and f_p should be at least 5 (half a decade). Namely :

$$\frac{R_e}{D_{off}}\sqrt{\frac{C_o}{L}} > 5 \tag{15}$$

The Bode plot of Fig. 6 , drawn for the values given above (Section II) and D_{off}=0.57 demonstrate the nature of (12). With these practical values the crossover is around

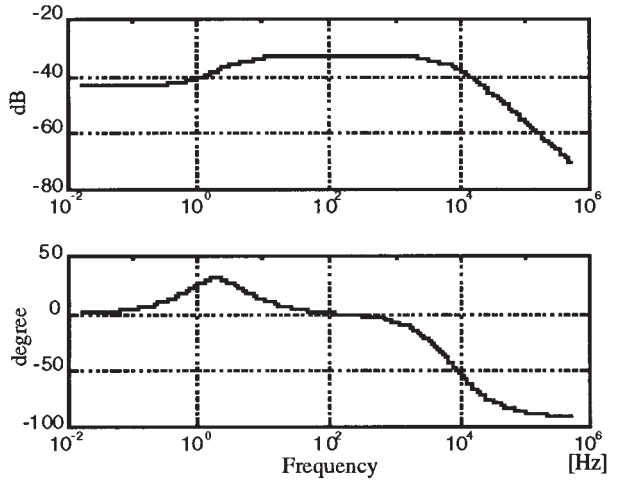


Fig. 7. Small signal line-voltage to input-current transfer function (16) for the parameter values given in Section II. Upper trace: amplitude. Lower trace: phase.

10kHz (as predicted from the approximate analysis) with a phase margin of 90^0. In engineering design, care should be paid to the location of the complex pole. If the crossover slope of the current loop gain is maintained at -20db/dec, the general behavior will be like predicted by the approximate analysis (5).

Following the same linearization procedure, the inner loop response (i_L/v_{in}) was found to be:

$$\frac{i_L}{v_{in}} = \frac{sC_oR_o + 1}{s^2LC_oR_o + s(L + C_oR_oR_e) + 3R_e} \tag{16}$$

with a zero at

$$f_z = \frac{1}{2\pi C_oR_o} \tag{17}$$

and a double pole at:

$$f_p = \frac{1}{2\pi}\sqrt{\frac{3R_e}{LC_oR_o}} \tag{18}$$

When $C_o \to \infty$ the output voltage can be considered constant and (16) is reduced to the approximate analysis solution (6). The nature of (16) can be appreciated by considering the Bode plots of Fig. 7 that were drawn for the numerical values given in Section II. For the range of interest (100Hz to 1kHz) tracking is excellent . At very low frequencies (DC) the gain is somewhat lower due the fact that V_o is now variable. This might introduce some distortion [11]. However as is demonstrated below, the actual distortion introduced is minor.

3. Outer loop gain

The outer open-loop response (v_o/v_e) was also derived by linearizing the system around a given operating point (Fig. 8). The outer response was found to be:

$$\frac{v_o}{v_eK_M} = \frac{sLI_L^2R_o - V_o^2}{s^2LC_oR_o + s(L + C_oR_oR_e) + 3R_e} \tag{19}$$

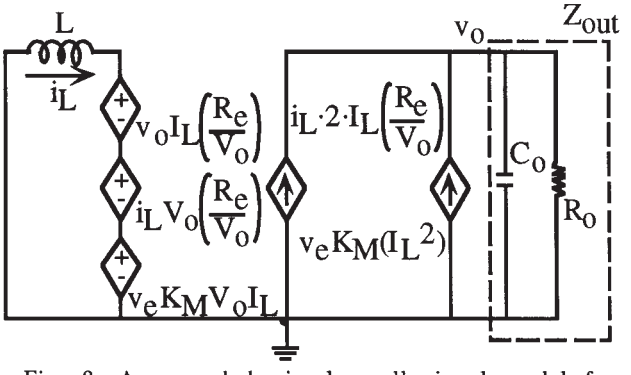


Fig. 8. Average behavioral small signal model for deriving outer loop transfer function.

L mH	C_o mF	V_r Volt (p-p)	3rd harmonic %	5th harmonic %	7th harmonic %	9th harmonic %	THD_{3-9} %
1	1	8	0.4	1.1	1.2	0.6	1.8
1	0.5	16	0.9	1.1	1.1	0.7	1.9
1	0.1	82	4.3	1.3	1.1	0.6	4.6
0.5	1	8.5	2.1	1.9	1.2	0.7	3.2
0.5	0.5	17	2.1	1.8	1.1	0.6	3.0
0.5	0.1	83	4.4	2.3	1.2	0.7	5.1

Table I. Percent harmonic distortion and THD of input current (for 3-9 harmonic components) as obtained by average simulation for 1kW APFC, V_o=380V and input voltage of 220V_{rms}.

where K_M is the transfer constant of the PWM modulator (D_{off}/(Volt·Amp)).

This transfer function includes a Right Half Plan Zero (RHPZ) at:

$$f_z = \frac{R_e}{2\pi L} \qquad (20)$$

and a double pole at:

$$f_p = \frac{1}{2\pi}\sqrt{\frac{3R_e}{LC_oR_o}} \qquad (21)$$

The typical response of Fig. 9 (for the values given in Section II) reveals the nature of the outer loop transfer function. Excess phase shift is evident due to the RHPZ. However since the required bandwidth is small (up to 10Hz) classical phase compensation procedures should suffice to stabilize the outer loop (Fig. 3a).

The gain of (19) at low frequencies (s -> 0) reduces to:

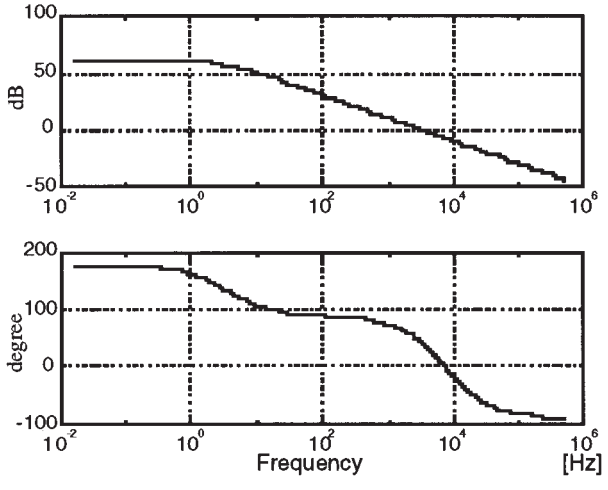


Fig. 9. Outer loop transfer function (19) for the parameter values given in Section II. Upper trace: amplitude. Low trace: phase.

$$\frac{v_o}{v_e K_M} = \frac{[V_o(av)]^2}{3R_e} \qquad (22)$$

Namely, the DC gain is a function of R_e, that is: the power level and rms input voltage. For optimum outer loop response one may wish to introduce feedforward compensation [10, 11]. This however will require sensing of the input voltage but only for the DC (heavily filtered) component.

4. The effect of output ripple.

Output ripple due to the practical finite value of the output capacitor will tend to distort the input current. Two effects can be envisioned. One is related to the fact that V_o (Fig. 1) includes an AC component and is not pure DC as assumed.

Secondly, the output of the outer loop error amplifier (Fig. 3a) will have an AC component that will modulate the current programming signal. The latter is not different from the case in conventional CCM APFC control [11, 12] and will not be dealt with here. The nonlinear effect of the ripple on the inner loop was studied by simulation for the 1kW case considered in Section II and the results are summarized in Table I. It is evident that even for the impractical case of L=0.5mH and C_o=100μF (1kW) which results in a ripple (V_r) of 83 V_{p-p}, the expected THD is relatively small, about 5% (Table I).

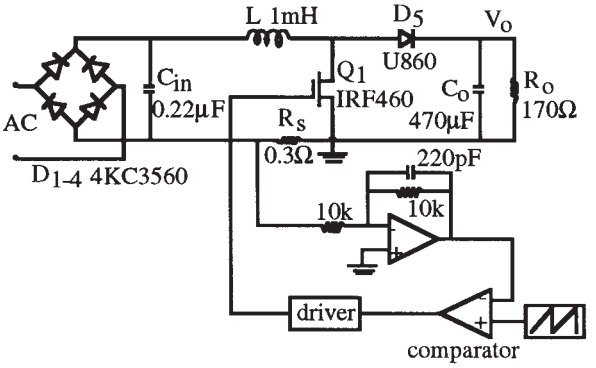


Fig. 10. Experimental set up.

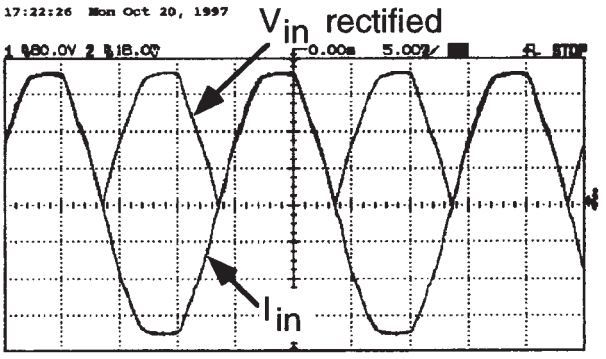


Fig. 11. Rectified line voltage and input current of experimental circuit (Fig. 10) for 1kW power level. Vertical scale: 80V/div and 1.6A/div. Horizontal scale: 5mS/div.

IV. VERIFICATIONS

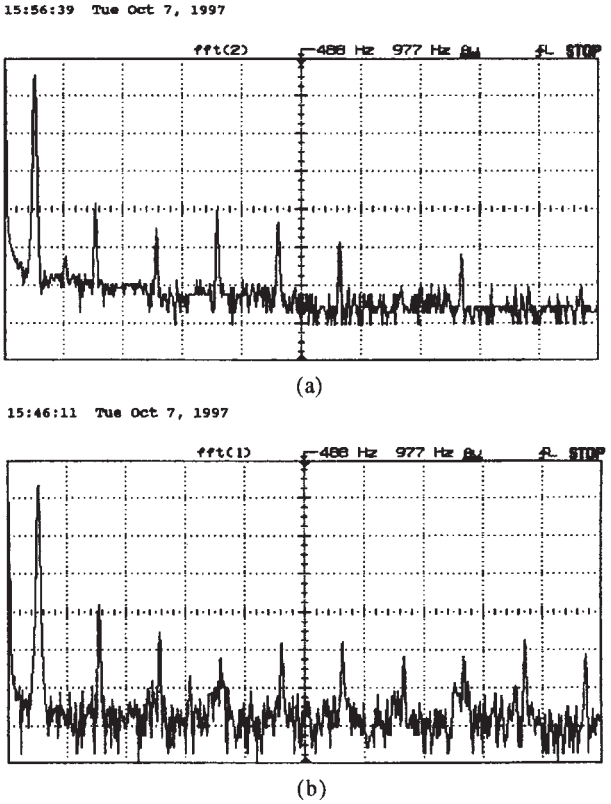
The theoretical considerations and results of the analyses given in above sections were verified by average simulation and laboratory experiments. The agreement between the theoretical derivation and average simulation was excellent to the point of being identical. It is indeed felt that average simulation could be conveniently used as a design assistant to check dependence on input voltage, power level etc.

A prototype converter was also built and tested in open outer loop. That is, in difference of Fig. 3a without controlling the output voltage. In this mode the output voltage will depend on the value of the programmed R_e . The actual implementation (Fig. 10) included a Boost stage and a simple D_{off} programming scheme. The tracking quality obtained experimentally is demonstrated by comparing the line current to the rectified input voltage (Fig. 11) . The spectra of the input voltage and input current (Fig. 12 a,b) suggest that the tracking introduces only minor excess THD.

V. DISCUSSION

To further explore the salient differences between the proposed approach and the 'classical' CCM implementation [11, 12] we compare the two when represented by a control-type block diagrams (Fig. 13). Only the parts associated with the current tracking are depicted. In each case there would be a need for an outer loop amplifier to keep the output voltage constant under variable operating conditions. The output of that error amplifier (V_{ev}) is used to drive the inner current loop. The two block diagrams are approximate. Both assume that the output voltage has no ripple component. We will also neglect here the ripple on V_{ev} and possible feedforward circuits [11, 12].

In the conventional control scheme shown in Fig. 13a, we recognize an inner current loop and a multiplier (M) that generates the reference to the inner loop. The feedback loop is composed of two parts: the inductor which sees two opposing voltages, $V_{in}(av)$ and $V_o D_{off}$ [7, 8] and a current error amplifier A_I. The latter is taken to include the modulator transfer function, sensing resistor etc. The drive signal of this inner loop is a reference current I_{ref} which is generated by multiplying the rectified input voltage by the output of the outer loop error amplifier (V_{ev}). On the other hand, the proposed control scheme uses the input voltage $V_{in}(av)$ as the excitation signal of the inner current loop (Fig. 13b). In this case, the output of the outer loop operational amplifier (V_{ev}) modulates the effective input resistance (R_e). Nominal value is assumed to be R_{e0} and for any other operating condition V_{ev} will change the input resistance so as to keep V_o at the desired level. For the conventional control scheme (Fig. 13a) $V_{in}(av)$ is in fact a disturbance. However, due to the high loop gain provided by A_I, which is built around an operational amplifier, the conventional current loop can suppress this disturbance as well as that caused by the output ripple. In the proposed control scheme (Fig. 13b), the magnitude of loop gain is evidently smaller (5) but if the interaction between the inductor L and output capacitor are taken into account (eq. 12, Fig. 6) one finds that the increase in the loop gain due to the passive components is rather significant. As it happens, practical value of L and C_o will have a resonant frequency around the low frequency range. A theoretical analysis of this question is beyond the scope of this paper. But examination of practical examples clearly show that the resonant range is as pointed out. For example, a normal engineering choice is



(a)

(b)

Fig. 12. FFT of line voltage (a) and input current (b). Vertical scale: 10dB/div. Horizontal scale: 97.7Hz/div.

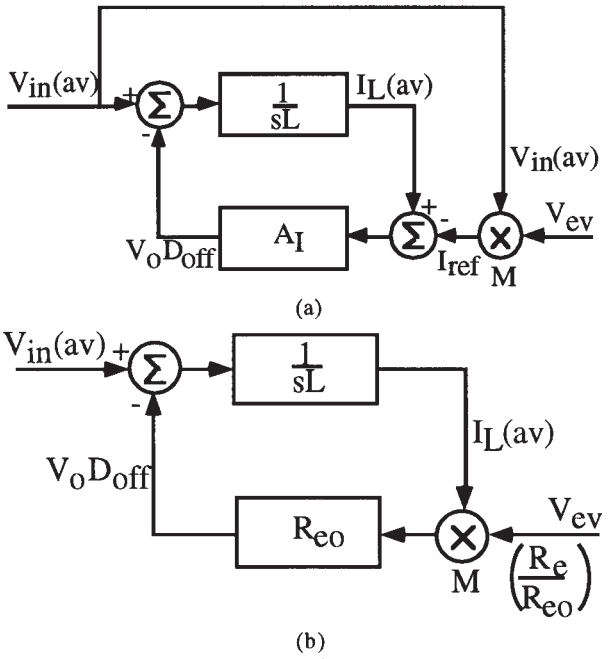


Fig. 13. Block diagram of a conventional (a) and proposed (b) power factor correction control.

1mF for a 1kW APFC while the inductor will be in the range 0.5mH to 1mH for this power range (depending on the switching frequency) . This will result in resonant frequency of 160 Hz. Damping will move the resonant frequency somewhat but still, it is expected to be in the right range.

The high loop gain due to the passive resonant phenomena explains the excellent tracking and the rejection of the disturbance due to the output ripple. In the conventional case, the rejection is due to the high loop gain provided by A_I (Fig. 13a). But the high gain of the operational amplifier plus the extra phase shifts of the phase compensation network may deteriorate the phase margin. Furthermore, the introduction of a very high gain operational amplifier may render the system sensitive to switching noise. In the light of the above, it appears that the lack of an operational amplifier in the inner current loop may not be deficiency but rather an advantage.

VI. CONCLUSIONS

The results of this study suggest that the proposed control scheme yields a stable dynamic system and provides good tracking of the input current. The inner loop gain of the system is well behaved and should not pose instability problems. The expected and actually measured bandwidth of current tracking should suffice in most if not all practical applications. It was further shown that the effect of output ripple is really minor from the practical point of view. It would thus appear that the proposed current programming scheme has all desirable characteristics required for implementing APFC.

The major advantage of the proposed scheme over the conventional approach [11] is the fact that there is no need to sense the input voltage and that it leads to a simpler control circuit. The advantage over other indirect methods [3-6] is the simplicity of implementation. The modulator of the proposed scheme is just a basic PWM circuit whereas in other indirect methods a much more elaborate duty cycle generators are required [3-6].

The intuitive reasoning, theoretical analysis, simulation and experimental results of this study seem to indicate that the proposed control scheme is useful and practical. Some questions are still open: operation in DCM, the need and implication of a feedforward path [11, 12] and optimal realization of the complete controller.

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