AVERAGE MODELING, ANALYSIS AND SIMULATION OF CURRENT SHARED DC-DC CONVERTERS

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Abstract - A practical, 'user-friendly' methodology is developed to study the behavior of current-shared converters. It applies average modeling, analysis and simulation to examine the static conditions and small-signal stability of converters that operate in Average Current Sharing (ACS) mode. Simple expressions for stability criterion were developed and applied to assess the influence of the number of paralleled modules on the stability and dynamics of the converters system.

I. INTRODUCTION

Paralleling of DC-DC converters has many desirable features: increased reliability, expandability and on-site repair when hot plug-in capability is incorporated. However, the analysis and design of parallel converters are far from being simple due to the fact that they are no longer of the single-input single-output type [1-6]. For increased reliability, paralleled converters require a Current Sharing (CS) mechanism to ensure distribution of currents and stresses between the modules. Unfortunately, the CS control introduces additional feedback loops that might render the paralleled system unstable even if each module by itself is stable [3-6].

The objective of this study was to develop a simple, 'user friendly' methodology for the analysis of current shared converter systems. The approach applies average behavioral modeling and general purpose circuit simulation programs such as PSPICE (MicroSim Inc.) to simplify the mathematical treatment. The key idea is to leave the (often messy) derivation of basic small signal transfer functions to the simulator while treating the global problem in an analytical form. The proposed method was applied to derive simple expressions that can be used to examine the effect of the CS circuitry and number of paralleled modules on the system's load-sharing stability and dynamics. Although demonstrated by considering voltage mode Buck converters operating in 'average CS' configuration [1,3-4], the proposed analytical methodology can be extended to any kind of converter modules (topologies, current or voltage mode control) with any type of CS scheme.

II. PARALLELED CONVERTER MODULES WITH AVERAGE CURRENT SHARING

The proposed methodology will be detailed by considering a system of n paralleled DC-DC converters with Average Current Sharing (ACS) and load resistance R_L. In the ACS scheme (Fig. 1) a single shared bus interconnects all the modules. The signal (normally voltage) of this common line (V_{bus}) represents the average load-current contribution of all units. The shared bus signal (V_{bus}) is compared to the output current I_o of the individual module (after translation to a voltage signal V_{cs}) and the difference adjusts by current sharing control (CSC) the reference of the voltage amplifier that senses the output voltage (scaled by k_v) until load current equalization is achieved.

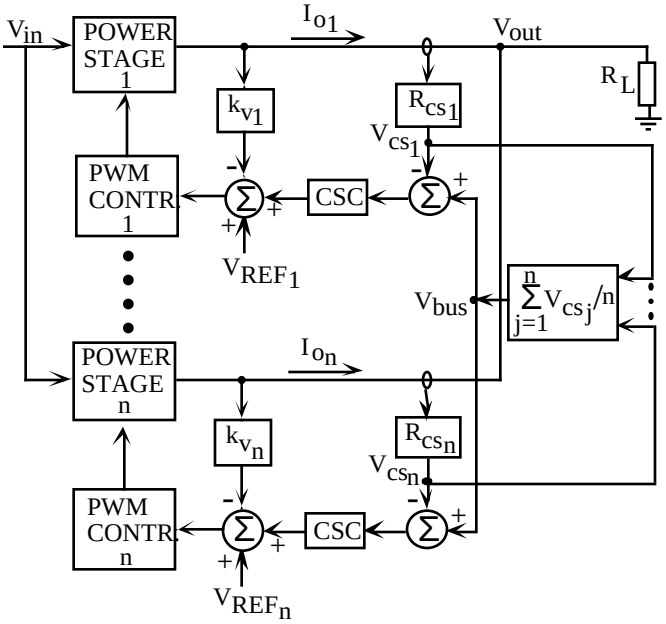

Fig. 1 Block diagram of n paralleled converters with Average Current Sharing (ACS).

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III. MODELING A SINGLE CONVERTER MODULE

The circuit diagram of a single voltage-mode (transconductance error amplifier) controlled Buck converter module with an ACS interface (F_{cs}) is shown in Fig. 2 and its average model based on the Switched Inductor Model (SIM) is given in Fig. 3 [7-9]. The average modeling of single converter module is shown in Fig. 3. The model is based on the Switched Inductor Model (SIM) presented in [8-9]. This model is based on the observation that by applying the average voltage across an inductor (L) one gets the average current (I_L) flowing through it. This current can then be incorporated as dependent current sources to emulate the average currents of the other two ports of the switched inductor. The expressions of the dependent sources for the average model of Fig. 3 are thus as follows:

$$G_a = \frac{D_{on}\, I_L}{D_{on}+D_{off}} \qquad (1)$$

$$G_b = \frac{D_{off}\, I_L}{D_{on}+D_{off}} \qquad (2)$$

$$G_c = I_L \qquad (3)$$

$$E_L = V_{ac}\, D_{on} + V_{bc}\, D_{off} \qquad (4)$$

where D_{on} is the duty-cycle and

$$D_{off} = \frac{2\, I_L\, L\, f_s}{V_{ac}\, D_{on}} - D_{on} \quad \text{for Discontinuous Conduction Mode}$$

or $D_{off} = 1 - D_{on}$ for Continuous Conduction Mode (5)

where f_s is the switching frequency.

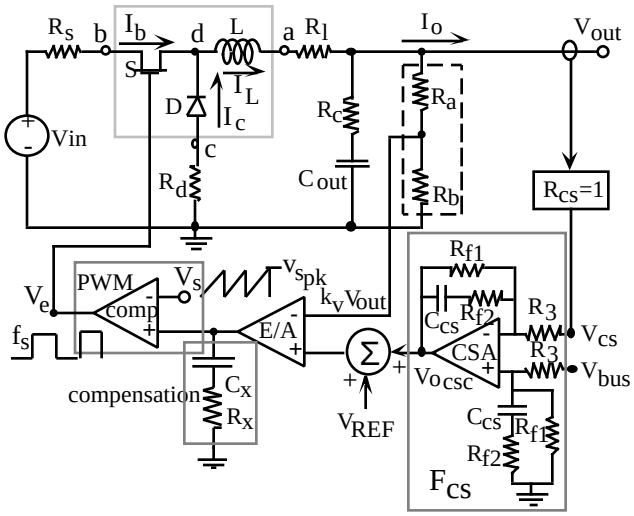

Fig. 2. Circuit diagram of a single voltage-mode controlled Buck converter module with ACS interface.

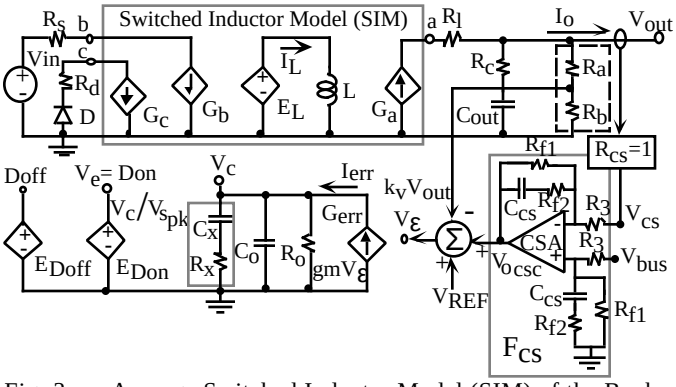

Fig. 3. Average Switched Inductor Model (SIM) of the Buck converter module shown in Fig. 2.

In Fig.3 G_c represents the average current feeding the steering diode D (Fig.2), E_L is the average voltage across the inductor (4), G_b is the average current of the input port (b) and G_a is the average current fed to the load (a). The voltage error amplifier (Fig.2) is represented in Fig. 3 as transconductance dependent source (G_{err}). E_{Don} and E_{Doff} in Fig. 3 are dependent sources that generate the voltage coded D_{on} and D_{off} as a function of PWM generator ($V_c/V_{s_{pk}}$) (Fig. 2). The Current Sharing Amplifier (CSA) in Fig. 2 is implemented in Fig. 3 by voltage dependent source with gain of 10^5.

IV. STATIC ANALYSIS OF N PARALLELED MODULES

Assuming that the combined error voltage $V_\varepsilon \to 0$ (high gain E/A), the reference voltage of an arbitrary X-th converter module (V_{REF_X}) (Figs. 2,3) is related to other relevant parameters by the relationship:

$$V_{REF_X} = k_{v_X}\, V_{OUT} + k_{cs_X}\,(I_{O_X} - V_{BUS}) \qquad (6)$$

where $k_{cs_X} = R_{f1}/R_3$ is the DC gain of F_{cs_X} (Figs. 2,3) and all other parameters in this equation refer to steady-state values.

The bus voltage is a function of output currents of all converter modules:

$$V_{BUS} = \frac{\sum_{j=1}^{n} I_{O_j}}{n} \qquad (7)$$

We assume that $k_{v_1} = \ldots = k_{v_n} = k_v$. The output voltage is then derived from (6):

$$V_{OUT} = \frac{V_{REF_{av}}}{k_v} \qquad (8)$$

where

$$V_{REF_{av}} = \frac{\sum_{j=1}^{n} V_{REF_j}}{n} \qquad (9)$$

When $V_{REF_x} \neq V_{REF_y}$ and $k_{cs_1} = \ldots = k_{cs_n} = k_{cs}$, the output current distribution of any two converter modules is found to be:

$$I_{o_x} - I_{o_y} = \frac{V_{REF_x} - V_{REF_y}}{k_{cs}} \qquad (10)$$

The last equation implies that the current distribution between any two converter modules with different reference voltage (V_{REF}) will exhibit smaller imbalance when k_{cs} is large enough.

V. DYNAMIC ANALYSIS OF N PARALLELED MODULES

The analysis of n paralleled modules system now proceeds under the assumption that all modules are identical. The small signal model of a single converter module is based on the average model of Fig. 3. Two transfer functions for this module are defined for a given j-th module:

$$H_j = \frac{i_{o_j}}{v_{e_j}} \qquad F_j = \frac{v_{e_j}}{v_{\varepsilon_j}} \qquad (11)$$

H_j describes the converter's small signal transfer function from the error voltage v_{e_j} to the converter's output current i_{o_j}, and F_j is the feedback small signal from the combined error voltage v_{ε_j} to the error voltage v_{e_j} (Fig. 3). The H and F transfer functions can be derived analytically [8] or evaluated by simulation [7-9]. The latter method, which is of course much easier to execute, is less prone to errors but yet provides all the necessary information for a thorough analysis of a CS converter system. This 'mixed mode' (simulation-analytical) approach is applied here. In the followings, 'measured' means obtained by simulation.

The combined error voltage v_ε includes four components:

$$V_\varepsilon = F_{cs}\, v_{bus} - F_{cs}\, i_o + v_{ref} - k_v\, v_{out} \qquad (12)$$

where F_{cs} describes the small signal transfer function of CS loop ($Vo_{csc}/(v_{bus} - i_o)$) (Figs. 2,3). Setting v_{ref} to zero (because it does not affect small-signal stability), the following expression for an arbitrary X-th module was obtained:

$$v_{\varepsilon_x} = -i_{o_x}\left(\frac{n-1}{n}F_{cs} + k_v R_L\right) + \left(\sum_{j=1}^{n} i_{o_j} - i_{o_x}\right)\left(\frac{F_{cs}}{n} - k_v R_L\right) \qquad (13)$$

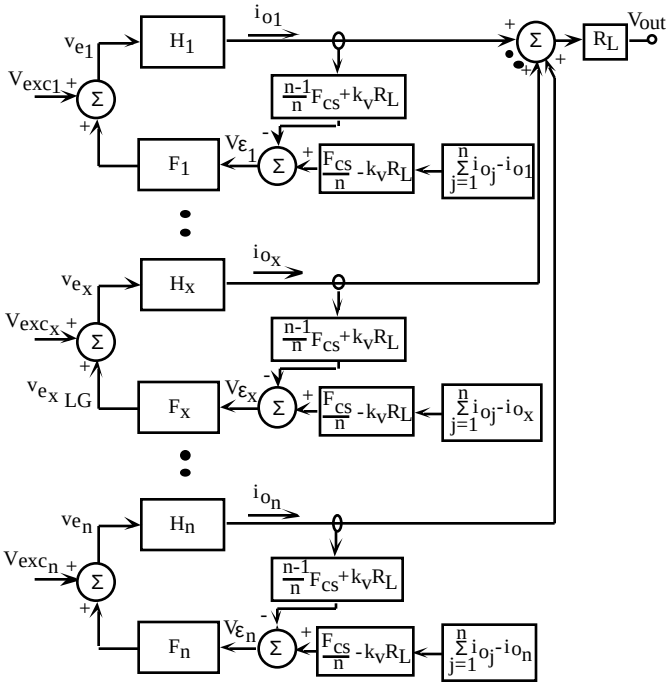

Fig. 4. Small signal block diagram for n parallel modules with ACS driving a load R_L.

Following the above procedure, the small signal output current of any given X-th module was found to be:

$$i_{o_x} = \left[-i_{o_x}\left(\frac{n-1}{n}F_{cs} + k_v R_L\right) + \left(\sum_{j=1}^{n} i_{o_j} - i_{o_x}\right)\left(\frac{F_{cs}}{n} - k_v R_L\right)\right] F_x H_x \qquad (14)$$

Since the location of the single AC voltage source excitation is in the X-th module (Fig. 4) it will influence the measured (by simulation) transfer function H_x. That is $H_x \neq H$ where H is the measured transfer function of all modules except the X-th. Hence, $i_{o_x} \neq i_o$ where i_o is the output current of all modules except the X-th. However, the measured transfer function F_j of all identical modules including X-th is the same, i.e. $F_j = F$.

The output current of each module except the X-th is related to the output current of the X-th module by following equation:

$$i_o = \frac{\left(\frac{F_{cs}}{n} - k_v R_L\right) F H}{1 + \left(\frac{F_{cs}}{n} - (n-1)k_v R_L\right) F H}\, i_{o_x} \qquad (15)$$

The loop-gain for 'single excitation' of X-th module ($(L.G)_x$) is obtained from (14) and (15):

$$(L.G)_X=\left[\left(\frac{n-1}{n}\right)F_{cs}+k_vR_L\frac{(n-1)\left(\frac{F_{cs}}{n}-k_vR_L\right)^2}{1+\left(\frac{F_{cs}}{n}-(n-1)k_vR_L\right)F_H}\right]Fh_X \quad (16)$$

Although (16) is theoretically correct, it is extremely hard to apply in practical cases. One reason for that is the fact, that the transfer functions H represent the transfer function i_o/v_e of any given module while loaded by R_L in parallel with the parallel output impedances of (n-1) modules. To overcome this difficulty we purpose to use average simulation to obtain the key dynamic parameters of the systems. Three tests are proposed: a global stability test, the common mode response and current sharing (differential) response.

Global stability test

The stability and dynamic performance of the system can now be evaluated by singling out one converter (to be labeled 'X') and performing a traditional loop gain analysis around this unit. To this end, an external independent AC voltage source excitation should be placed in series with the duty-cycle E_{Don} dependent source (Fig. 3) [10]. The excitation is included only in the X-th module, V_{exc_X} =1[Vac] while in the other modules V_{exc_j} =0 (Fig. 4). The loop-gain and phase-margin can now be obtained by examining $Ve_{X_{LG}}/Ve_X$. Since the sample module X is arbitrarily chosen, the derived loop gain is in fact the loop gain of the system, since it describes the dynamic response of the any module to a disturbance.

Common mode response

To test the inner-loops control of the system (voltage loop in voltage-mode or current and voltage loops in current-mode), a common AC voltage source excitation should be applied to all paralleled converter modules (Fig. 4) $V_{exc_1}=V_{exc_X}=....=V_{exc_n}$ =1[Vac]. It induces equal output currents $i_{o_1}=i_{o_X}=...=i_{o_n}=i_o$ and $v_{bus}=i_o$ and therefore eqs. (12) and (13) reduce in this case to:

$$v_\varepsilon = - k_v\, v_{out} = - k_v\, n\, i_o\, R_L \quad (17)$$

Hence, the loop-gain of any given module is found to be:

$$L.G_C = - k_v\, n\, R_L\, H_C\, F_C \quad (18)$$

where the transfer functions H_C, F_C for the common excitation case have the same basic definitions of (11). The total feedback loop (β_C) transfer function reduces to:

$$\beta_C = k_v\, n\, R_L\, F_C \quad (19)$$

where the feedback loop β_C can be obtained by measuring $Ve_{X_{LG}}/i_{o_X}$ (Fig. 4) . However, H_C differs from H and H_X, due to the otherwise loading. It should be noted, that H_C can be easily obtained by simulation or analytically and the control voltage loop (F_C) now can be independently designed. Indeed, loop-gain LG_C (18) offers the ability to examine the stability of n paralleled converters loaded by R_L without the influences of current-sharing loop. Applying (18) the loop-gain and the phase-margin of each module are obtained. It means that, this case examines only the dynamic response of a common (or identical) perturbation in all the modules.

The differential response

To examine the influence of current-sharing loop (outer-loop) on the stability of the system we apply now a differential AC voltage source excitation. In this case, we examine arbitrarily the X-th module by applying V_{exc_X} =1[Vac] into the X-th module (Fig. 4) and $V_{exc_1}=...=V_{exc_n}$ =-1/(n-1)[Vac] into the other modules. Since all modules are identical, it induces $i_{o_1}=..=i_{o_n}=i_o=-i_{o_X}/(n-1)$, which implies $v_{bus}=0$ and $v_{out}=0$. It also follows that the load current is zero:

$i_{R_L}=i_{o_1}+..+i_{o_X}+..+i_{o_n}=(n-1)i_o+i_{o_X}=0$,

and therefore eqs. (12) and (13) reduce to:

$$v_{\varepsilon_X} = - F_{cs_X}\, i_{o_X} \quad (20)$$

Thus, the loop-gain of arbitrary X-th module for differential excitation is given by:

$$(L.G_d)_X = - F_{cs_X}\, H_{d_X}\, F_{d_X} \quad (21)$$

where the transfer functions H_{d_X} and F_{d_X} for the differential excitation case have the same basic definitions as shown in (11). The total feedback loop transfer function from (21) can be expressed as:

$$\beta_{d_X} = F_{cs_X}\, F_{d_X} \quad (22)$$

where β_{d_X} can be obtained by measuring $Ve_{X_{LG}}/i_{o_X}$ (Fig. 4) . Indeed, this case examines the sample module X when it is loaded only by the other (n-1) modules, because the total current load perturbations are zero and the load R_L has thus no effect, which means that H_{d_X} differs from H_C and H. The importance of eq. (21) is its ability to examine or even design the current-sharing control loop without the effects of the voltage control loop. Consequently, this case explores the dynamic response of differential perturbations between the modules.

The observation of the general expressions (16), (18), (19), (21) and (22) can be practiced as follows. For a given H_C (analytically or by simulation) the LG_C (18) and (19) can

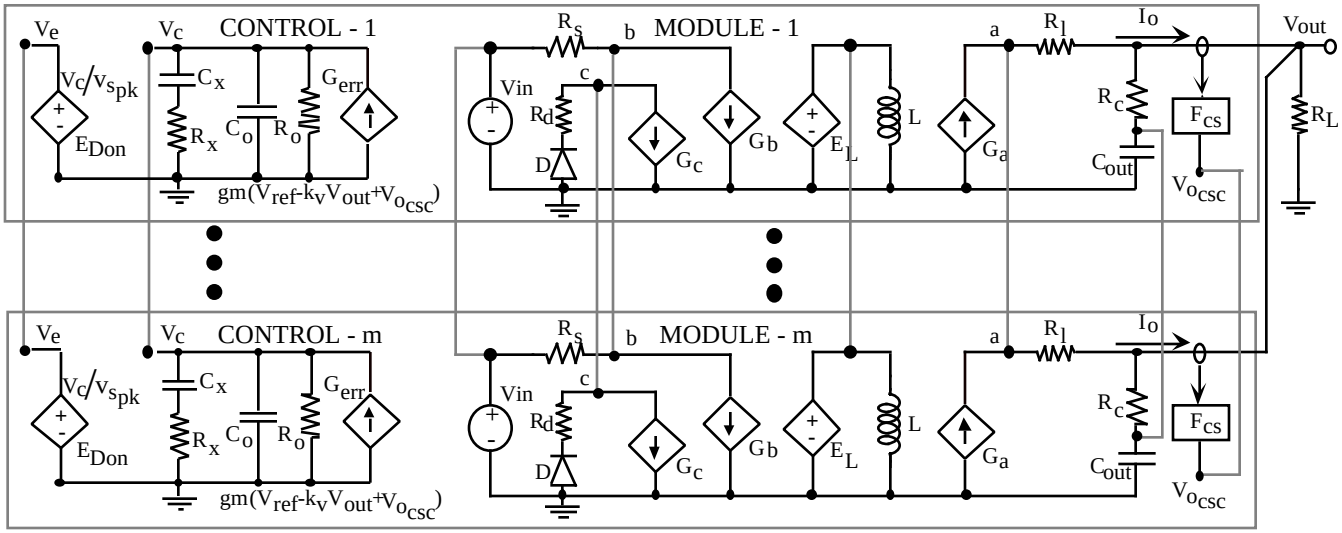

Fig. 5. The current and voltage properties of paralleled brunch in identical converter modules.

be used to design the inner loop F_c ($F=F_c=F_d$). Now, H_d can be obtained by simulation and through LG_d (21) and (22) the outer loop F_{cs} can be designed. This procedure grants the ability to predict by simulations the influence of the transfer functions H, F, load resistance R_L and number of modules n on the loop-gain (LG). Consequently, these relationships can be used in a simple manner to stabilize the system and/or improve the system's phase-margin as follows:

1. Design and stabilize the inner loops according of the procedure of 'common mode response'.
2. Design and stabilize the outer-loop (CS loop) according of the procedure of 'differential response'.
3. Determine the phase-margin of the overall system by 'single excitation'.

VI. THE FOLDED MODEL

The procedures suggested above involve simulation of systems with n modules. In some cases m modules are identical and parallel connected to the load. To simplify and cut simulation time we can 'fold' m parallel connected units into a single unit. This is justified by the fact that all node voltages of identical units are equal and hence can be connected (Fig. 5). By doing this the system of m parallel units is reduced to a single unit. However, some 'folding rules' have to be observed:

1. Control circuitry is left as is. The reason is that the small signal response of a single circuit or m parallel connected control circuits are the same.
2. In case when m power stages feed a load, the impedances have to be reduced by m. This is needed to correctly represent the lower output impedance of m parallel connected power stage units.

Following these 'folding rules' n current shared modules can be represent as a basic module in parallel to an (n-1) folded unit (Fig. 6).

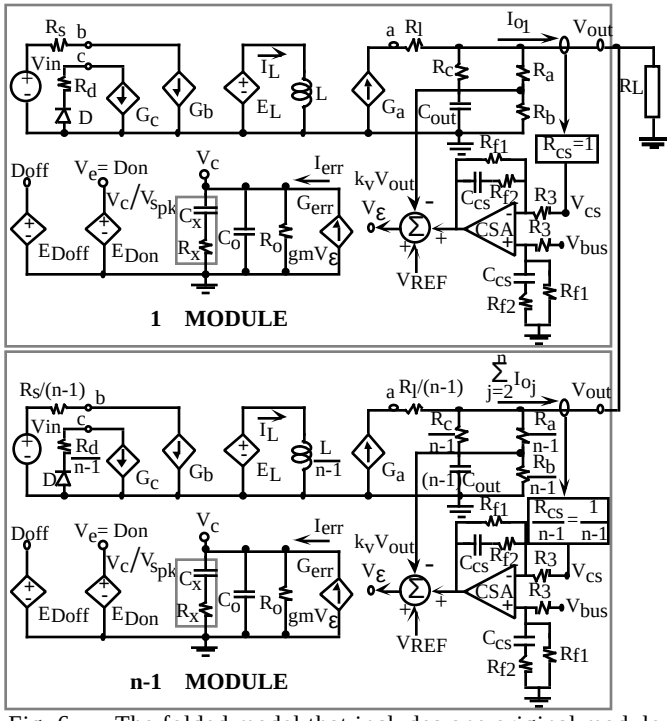

Fig. 6. The folded model that includes one original module with n-1 folded modules.

VII. SIMULATION RESULTS

To illustrate the above proposed procedures for testing parallel ACS system, Bode plots of loop-gain (gain and phase) and transients output voltage and currents were simulated by PSPICE (V. 7.1, MicroSim Inc.) for three paralleled modules similar to Fig 3 by applying the folded model of Fig. 6.

The parameters of the three converters were as follows: common load R_L=5Ω, power stage: V_{in}=12V, L=75μH, C_{out}=220μF, R_c=0.07Ω, R_s=0.1Ω, R_d=0.1Ω, R_l=0.1Ω, R_a=R_b=10KΩ. voltage control loop: V_{REF}=2.5V, gm=3.21[mA/V], R_o=3MΩ, C_o=177pF, R_x=12.3KΩ, C_x=25.9nF, $V_{s_{pk}}$ =2.5V. current-sharing loop: R_{cs}=1Ω, R_3=10kΩ, R_{f1}=100KΩ, C_{cs}=145nF and R_{f2}=250Ω and later R_{f2}=0. Analysis and design techniques were verified by running two sets of simulations. All sets were done on the complete parallel system as a function of R_{f2}. The resulting Bode plots of H_c, $1/\beta_c$, LG_c and phase under common excitation $Vexc_1$ =$Vexc_{2,3}$=1[Vac] (Fig.4) are shown in Fig. 7. The crossover phase is -136°, indicating stable operation with phase-margin (PM) of 44°. Note that CS loop (or R_{f2}) does not influence upon LG_c. We now examine the Bode plot (Fig. 8) of H_d , $1/\beta_d$, LG_d and phase for the arbitrary 1-th module under differential-mode excitation $Vexc_1$ =1[Vac] and $Vexc_{2,3}$=-1/2[Vac]. The crossover phase is -122°, indicating stable operation with phase-margin of 58°. The transient response of three parallel converters is simulated by 10mV, pulse 10[μSec] excitation injected into voltage error amplifier (E/A) of the 1-th module. Fig. 9 shows the resulting response of the three converter output currents, which quickly decay down, indicating reasonable stability. Fig. 10 shows the Bode plot of the overall LG (eq. 16) and phase for 1-th module under single excitation $Vexc_1$ =1[Vac] and $Vexc_{2,3}$=0 to confirm the stability for the combination of the common and differential modes PM=57°.

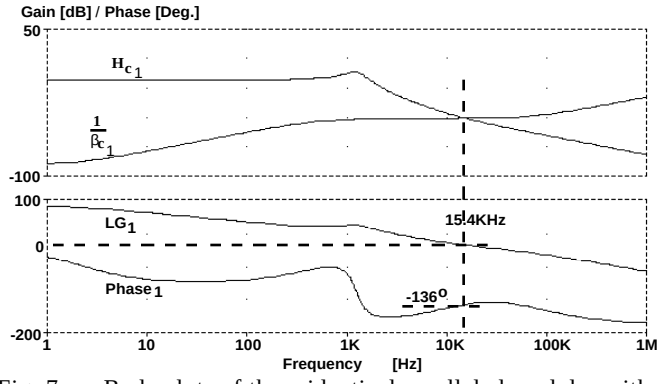

Fig. 7. Bode plots of three identical paralleled modules with ACS under common excitation.

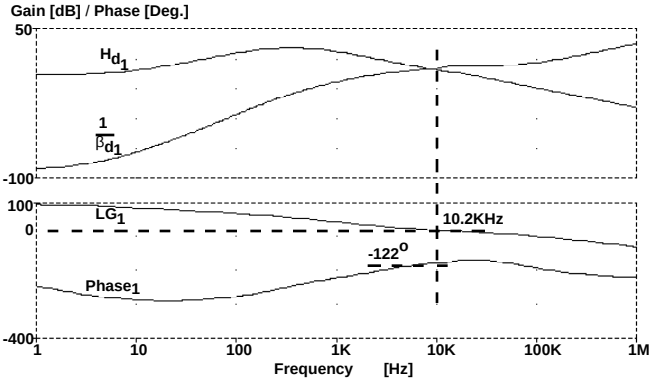

Fig. 8. Bode plots of three identical paralleled modules with ACS under differential excitation, with R_{f2}=250Ω.

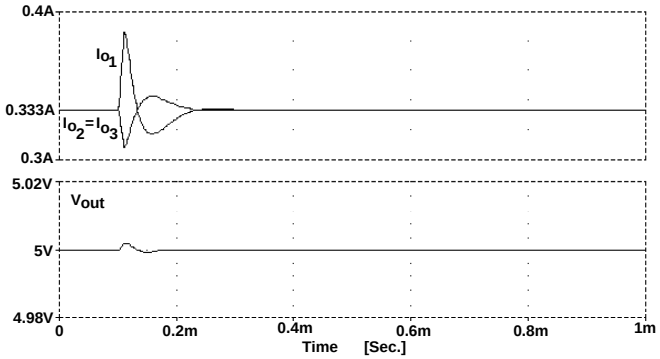

Fig. 9. Transient simulations of output currents and output voltage of three identical paralleled modules, with R_{f2}=250Ω, when the pulse excitation is injected into the first module.

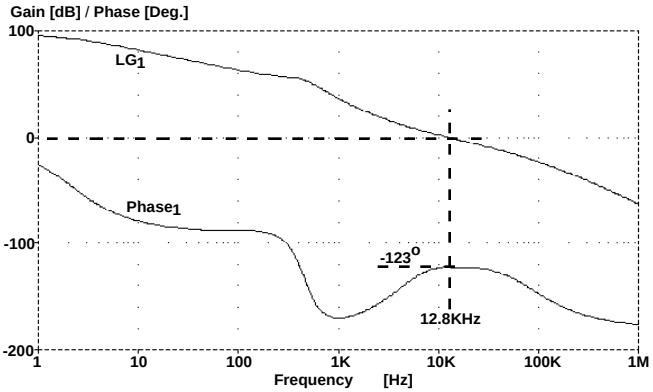

Fig. 10. Bode plots of ACS system with three identical modules under single excitation, with R_{f2}=250Ω.

Next, R_{f2} was set to zero. The Bode plot under differential-mode is shown in Fig. 11, where the crossover phase is -186°, indicating instability, with phase-margin of -6°. The simulated transient response is shown in Fig. 12, where the amplitude of the output current of the three modules is increasing, as expected. Bode plot under single module excitation in Fig. 13 verify instability again PM=-10°.

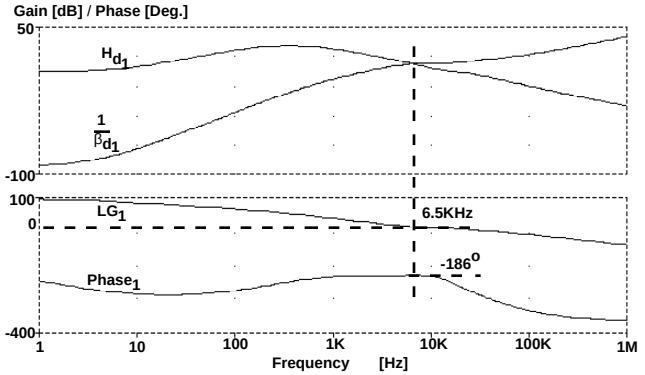

Fig. 11. Bode plots of three identical paralleled modules under differential excitation, with R_{f2}=0, indicating instability.

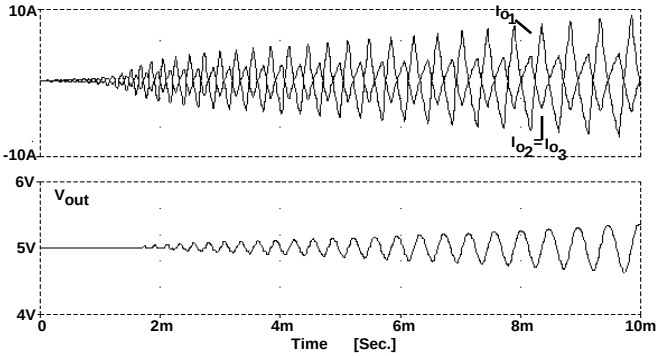

Fig. 12. Transient simulations of output currents and output voltage of three identical paralleled modules, with R_{f2}=0, when the pulse excitation is injected into the first module.

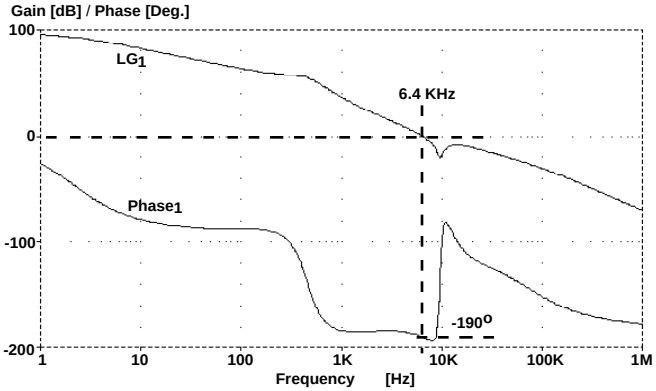

Fig. 13. Bode plots of ACS system with three identical paralleled modules under single excitation, with R_{f2}=0.

VIII. DISCUSSION AND CONCLUSIONS

Results of this study clearly show that stability conditions of a paralleled ACS converter system can be readily analyzed by applying the methodology proposed in this investigation. The methodology is based on frequency domain loop gain response which is conveniently obtained by average simulation. The LG expressions (16), (18), (21) developed for an ACS system of n paralleled identical modules were found efficient to correctly predict the system's behavior. These relationships can thus be used in the design phase of a ACS converter system. The theoretical implications of (16), (18), (21) are discussed and used in representative example. To illustrate and design n identical converter modules, we developed a folded model that can simplify the simulations based methodology proposed in this investigation. The present study considered a voltage mode Buck module but the results are general and apply to any topology and any control method (e.g. Boost in peak current mode) as long as the pertinent transfer functions H and F can be derived or obtained by average simulation. Applying the general 'mixed mode' methodology proposed here, other CS scheme can be analyzed for their static and dynamic behavior.

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