A NOVEL SELF-OSCILLATING SYNCHRONOUSLY-RECTIFIED DC-DC CONVERTER

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ABSTRACT

A new topology, a Self Oscillating Synchronously Rectified DC-DC Converter (SOSYRC) is proposed and examined analytically and experimentally. The converter is composed of an autonomous high frequency push-pull oscillator, a synchronous PWM controller/driver, a synchronous rectifier and an output filter. The synchronous controller is built around a conventional PWM controller. Its function is to maintain zero voltage switching (ZVS) and to pass integer number of cycles of the main frequency to prevent saturation of the push pull transformer due to unbalanced operation. The main features of the SOSYRC are: operation under ZVS conditions, sinusoidal voltage waveforms and the ability to independently control multiple outputs. Another important feature is the fact that only a fraction of the resonant current passes through the switches. Simulation and experimental results were found to be in good agreement with the model developed for the proposed SOSYRC.

INTRODUCTION

The ever persisting quest for smaller and yet highly efficient DC-DC converters has lead investigator to examine resonant and quasi-resonant topologies. The inherent feature of these approaches is the reduction of switching losses at high frequencies by ensuring a more favorable switching conditions such as zero current switching. The resonant topologies proposed hitherto have, however, two major drawbacks: the fact that the resonant currents are passing through the switches, the wide frequency range of operation and the need for rather complicated VCO type controllers. Here we propose a new topology: the Self-Oscillating Synchronously-Rectified DC-DC Converter (SOSYRC) which is practically free of these problems. The major idea behind this approach is the synchronization of all switches to a sinusoidal signal which is generated by an autonomous high frequency power oscillator. By this, one overcomes the need for a variable frequency controller and has only to synchronize the switching signals to the inherent resonant frequency of the system. Hence, switching losses can be reduced by properly synchronizing the switching operation with the zero crossing points of the sinusoidal waveform. An important side benefit of this mode of operation is the dramatic reduction of the emitted EMI and the grouping of the spurious signal around the main HF carrier.

THE PROPOSED TOPOLOGY

The proposed topology is composed of four major parts (Fig. 1): an autonomous push-pull high frequency oscillator, a synchronous PWM controller/driver, a synchronous rectifier and an output filter in a Buck configuration. The functions of the synchronous PWM controller/driver are three fold: it generates a duty cycle signal (D) which is proportional to the control voltage (V_{cotrol}), it ensures zero voltage switching of the synchronous rectifier and it adjust T_{on} such that it will always be an integer number of sinus cycles (that is, an even number of half cycles). The latter is required to prevent

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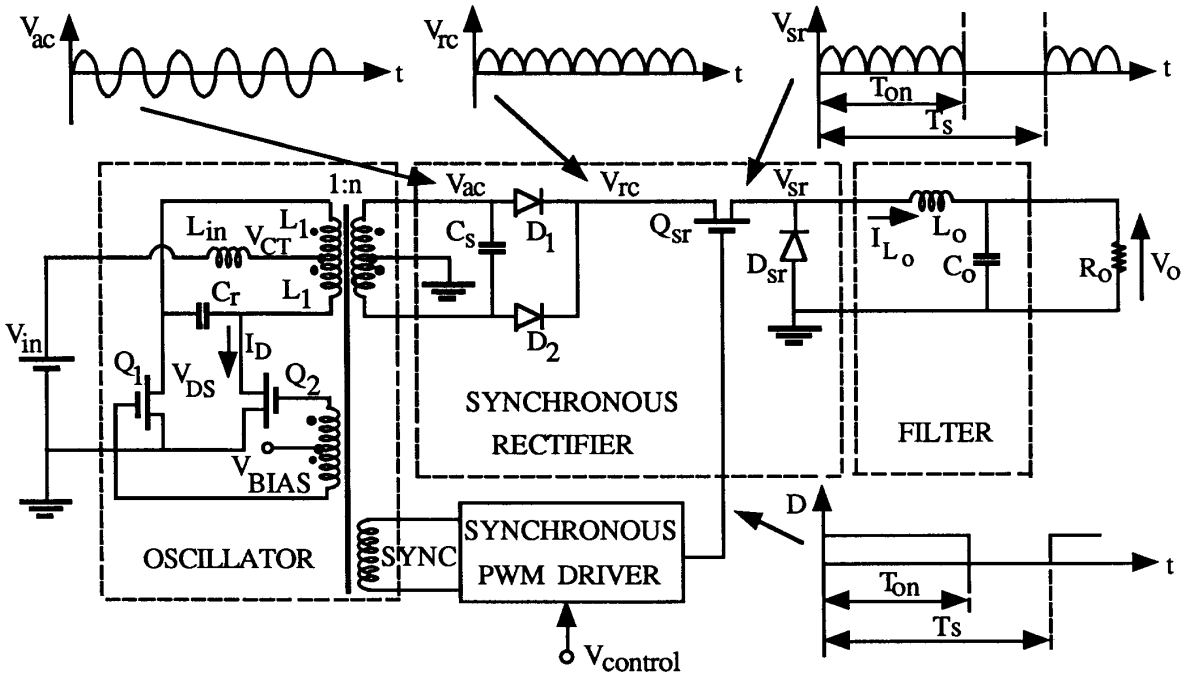


Fig. 1. Proposed SOSYRC topology.

transformer saturation due to unbalanced operation. The synchronous PWM controller/driver is built around a conventional PWM controller with some logic circuitry to synchronize the duty cycle signal to the main frequency of the system. Since the controller is located at the secondary, multiple regulated outputs can easily be realized by driving each output by its own dedicated controller.

Examination of the overall topology of the proposed SOSYRC reveals several important features. The most important one being the fact that it operates under zero voltage switching (ZVS) conditions. This is true for all the switching elements: the oscillator drivers, the rectifier diodes, the PWM switch and the freewheeling diode. Consequently, switching losses should be low even when operated at high frequency. Furthermore, since there is no chopping of the sinusoidal signals, the spectral content of the voltages waveforms should be confined to the neighborhood of the main frequency of the system. This should help to reduce emission EMI. Other important features of the proposed SOSYRC will be discussed below following the development of the SOSYRC's models.

MODEL DEVELOPMENT

The unloaded oscillator. We first consider the operation of the high frequency power oscillator. The oscillator is similar to the well known current fed inverter [1]. However, contrary to the operating conditions of the current fed inverter, the input series inductor L_{in} (Fig. 1) of the SOSYRC must not be made large since large L_{in} will result in a narrow small-signal bandwidth. This is evident from the average model developed below. Consequently, one can not made the assumption that the push pull stage is fed by a current source.

The basic model of the unloaded oscillator includes a toggle switch which alternately shorts to ground the two ends of a parallel resonant circuit which is composed of an inductor L_r and a capacitor C_r. Note that the inductor L_r represents the total primary winding of the transformer shown in Fig. 1. That is :

$$L_r = 4 L_1 \qquad (1)$$

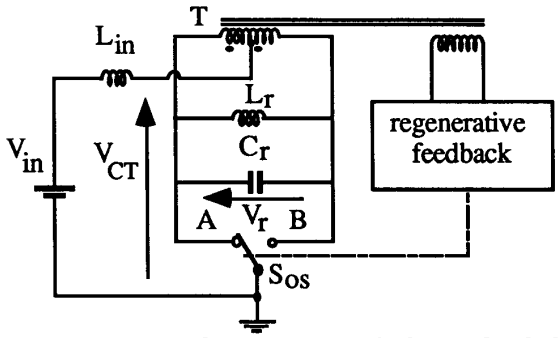


Fig. 2. Equivalent circuit of the unloaded push-pull oscillator.

The transformer action (Fig. 2) is modelled by an ideal auto-transformer with a 1:1 turns ratio.

The oscillations in the circuit are sustained by a regenerative action which toggles the switch whenever the voltage across the resonant circuit crosses the zero (Fig. 3). This insures ZVS conditions for both turn-on and turn-off. A thorough analysis of the stability of oscillation of the circuit is beyond the scope of this paper. It will be assumed here that oscillations are sustained and since a lossles circuit is assumed at this stage, the waveform is sinusoidal. Under this assumption, the waveform at the center tap of the transformer (V_{CT}) will be as shown in Fig. 3. Being this the case and assuming that L_{in} current is bound, the steady state average voltage of V_{CT} must be equal to V_{in}:

$$\bar{V}_{CT} = V_{in} \tag{2}$$

And since :

$$\bar{V}_{CT} = \frac{1}{\pi}\int_0^{\pi} \frac{V_r(\phi)}{2}\, d\phi = \frac{V_r}{\pi} \tag{3}$$

the amplitude of oscillation across the tank is found to be:

$$V_r = \pi\, V_{in} \tag{4}$$

The next question to consider is the average model of the push-pull stage as seen from the center tap. That is, the average (low frequency) load that L_{in} sees (Fig. 2). Elementary considerations suggest that this load has a

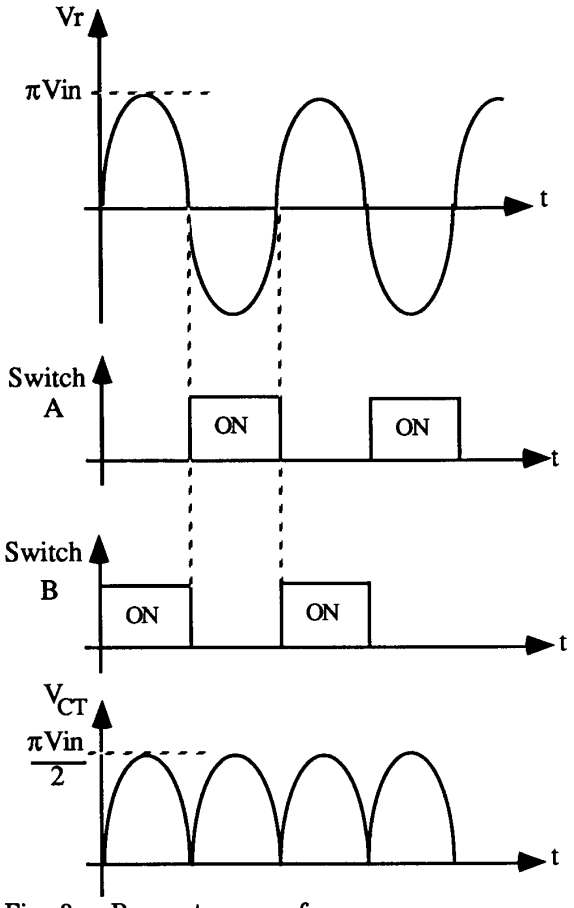


Fig. 3. Resonator waveforms.

capacitive nature. This conclusion is reached by considering the response of the resonant circuit when a current impulse fed at the center tap . The expected increase in the voltage amplitude of the oscillation is that of a step function, similar to the response of a capacitor. One can thus conclude that the equivalent circuit of Fig 4 will represent the *average* response of the oscillator of Fig 3. The value of the equivalent capacitor (C_{eq}) can be estimated by the requirement that the energy stored in it should be equal to the energy stored in the resonant circuit. That is:

$$\frac{(V_{in})^2\, C_{eq}}{2} = \frac{(V_r)^2\, C_r}{2} = \frac{(\pi\, V_{in})^2\, C_r}{2} \tag{5}$$

From which:

$$C_{eq} = \pi^2 C_r \qquad (6)$$

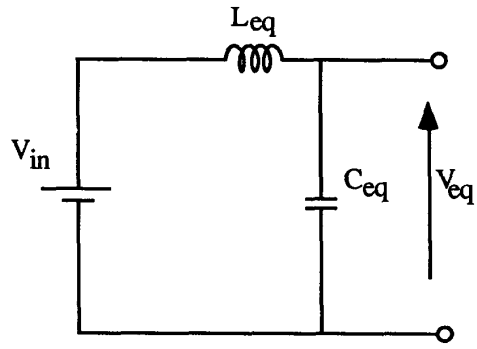


Fig. 4. Average model of the unloaded oscillator

SPICE simulations (see below) seem to support this conclusion but suggest that the average model can be refined by including some residual effect of the resonant inductor L_r. As a first approximation we added the value of L_r to the input inductor i.e. $L_{eq} \cong L_{in}+Lr/4$. Hence, the proposed low frequency model of the unloaded oscillator is as shown in Fig. 4. For the case $L_{in} > L_r/4$, the bandwidth (f_{BW}) of the unloaded system will be:

$$f_{BW} = \frac{1}{2\pi\sqrt{C_{eq} L_{eq}}} = \frac{1}{2\pi\sqrt{(Lr/4+L_{in})}} = \frac{1}{2\pi^2\sqrt{C_r(Lr/4+L_{in})}} \qquad (7)$$

The model clearly demonstrate the fact that, in steady state, the average input current to the oscillator is zero. An important corollary of this is the fact that the switches are required only to carry the current of L_{in}. That is, if L_{in} if is chosen to be sufficiently large ($L_{in} > L_r/4$), most of the resonant current will be confined to within the L_r-C_r loop. However, as implied by equation (7), a large L_{in} will reduce the bandwidth of the oscillator.That is, there is a trade off between the magnitude of the resonant current fraction that flows through the switches and the dynamic response of the converter.

The magnitude of the resonant current can be calculated by considering the fact the the steady state resonant voltage is a 'stiff' function of the input voltage:

$$I_{r(pk)} = \pi V_{in} (2\pi F_{os}) C_r \qquad (10)$$

Where F_{os} is the resonant frequency.

Elementary network considerations show that the resonant frequency is:

$$F_{os} = \frac{1}{2\pi\sqrt{C_r(4L_{in} \,||\, L_r)}} \qquad (11)$$

Hence the resonant current will be:

$$I_{r(pk)} = \pi V_{in}\sqrt{\frac{C_r}{4L_{in} \,||\, L_r}} \qquad (12)$$

Since the resonant current is a function of the input voltage and *independent* of the converter's power level, overall efficiency should improve under heavy load conditions.

The oscillator with a resistive load. Energy dissipation considerations leads to the relationship between the equivalent resistance (R_{eq}) that has to be included in the model to account for a resistive load (R) placed across the tank:

$$\frac{(V_{in})^2}{R_{eq}} = \frac{(V_r)^2}{2R} = \frac{(\pi V_{in})^2}{2R} \qquad (8)$$

Which imply:

$$R_{eq} = \frac{2}{\pi^2} R \qquad (9)$$

The loaded converter. The loaded oscillator model is developed under the assumption that the duty cycle (D) is unity. That is, that the rectifier's switch Q_{sr} (Fig. 1) is 'on' all the time. The action of the transistors Q_1 and Q_2 and the diodes D_1 and D_2 can now be emulated by toggle switches as shown in Fig.5a. Next we reflect the secondary to the primary by taking into account the turn ratio (n) of the ideal transformer (Fig. 5b, 5c). Note that in this representation the two switches S_{os} and S_{rc} are in fact the same switch namely the push pull transistors of the oscillator. As indicated before, the current through S_{os} is a fraction

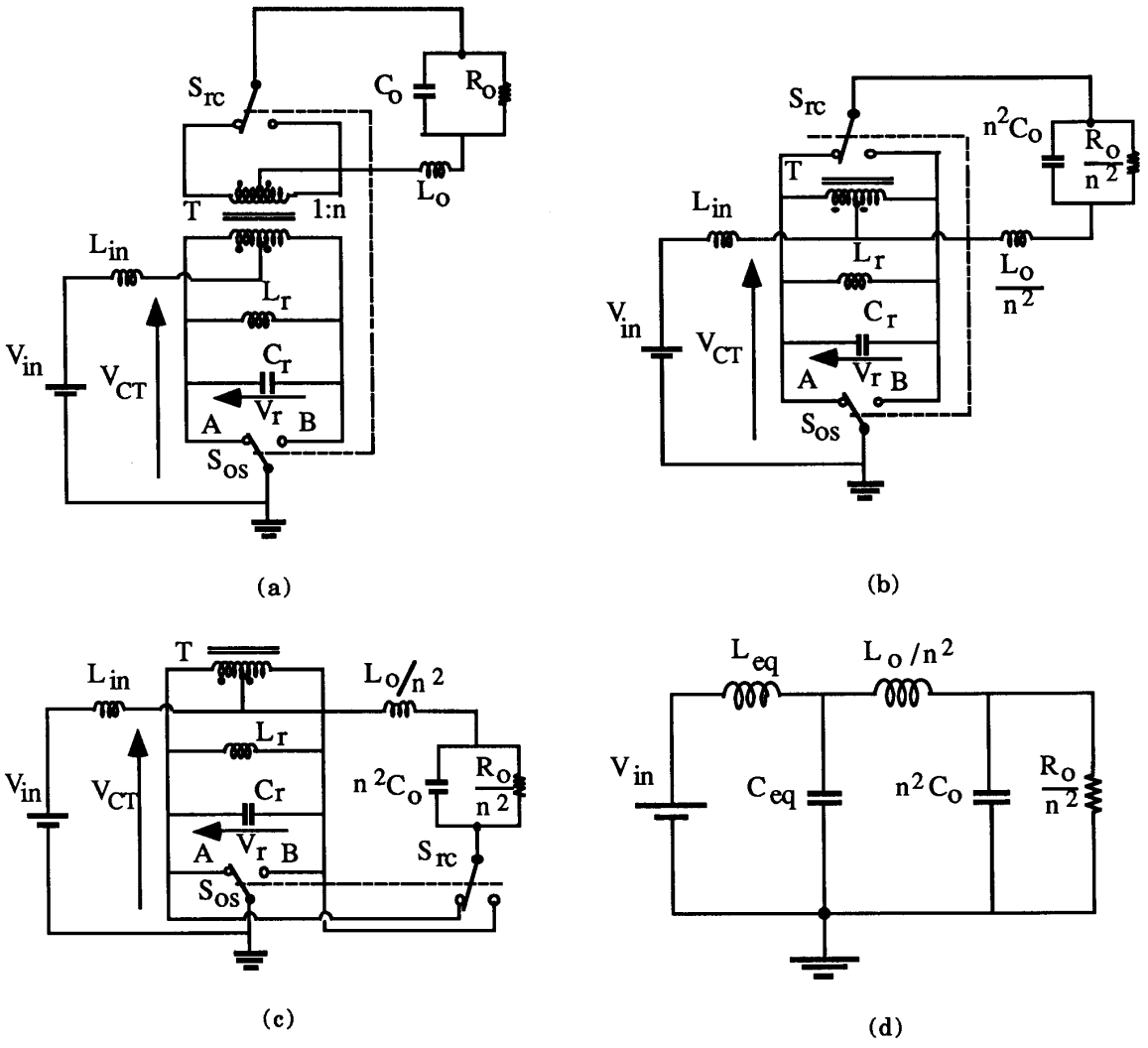


Fig. 5. The loaded oscillator. (a) original. (b) after reflecting the secondary to the primary side. (c) same as (b) but rearranged. (d) average model.

($L_r/(L_r+4L_{in})$) of the resonant current. By choosing ($L_{in} > L_r/4$), the push pull switches will practically carry only the actual load current. Applying the results for the unloaded oscillator, we can immediately arrive at the average, low frequency model of the system (Fig. 5d). Assuming that $L_o >> L_{in}, L_r$, as required for good filtering, the resonant frequency can still be approximated by equation (6).

The average model of the SOSYRC. The model of Fig. 5d assumes that the oscillator is continuously loaded. The actual situation is similar to the Buck topology as shown in Fig. 6. The PWM action can be emulated by applying the Switched Inductor Model (SIM) developed earlier [2,3]. For the sake of brevity we assume here a continuous inductor current condition. Discontinuous conditions can be also easily modeled by applying the USIM approach [4]. Applying the SIM, the complete average model of the SOSYRC is derived as shown in Fig. 7.

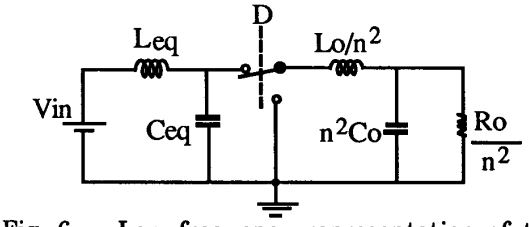


Fig. 6. Low frequency representation of the SOSYRC.

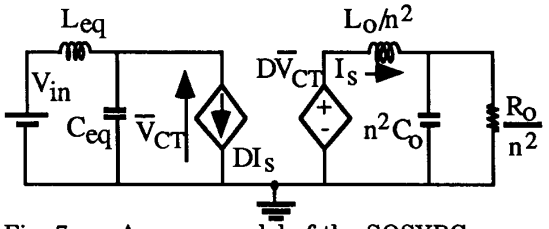
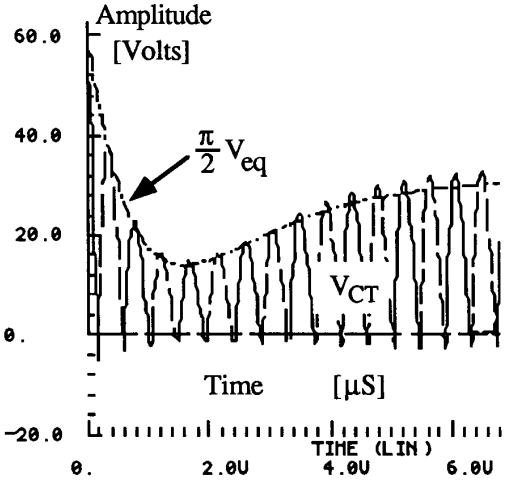
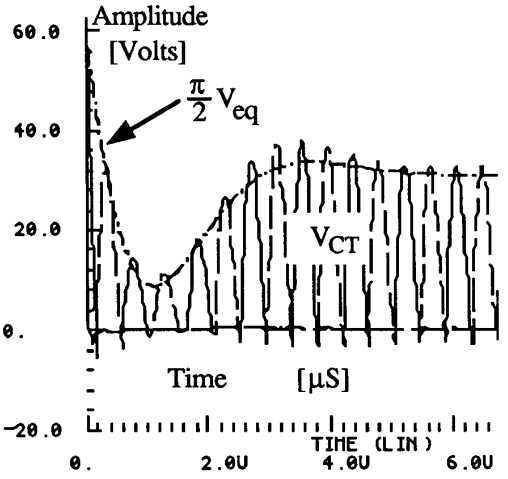


Fig. 7. Average model of the SOSYRC.



(a)



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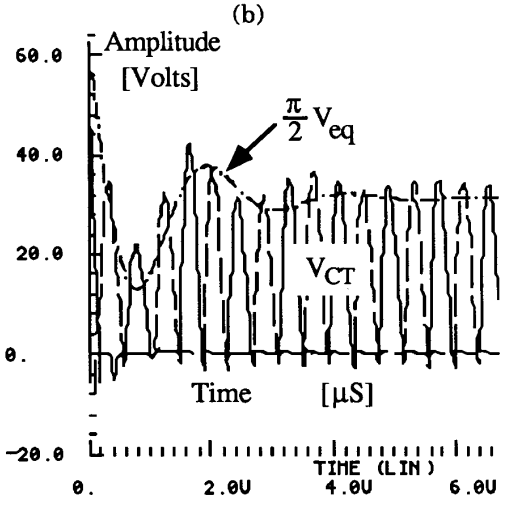


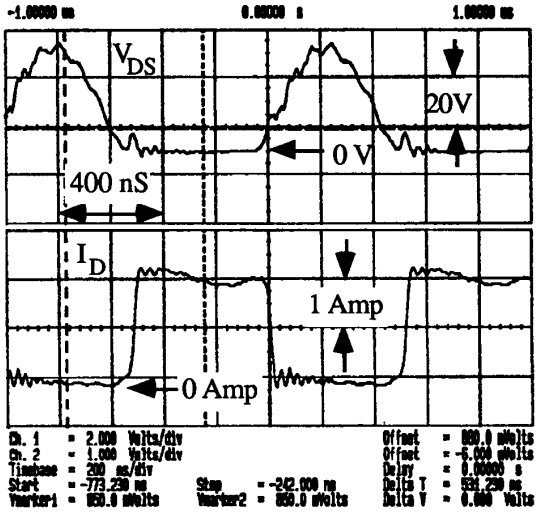
(c)

Fig 8. SPICE simulation comparison between transient response of a resistively loaded resonator and proposed equivalent circuit (Fig 4) loaded by R_{eq}. For all cases: R=70Ω; C = 4 nF; L_r = 4 μH; C_{eq} = 40 nF;$L_{eq} = L_{in} + L_r/4$;R_{eq} = 14 Ω. (a) L_{in} = 30μH. (b) L_{in} = 10μH, (c) L_{in} = 1μH.

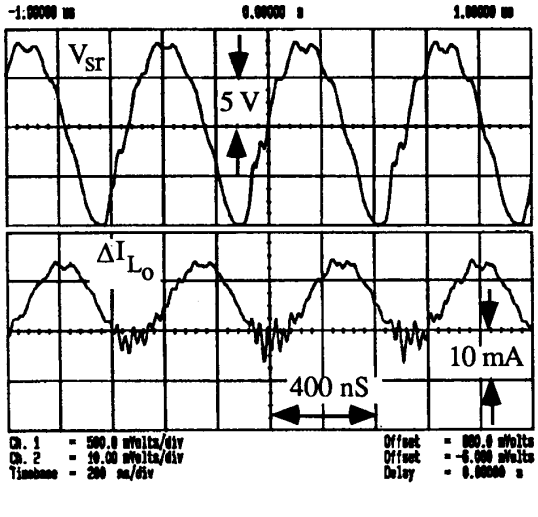
SIMULATION AND EXPERIMENTAL RESULTS

The proposed SOSYRC converter has been studied by running SPICE simulations and preliminary measurements on a prototype converter operating at the 1 MHz range. A typical time domain simulation is shown in Fig. 8. This simulation run compares the transient turn-on response of a loaded oscillator with the response of the proposed average equivalent circuit (Fig. 4). It is apparent that the proposed average

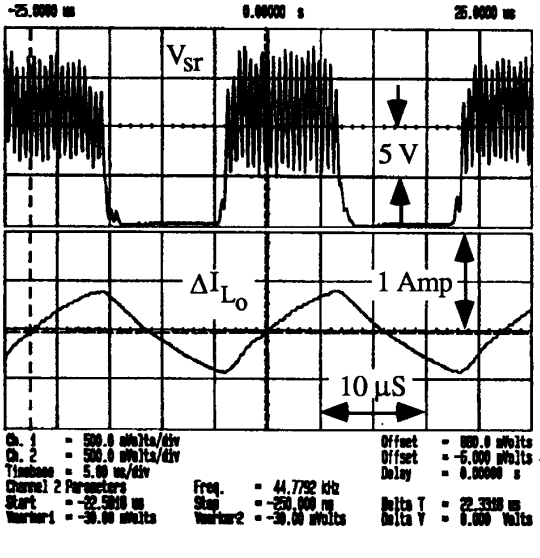
equivalent circuit is a good approximation when $L_{in} > L_r/4$. Further 'tuning' of the model is apparently needed to take into account the residual effect of L_r when the above conditions not fulfilled.



(a)



(b)



(c)

Fig. 9. Typical signal waveform of experimental SOSYRC. V_{in} =12 V. See Fig. 1 for waveform notations. (a) D=1; V_o= 10.5 V; R_L=5 Ω. (b) D=1; V_o= 10.5 V; R_L=10 Ω. (c) D=0.5; V_o= 5.1 V; R_L=2.7 Ω.

The overall efficiency of the system operating in closed loop condition was found to vary between 50% and 80% for the tested operating range (Fig. 10). The highest efficiency was obtained for the lowest input voltage tested. The worst case was found for the case of 15 V input. The main relevant effects of a higher input voltage will be a smaller duty cycle (D) and a higher voltage drop on the switches during their 'off' state. The latter may deteriorate the efficiency if true ZVS conditions are not met. Indeed, if the bias of the push pull stage is optimized for each input voltage (which was not done in the experiments of Fig. 10) the efficiency for high input voltages is improved.

DISCUSSION AND CONCLUSIONS

The preliminary SPICE simulation runs (Fig. 8) and the measured data (Fig. 9) clearly support the theoretical consideration given above including the assumption of ZVS condition (Fig. 9a). For the present experimental inverter, the push pull transistors' current is mainly the (reflected) load current with only a small fraction of the resonant current. As pointed

out above, the magnitude of this residual current is a function of the ratio (L_{in} /L_r). A large ratio will decrease this residual current but will slow down the response of the system (Fig. 8). For the experimental converter, the expected bandwidth is $f_{BW} \cong$ 700KHz (equation 7) which is fast enough to permit a PWM operation at 50KHz (Fig 9c) and possibly even at a higher frequency. Unfortunately, the output filter of the SOSYRC has to be designed for the PWM signal and hence does not benefit from the oscillator's high frequency (Fig. 9c). However since an operating frequency of 10MHz is possibly achievable with present day components, this limitation may not be that severe. Another disadvantage of the SOSYRC is the relatively high voltage stress on the push pull switches Fortunately, this situation is encountered in the 'off' state of the devices when the current is negligibly small. As shown and experimentally verified (Fig. 9a), the maximum voltage is (π V_{in}). The high stress condition is of course not unlike the situations encountered in conventional resonant converters [5] or quasi-resonant converters [6] which are subject to a high voltage stress a high current stress or both. It is expected that when the SOSYRC is properly designed, the peak voltages during transient conditions will not be much different from the steady state values. Considering the fact that only a fraction of the resonant current (I_r) passes through the switches, high efficiency at high output power is also expected. The efficiency at high frequency is enhanced by the fact that parasitic inductances and capacitances of the primary and secondary sides become part of the resonant circuit.

Higher carrier frequenciy, low switching losses and application of well studied and technology proven control methods and components make the proposed SOSYRC a viable alternative to resonant and quasi-resonant converters. An important feature, lacking in PWM and resonant converters is the ability to individually control a number of isolated outputs.

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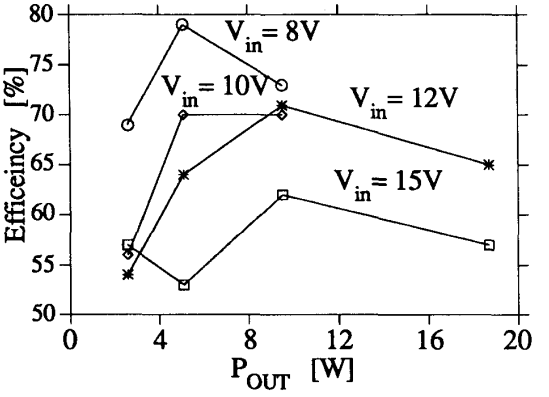

Fig. 10 Efficiency of experimental SOSYRC operated in closed loop. V_{out}= 5 V.

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