Analysis and Design of DC-Isolated Gate Drivers

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***Abstract* – A circuit for operating high-side MOSFET transistors using a ground-referred low-side driver is proposed and investigated analytically and experimentally. The circuit is implemented solely with low-cost non-inductive passive components. The targeted application is for cases in which the source of the floating transistors (N or P type) can be connected to DC buses. Design guidelines are introduced, including design considerations that were developed and verified experimentally. The inexpensive implementation is shown to introduce negligibly small losses, making it energy-efficient and cost-effective, surpassing existing flotation solutions since neither active nor inductive devices are needed.**

Keywords – DC Restorer, High-side Drive, Floating Gate Drive

I. Introduction

Driving gates of floating transistors in common power electronics systems, such as inductor-based converters and switched capacitor converters, requires designated driving systems. The driving circuitry needs to create proper isolation to overcome the voltage differences existing between the transistors' sources and the drivers' ground potential.

Present solutions achieve isolation by means of transformers or opto-couplers. However, the latter requires a floating power supply mechanism, while the former solution is limited to the high switching frequency range and to MOSFET transistors that require relatively small gate charges.

The objective of this study is to investigate a method that applies capacitive coupling in order to drive a high-side MOSFET transistor that is connected to a DC bus (such as the input or output voltage), where the latter is operated by a low-side ground-referred driver. This approach is examined and design guidelines and considerations for optimal operation are developed. The analytical predictions were verified by simulations and by experimental studies obtained from an implementation in a designated converter.

II. Gate Drive Isolation

The employment of a transformer to achieve isolation of a high-side transistor's gate from its low-side driver can be useful for high voltage applications, such as motor drives and inverter topologies [2,3]. However, this approach has its limitations. The average volt-second at the transformer needs to be zero in order to prevent core saturation, that is, high duty cycle ratios result in potentially high voltages, risking a gate-source breakdown or voltages lower than the gate's threshold voltage. At low frequencies, the core size needs to be increased substantially to be able to withstand the magnetic flux without saturating. Creative solutions must be found to apply transformers to wideband high-side drives For instance, in [1] the no-saturation 'taboo' is broken when charging the high-side gate through a series diode and letting the core saturate, resulting in a voltage drop in the secondary, which, in turn, reverse biases the diode, leaving the gate high at float. The gate is later discharged via a small drive MOSFET during the off cycle.

A second method commonly used is floating the whole driving circuitry. This requires galvanic isolation for both the drive signal and the driver's power source. The drive signal can be isolated using an opto-coupler or a transformer and the high-side power supply can range from a conventional forward converter solution to designated topologies such as [5]. A common implementation that eliminates the need for a high-side supply is the use of an IC with a bootstrap capacitor to supply the isolated driver. The capacitor charges during off periods and supplies the needed charge independently during turn-on. This solution is applicable if the source is ground-referred during off-periods for proper charge. Using a bootstrap can be problematic in high voltages, mainly because the capacitor charging diode needs to withstand the high voltages and have a minimal reverse-recovery time to prevent discharge of the bootstrap capacitor.

A different and more straightforward IC solution to the floating supply was developed in [4]. It consists of a low side driver, a high-side driver with an isolated input and a fully integrated DC-DC converter, capable of supplying additional auxiliary low-power components. This solution provides a one-chip solution at the expense of efficiency.

An alternative way to optically deliver the needed drive power also mentioned in [1], is by a Photo-Voltaic Isolator (PVI). A PVI has an IR LED at its input that reflects on PV cells connected to the output, giving enough power for driving relatively low gate-charge MOSFET transistors at low frequencies, or in applications that demand constant-on times.

Some application-specific solutions exist that do not include isolation, e.g. in Buck converters, a P-type MOSFET can be used, operated by a ground-referred inverted-output open collector driving circuit. This approach is limited to cases when the MOSFET's source voltage is lower than the gate-to-source breakdown voltage. For higher voltage differences there is a need for voltage dividers to prevent breakdown, increasing the effective resistance of the drive and limiting the possible switching frequency.

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III. Capacitive DC-Isolated Gate Driver – The Concept

This study investigates a method that applies capacitive coupling to solve the problem of driving a MOSFET transistor which is not directly connected to the driver's ground. This method is applicable to cases in which the source of the floating transistor (N or P type) can be connected to some DC bus. The constant potential difference between the ground-referred driver and the driven MOSFET's source can be decoupled using a series capacitor in between the driver and the gate. The DC voltage needed at the gate side for proper drive over the full duty cycle range is then recovered by using a diode to clamp the coupling capacitor to the DC bus voltage, thus maintaining $V_{gs} \geq 0$ for N-MOS or $V_{gs} \leq 0$ for P-MOS. As a result, during the 'on' period, the gate voltage, V_g, will be referred to the DC bus voltage, i,e. the source of the transistor.

Fig. 1 shows schematic diagrams of implementations for N and P type MOSFET switches. The two key elements are the series capacitor, C_s, and the diode, D, which initially charges the series capacitor to V_{BUS} but, in order for the drive to work properly, more features are added. As in most driver circuits, the current loop in the PCB design should be kept as small as possible to prevent overshoots caused by parasitic inductances that might interfere with the switching. In the method introduced here, a second capacitor, C_{loop}, was added between the MOSFET's source and the driver's ground input, providing an alternative low impedance path, diverting the ground loop currents from the relatively high impedance bus source voltage (Fig. 1). The capacitor should be placed in the circuit such that the loop will be as short and as small as possible. Adding a series resistor R_s damps the drive circuit, preventing overshoots from further stray inductance that might exist even after choosing an appropriate C_{loop}.

A bleeder resistor in parallel with the diode is necessary to allow C_s to follow changes in V_{BUS}. The tracking prevents the transistor from staying active during 'off' periods and, additionally, helps in preventing a potential gate-source breakdown.

IV. Analysis and Design Considerations

The size of C_s is determined by the charge delivered to the gate in each cycle. This charge depends on the desired V_{gs}, and on the voltage ripple allowed for C_s, as can be shown in (1):

$$C_s \geq \frac{Q_{gate}}{\Delta V_{C_s}}, \tag{1}$$

where ΔV_{C_s} represents the voltage ripple on C_s and Q_{gate} is the charge needed to raise the MOSFET's gate and is dependent on the operating voltage.

R_{bleed} can then be chosen, considering (2):

$$T_{transient} > R_{bleed} C_s \gg 0.5 T_s \tag{2}$$

where $T_{transient}$ is the expected circuit transient time, and T_s is the switching time. This selection allows the capacitor to follow transients in V_{BUS}, but not to discharge during 'on' periods, when there is a drive signal. C_s should not be much larger than indicated in (1) to be able to track V_{BUS}, when

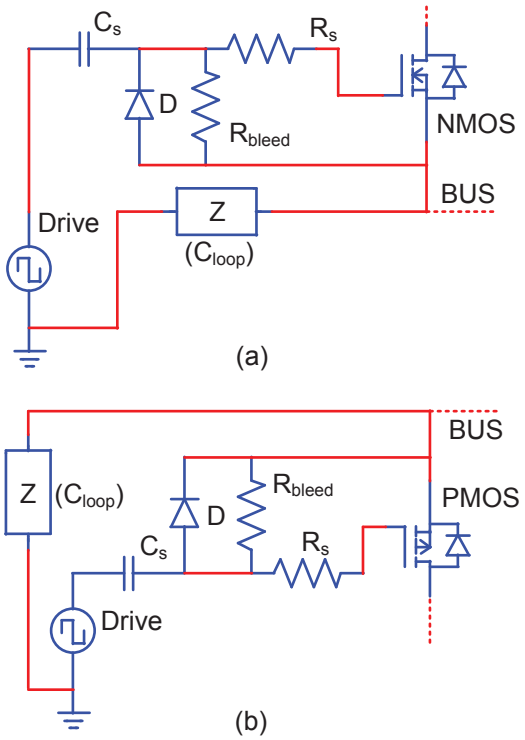

Fig. 1. A schematic diagram for the high-side driving system. (a) Implemented for N-MOS, (b) implemented for P-MOS

needed, within the expected transient time. The value of R_{bleed} must be sufficiently high to minimize energy dissipation. The selection of R_s is made such that its interference with proper charging of the gate is minimal. The drive circuit needs a harmonic quality factor value, Q, smaller than 0.5 to prevent overshoots. These factors can be expressed as in (3):

$$\begin{cases} R_s \ll \frac{T_s V_{gs}}{2Q_g} \\ R_s > 2 \cdot \sqrt{\frac{L}{C_s}}, \end{cases} \tag{3}$$

where V_{gs} is the gate-source voltage during 'on' times and L is the stray inductance element in the drive circuit.

The value of C_{loop} needs to be sufficiently high so that ripple from the bus won't affect the drive ground. Considering a maximum allowed ripple of $\Delta V_{C_{loop}}$, the capacitor value can be chosen by (4):

$$C_{loop} \geq \frac{Q_{gate}}{\Delta V_{C_{loop}}}. \tag{4}$$

$\Delta V_{C_{loop}}$ should be significantly smaller than the drive signal level to minimize ground interferences. A good value should be $\Delta V_{C_{loop}} < 0.01 V_{gs}$.

Since the gate driver sources at turn-on and sinks at turn-off, an equal amount of charge (the charge on C_s) remains constant after each cycle. This implies that the diode is only needed in order to compensate for charges lost through R_{bleed} and for stabilization during transients in V_{BUS}. Yet, a fast diode with reverse recovery time considerably shorter than the desired switching frequency is still required in order to prevent the discharge of the capacitor during drive 'on' times.

If R_{bleed} is chosen to be high enough, the energy used to replenish charge lost due to R_{bleed} is negligibly small, meaning that no excess energy is consumed due to the addition of the proposed scheme.

The switching power will then be:

$$P_{loss} = V_{supply} Q_g f \quad (5)$$

where V_{supply} is the driver's supply voltage and is usually the same as the desired V_{gs}.

V. Simulations

Simulations were performed using PSIM (PowerSim Inc.), modeling the driving scheme and using capacitors C_g to model N-MOS and P-MOS transistors (both driven by the same driver). A series inductance, L_{stray}, was added between the V_{BUS} ground reference and the drive signal ground reference to simulate parasitic inductances.

The following parameters were used, satisfying (1)-(4):

- $C_s = 0.47\mu F$
- $C_g = 5nF$
- $C_{loop} = 4.7\mu F$
- $R_s = 3.3\Omega$
- $R_{bleed} = 1.5k\Omega$
- $V_{supply} = 10V$
- $V_{bus} = 50V$
- $L_{stray} = 100\mu H$
- $f_s = 100kHz$

The simulations' basic schematic and results are depicted in Fig. 2, showing traces of V_{gs} for the N-MOS and P-MOS representations. In one simulation, two circuits were run simultaneously, one with and one without C_{loop} (Fig. 2(a)). The results displayed in Fig. 2(b) show the importance of the additional capacitance, effectively lowering the ground impedance and resulting in a low quality factor in the drive circuit, which prevents overshoots in the driven transistor's gate. When C_{loop} is omitted, a phenomenon of extra offset occurs in V_{gs}, preventing the 'off' levels from reaching zero. This is a result of C_s overcharging from the voltage overshoots caused by L_{stray}. This undesired voltage might leave the MOSFET in some conduction state, potentially causing short circuits in the converter.

In the second simulation, transient changes of 2V to V_{BUS} were added to evaluate the reaction of the circuit. It can be seen in Fig. 2(b) that transients in V_{BUS} are compensated for by R_{bleed} and the diode well within the transient time.

VI. Experimental Study

In [7], a switched-capacitor based equalization scheme is proposed for overcoming the adverse effect of shaded panels in a serially connected PV array. The proposed solution is based on a modular approach, in which each two panels are connected to a bridge topology resonant switched-capacitor converter. This equalizing switched capacitor converter (EQSCC) is designed to handle differential currents between PV panels and was found to boost the maximum available power by about 50% when interfaced with two serially

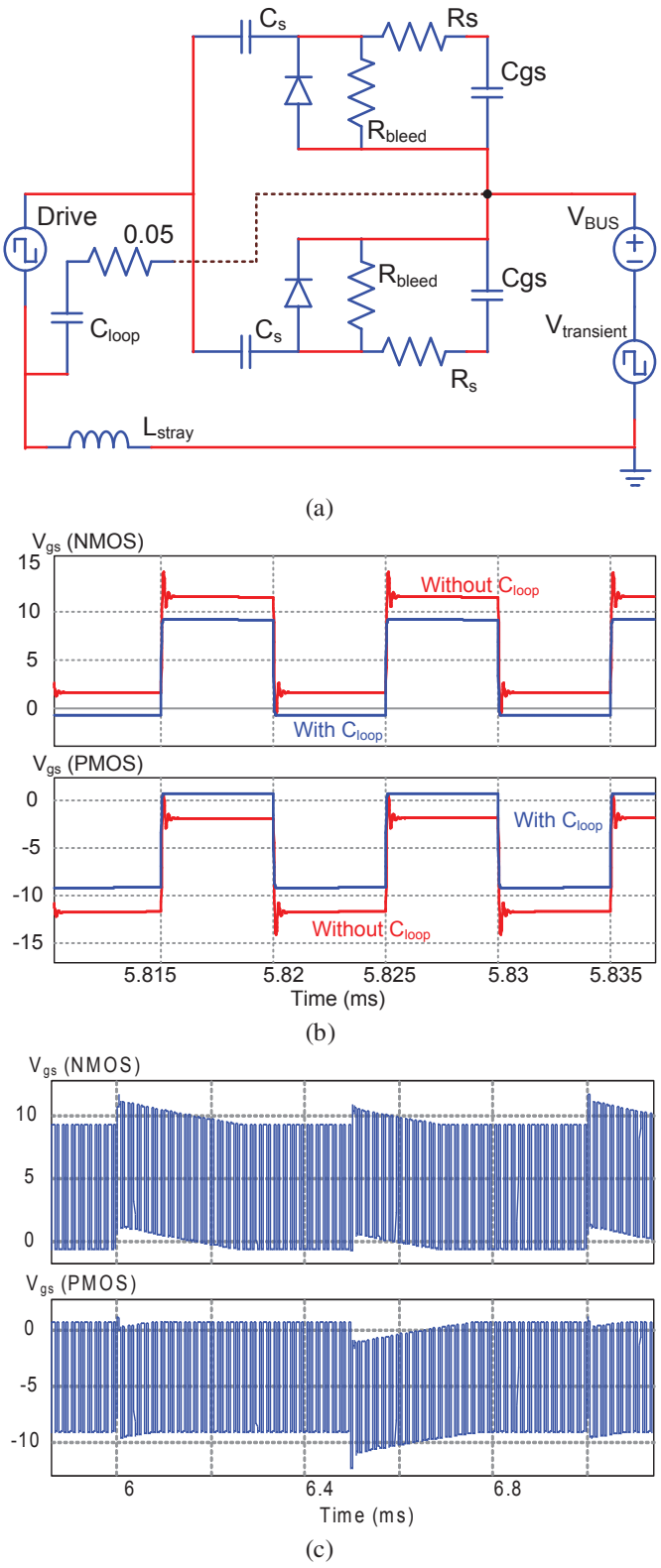

Fig. 2. The simulated circuit. (a) N-MOS and P-MOS driving topologies with the transistors represented as C_{gs} capacitors. (b) The results of simulations with and without C_{loop}. The top graph is for a N-MOS and the bottom for a P-MOS. (c) Simulation results showing transient recovery times with C_{loop}.

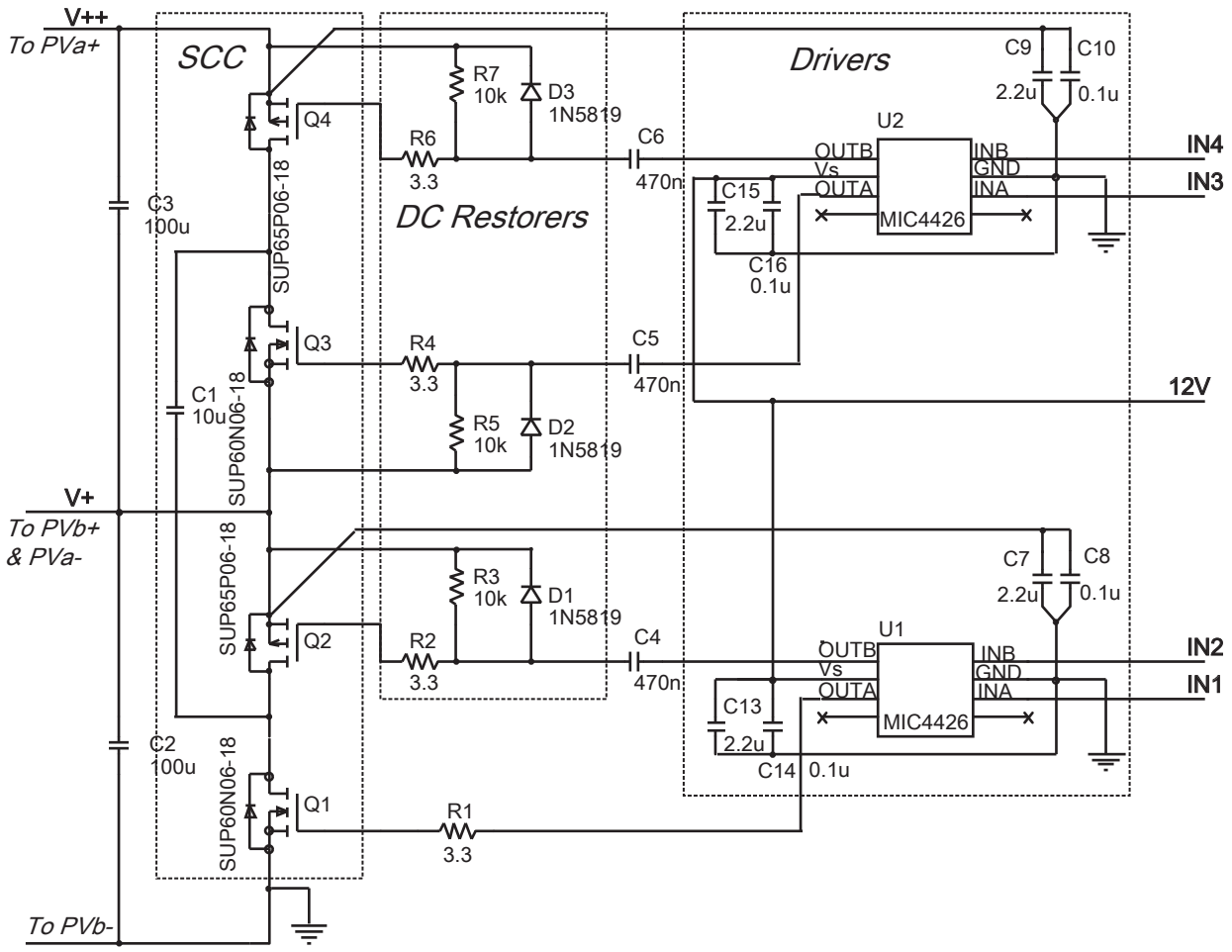

Fig. 3. Schematic diagram of the experimental EQSCC module

connected PV panels under insolation ratios between 20% and 100%. The design demands N-1 EQSCC modules for a chain of N PV panels. This creates a strong demand for budget-wise solutions that reduce the costs per-module without impacting the system's efficiency.

To avoid the use of expensive and energy-consuming isolated drivers, the studied floating mechanism was implemented. The type of power MOSFET transistors was chosen such that the sources of each transistor are connected to a DC bus, as can be seen in Fig. 3. Q1 and Q3 were chosen to be N-type MOSETs, while Q2 and Q4 were selected to be P-type MOSFETS. This made it possible to decouple the DC content of the drive signal from a ground-referred low-side driver. The DC level required to operate the high-side MOSFETs using the driver's signal can then be restored using diodes D1, D2 and D3 clamping the signal to the DC bus potentials during 'off' periods. The experimental circuit and a PCB prototype are shown in Fig. 3 and Fig. 4, respectively. The following components and parameters were used for the experimental system, satisfying (1)-(4):

- $C_s = 0.47\mu F$: C4-C6
- $C_{loop} = 2.2\mu F + 0.1\mu F$: C7-C10
- $R_s = 3.3\Omega$: R1, R2, R4, R6
- $R_{bleed} = 10k\Omega$: R3, R5, R7
- 1N5819 Diodes: D1-D3
- SUP60N06-18 N-MOS Q1, Q3. $Q_g \approx 45nC$
- SUP65P06-18 P-MOS Q2, Q4. $Q_g \approx 100nC$
- $V_{supply} = 12V$
- $V_{bus,1} \approx 22V$, $V_{bus,2} \approx 44V$
- $f_s \approx 100kHz$

In addition to the use of C_{loop}, existing ripple across the parallel bus capacitors C2 and C3 may penetrate the gate drive voltage if L_{stray} is low enough. Extra precaution is taken to ensure a high enough noise immunity by keeping ripple as low as possible. To this end, MOSFET transistors with a relatively high gate threshold voltage were chosen, providing a large margin between the threshold voltage and the gate drive signal.

In Fig. 5, the rise times are clean with no overshoots. When the N-MOS transistors open, a downwards spike in the P-MOS switches is seen. This is caused by the high dV/dt on the drains, due to the N-MOSes opening. Parasitic capacitance between the gate and the source, along with the presence of R_s, causes the gate to nudge. Lowering R_s further might be needed when operating at higher voltages in order to reduce the risk of a false 'on' on the high-side.

VII. Discussion and Conclusions

The high-side driving approach explored in this study was found to be extremely efficient for driving high-side transistors using a simple low-side driver and low-cost passive components. Experimental results agree well with simulations and with the theoretical study. Proper layout implementation, taking into consideration the precautions mentioned in this study, leads to stable operation and high noise immunity.

Although the experiment was conducted within a specific switched capacitor bridge converter application, the scheme can be applied to any configuration with a constant voltage reference, e.g. buck DC-DC converters and inverter bridges, using appropriate N-MOS and P-MOS transistors, depending on the current direction.

VIII. Acknowledgements

This research was supported by the ISRAEL SCIENCE FOUNDATION (grant No. 517/11) and by the Kamin program of the Ministry of Industry Trade and Labor (Grant No. 47189).

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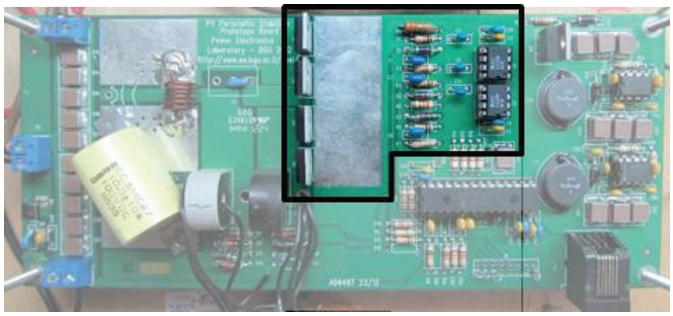

Fig. 4. The DC restoring mechanism, marked in the black contour, implemented as part of the experimental equalizing SCC prototype. Q1-Q4 are aligned from bottom to top on the left side and the drivers are on the right.

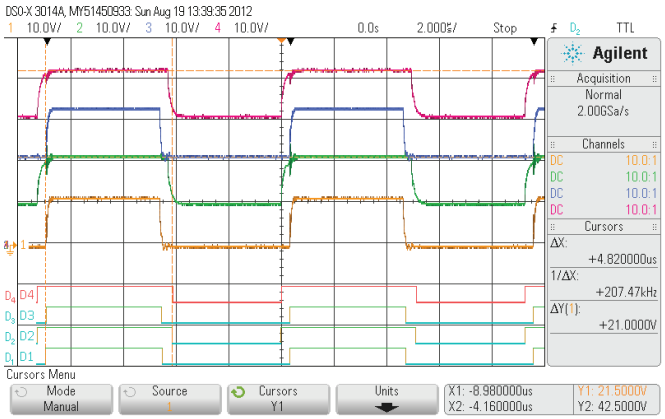

Fig. 5. Experimental gate signals, presented on digital channels D1-D4 for Q1-Q4 respectively. Q1-Q4 gate voltages are presented on analog channels CH1-CH4, respectively, (from bottom to top) all with an offset of (-11)V. Horizontal axis is 2μsec/div, vertical axis is 10V/div.