The Effect of Switching Transitions on Switched Capacitor Converters Losses

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***Abstract*—The contribution of the rise and fall times of switches to the losses of Switched Capacitors Converters was evaluated by an approximate analysis applying the equivalent resistance concept. It was found that switch turn-on and turn-off durations increase the equivalent resistance of the converter and, consequently, the losses, except in the case of complete charge/discharge of the flying capacitors within the switching phase. Loss increase is related to the fact that during the current rise/fall state, the instantaneous losses are much higher than when the switch is in a constant 'on' state. Theoretical predictions were validated by full circuit simulations and experimental results. The present study integrates the switching losses into the generic equivalent resistance loss model, enabling the calculation and/or simulation of the total losses in switched capacitor converters.**

***Index Terms*— DC-DC power converters, modeling, switched capacitor converter, switching losses.**

I. Introduction

Switched Capacitor Converters (henceforth referred to as SCC for plural and singular) suffer from a fundamental power loss due to the inherent energy dissipation when a capacitor is charged or discharged by a voltage source or another capacitor [1]. Two types of SCC have been considered in the literature; hard and soft switched SCC. The soft switched SCC employ a series inductor to achieve zero current switching [2-5]. Earlier studies [2-14], considered only conduction losses in SCC circuits and neglected switching losses. It has been postulated that there is no need to add the switching losses since they are part of the charge/discharge process and, as such, already included in the calculated losses. As revealed in this study, this conjecture is correct if during each switching phase the charge/discharge process is completed. That is, for cases where the equivalent time constant of the subcircuits is lower than the switching durations. However, when the charge/discharge process is incomplete, switching losses need to be added. The reason for this is the fact that during the rise and fall times of the current, the instantaneous losses are larger than when the switch is in the 'on' state because the effective resistances during these durations are higher than the switch resistance in the 'on' state. The objective of this study is to delineate the contribution of the switching process to switching losses in SCC systems.

The analytical approach pursued here follows the concept introduced earlier [6], in which the losses are expressed as a function of the average current passing through each flying capacitor. Since these currents are linearly proportional to the output current, the losses can easily be related to the output current of the SCC. The proposed model can be applied to derive the losses of SCC with multiple capacitors. The analysis presented here is an approximate analysis that is based on the assumption that the rise and fall times are substantially shorter than the switching phase duration. This assumption leads to simple and comprehensible expressions that can be intuitively understood and help clarify the issue of switching losses in SCC.

The paper presents some recent loss evaluation approaches and models of SCC (section II), introduces the proposed approach for the inclusion of switch transition loss in the earlier SCC loss model (section III) and presents an experimental validation of the concept, followed by a short discussion (section IV).

II. Power Loss in SCC

A generic representation of SCC is used in this study to analyze losses. It is widely accepted that for the purpose of loss calculation the SCC can be represented by a voltage source followed by a series resistance (Fig. 1), [2-14]. This serial resistance, defined as the "Equivalent Resistance", R_e,

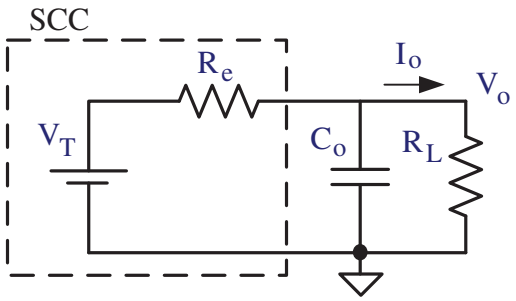

Fig. 1. Generic SCC model for loss evaluation.

represents the losses of the SCC. The voltage source, V_T, is the target voltage of the SCC, that is the no load output voltage.

In the classical approach, the capacitor losses are evaluated by:

$$E_{Loss} = \frac{\Delta V^2 C}{2} \quad (1)$$

where ΔV is an initial voltage difference between the capacitor and charging/discharging source and C is the capacitance that is being charged or discharged . This approach can only be used in the case where the charge/discharge process of the capacitor is completed within the switching period. However, loss calculation by (1) is impractical in SCC that include a multitude of switches and flying capacitors, since it is extremely difficult to evaluate ΔV for each switching phase.

Previous studies reported other, more workable approaches for the evaluation of the losses in SCC [6-9]. It was found that the losses of SCC have two limiting values, depending on the ratio of the switching duration, T_i, and the time constant of the charge/discharge circuit, R_iC_i, where for each subcircuit, i, C_i is the total capacitance of the i^{-th} charge/discharge loop and R_i is the total i^{-th} loop resistance. For the case that $T_i >> R_iC_i$, which is referred to as "Complete Charge" mode (CC), the equivalent resistance depends on the frequency and the capacitance (2), as in the classical case. For the case that $T_i << R_iC_i$, which is referred to as the "No Charge" mode (NC), the equivalent resistance is frequency independent and is a function of the total charge/discharge loop resistance R_i (3) [13, 14].

$$R_{e_i(CC)} = \frac{1}{f_s C_i} \quad (2)$$

$$R_{e_i(NC)} = 2R_i \quad (3)$$

In order to cover all the operation modes and, particularly, the intermediate mode, the "Partial Charge" mode (PC) (an empirical equation (4)) was proposed in [8, 15] to estimate the SCC losses in between the two boundaries of (2, 3).

$$R_{e_i} = \sqrt[p]{R^p_{e_i(NC)} + R^p_{e_i(CC)}} \quad (4)$$

The factor 'p' used in this estimation is equal to 2. Recent studies [16] have shown that a better estimation is available from an empirical equation. By analysing the closed form solution for equivalent resistance [6], Makowski, [16] has found that a better fit is obtained when 'p' is equal to 2.54. Two empirical approximations, along with the closed form solution for normalized equivalent resistance (5) as a function of switching frequency of SCC, are compared in Fig. 2. It should be noted that the rest of the circuit parameters are kept constant.

$$R^*_{e_i} = \frac{R_{e_i}}{R_i} \quad (5)$$

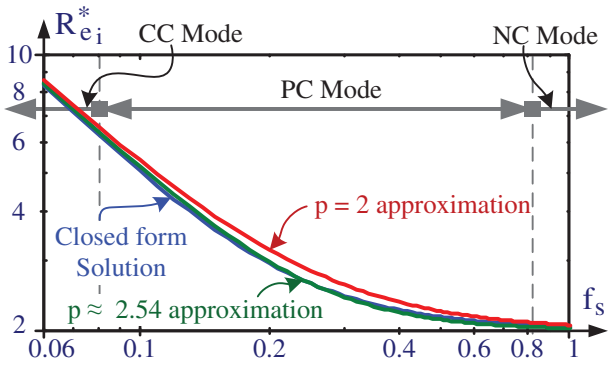

Fig. 2. Comparison of two empirical approximations of equivalent resistance to the closed form solution.

It can be concluded from Fig. 2 and from (2, 3) that, on the one hand in the classical case (the CC operation mode), SCC conduction losses are independent of the charge/discharge loop resistance, R_i (2). The waveform and, consequently, the switch rise and fall times have no impact on the losses. On the other hand, in the NC operation mode the impact of R_i on the SCC losses is obvious (3). Here (NC mode) the rise and fall times of the switch will affect the losses since they introduce a significant change in the current waveform and, consequently, in its RMS value. Hence, rise and fall processes need to be taken into account while calculating the losses. Detailed analysis of these losses follows.

III. Approximate Analysis of the SCC Losses Including the Switching Transitions

For the sake of clarity and brevity we consider the case of a 1:1 SCC, as depicted in Fig. 3. The analysis is made under the assumption that the input voltage, V_{in}, and output voltage, V_o, are constant over a switching cycle, the switches S_1 and S_2 have 'on' resistances of R_{S1} and R_{S2} respectively, the flying capacitor, C, has a series loss component R_{ESR} and that the switches connect the flying capacitor, C, to V_{in} and V_o during the times T_1 - charging phase i = 1, and T_2 - discharging phase i = 2, respectively. These 'on' times include the rise time and fall times, t_r, t_f, of the switches, respectively. The switching frequency is f_s and the switching period $T_s = 1/f_s$. Note that due to possible dead time between switch transitions, the total duration, $T_1 + T_2$, may be smaller than T_s. The generic charge/discharge process for each switching phase, T_i , can be represented by the basic equivalent circuit of Fig. 4 [6], in which ΔV_{0i} (i = 1,2) is the initial voltage difference between

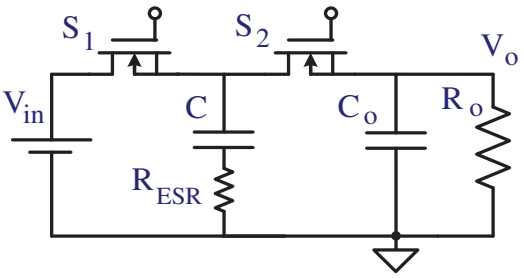

Fig. 3. Hard switched unity gain SCC.

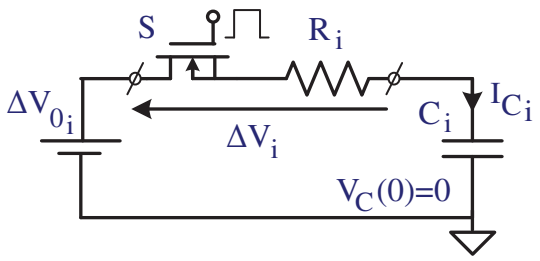

Fig. 4. Equivalent circuit of a charge (i = 1) or discharge (i = 2) process.

the capacitor and the corresponding voltage source (V_{in} or V_o in present example), R_i is the total resistance of the loop (switch 'on' resistance and capacitor's ESR), C_i is the equivalent capacitance of the loop and the initial voltage across C_i is zero (Fig. 4). The MOSFET switch, S, in the model of Fig. 4 represents the fact that the rise and fall times of the loop current are not instantaneous. Depending on the relationship between the time constant, R_iC_i, and the switching time, T_i (T_1 and T_2 in this private case), the charge/discharge process may take one of three possible forms (Fig. 5) [6, 13, 14].

A. The effect of the switching process when $T_i >> R_iC_i$
'Complete Charge' – 'CC' mode

This is the classical case, discussed in many text books, in which the capacitor is fully charged to ΔV_{0i} during the switching phase, T_i (Fig. 5a). The term "average capacitor current - I_{Cavi}" in this paper means the current averaged over the full switching period, T_s, or, in other words, the total charge transferred to/from a capacitor divided by the total switching period of the converter. Thus, the average capacitor current, I_{Cavi}, is related to the initial voltage, ΔV_{0i} , by:

$$\Delta V_{0_i} = \frac{I_{Cav_i} T_s}{C_i} \tag{6}$$

The energy loss in this classical case, $E_{(a)i}$, during the switching phase T_i is:

$$E_{(a)_i} = \Delta V_{0_i} \cdot I_{Cav_i} T_s - \frac{(\Delta V_{0_i})^2 C_i}{2} = \frac{(I_{Cav_i} T_s)^2}{2C_i} \tag{7}$$

Since the average capacitor current, I_{Cavi} , is linearly proportional to the SCC output current, I_o , by a factor k_i [6-9], the contribution of the switching phase, T_i , to the average power loss of the SCC is:

$$P_{(a)_i} = I_o^2 \left[k_i^2 \frac{1}{2 f_s C_i} \right] \tag{8}$$

and the total power loss (charge plus discharge phases) for the symmetrical 1:1 SCC ($C = C_i$, k_i=1 (for i = 1,2) [6]) is:

$$P_{(a)} = I_o^2 \left[\frac{1}{f_s C} \right] \tag{9}$$

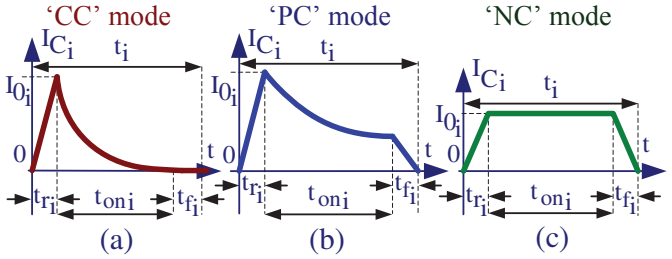

Fig. 5. Possible variants of capacitor current waveforms when the charge or discharge process is: (a) Complete ($T_i >> R_iC_i$); (b) Partial ($T_i \cong R_iC_i$); (c) 'No Charge' ($T_i << R_iC_i$).

As expected, the total power loss is independent of the rise and fall times and, in fact, of the charge/discharge current shape [2, 3, 6-9, 13, 14]. As shown earlier [6, 13] the term multiplying $(I_o)^2$ in (9) is the output resistance of the generic SCC average model [6].

B. The effect of the switching process when $T_i \cong R_iC_i$
'Partial Charge' – 'PC' mode

The evaluation of this intermediate case, depicted in Fig. 5b and in further detail in Fig. 6, is carried out under the assumption that the rise and fall time intervals are relatively short compared to the 'on' time, and consequently, the voltage ΔV_i across the loop resistance R_i and switch S (Fig. 4) is constant during these short intervals (Fig. 6).

The charges transferred during rise time, Q_{ri}, on time, Q_{oni} , and fall time, Q_{fi} (Fig. 6), are:

$$Q_{r_i} = \frac{\Delta V_{0_i}}{2R_i} t_{r_i} \; ; Q_{on_i} = \Delta V_{0_i} C_i \left[1 - e^{-\beta_i}\right] ; Q_{f_i} = \frac{\Delta V_{0_i}}{2R_i} e^{-\beta_i} \cdot t_{f_i} \tag{10}$$

where $\beta_i = t_{on}/(R_iC_i)$. The total charge, Q_T, transferred during the time period T_i is the sum of Q_{ri}, Q_{oni} and Q_{fi}, and its relationship to the output current [6] is:

$$I_o = Q_T \cdot f_s / k_i \tag{11}$$

Combining (10) and (11), ΔV_{0i} can now be expressed as a function of output current:

$$\Delta V_{0_i} = \frac{2R_i \cdot k_i \cdot I_o}{f_s \cdot \left[t_{r_i} + 2R_iC_i \left(1 - e^{-\beta_i}\right) + t_{f_i} \cdot e^{-\beta_i} \right]} \tag{12}$$

The energy losses during rise time, E_{ri}, 'on' time, E_{oni} and fall time, E_{fi}, (Fig. 6) are:

$$E_{r_i} = \frac{\Delta V_{0_i}^2}{2R_i} t_{r_i} \; ; E_{on_i} = \frac{\Delta V_{0_i}^2 C_i}{2} \left(1 - e^{-2\beta_i}\right) ; E_{f_i} = \frac{\Delta V_{0_i}^2}{2R_i} e^{-2\beta_i} \cdot t_{f_i} \tag{13}$$

The total power dissipated during time interval T_i, is equal to the sum of E_{ri}, E_{oni} and E_{fi} multiplied by switching frequency:

$$P_{avg_i} = \Delta V_{0_i}^2 \cdot \frac{f_s}{2R_i} \cdot \left(t_{r_i} + R_iC_i (1 - e^{-2\beta_i}) + t_{f_i} \cdot e^{-2\beta_i} \right) \tag{14}$$

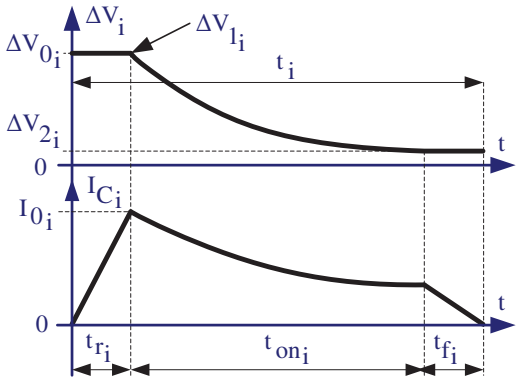

Fig. 6. Detailed waveforms of the 'PC' mode ($T_i \cong R_iC_i$): Upper trace: voltage ΔV_i across resistance R_i and S; Lower trace: current through the capacitor, according to the notations in Fig. 4.

Substituting (12) into (14) and tidying results in the expression for the average power loss of i^{-th} subcircuit operating in the 'PC' mode:

$$P_{(b)_i} = I_o^2 \cdot \left(k_i^2 \cdot \frac{2 \cdot R_i}{f_s} \cdot \frac{t_{r_i} + R_iC_i(1-e^{-2\beta_i}) + t_{f_i} \cdot e^{-2\beta_i}}{\left[t_{r_i} + 2R_iC_i\left(1-e^{-\beta_i}\right) + t_{f_i} \cdot e^{-\beta_i} \right]^2} \right) \quad (15)$$

For the symmetrical 1:1 SCC ($T_i = T_1 = T_2 = T_s/2$, $R = R_1 = R_2$, $\beta = 1/(2T_sRC)$):

$$P_{(b)} = I_o^2 \cdot (4R) \cdot \left\{ \frac{1}{f_s} \cdot \frac{t_r + RC(1-e^{-2\beta}) + t_f \cdot e^{-2\beta}}{\left[t_r + 2RC\left(1-e^{-\beta}\right) + t_f \cdot e^{-\beta} \right]^2} \right\} \quad (16)$$

When $t_{ri} = t_{fi} = 0$, the results converge to the expression found earlier for the zero rise and fall times case [6].

$$P_{(b)}\Big|_{t_r = t_f = 0} = I_o^2 \left\{ \frac{1}{Cf_s} \cdot \frac{(1+e^{-\beta})}{(1-e^{-\beta})} \right\} \quad (17)$$

C. The effect of the switching process when $T_i << R_iC_i$
'No Charge' – 'NC' mode

In this region, the current waveform is of a trapezoidal shape (Fig. 5c), while ΔV_i is practically constant. The loss for this case was evaluated by applying the Taylor series expansion to calculate the boundary value of (15) when $\beta_i << 1$:

$$P_{(c)_i} = I_o^2 \left(k_i^2 \frac{R_i}{f_s\left(\frac{t_{r_i}}{2} + t_{on_i} + \frac{t_{f_i}}{2}\right)} \right) \quad (18)$$

The total power loss for the symmetrical 1:1 converter is thus:

$$P_{(c)} = I_o^2 \left(\frac{2R}{f_s\left(\frac{t_r}{2} + t_{on} + \frac{t_f}{2}\right)} \right) \quad (19)$$

Here again, the finite rise and fall times increase the losses. In the limiting case, when $t_r = t_f = 0$ and $t_{on1} = t_{on2} = 1/2T_s$, (19) reduces to the limit value of 4R, as expected [2, 6-9, 14].

IV. Experimental Study

The analytical derivations outlined above were verified with experiments that were carried out on an SCC similar to the one described in Fig. 3, which included adjustable transition times (rise time, 'on' time and fall time of the switches). Breadboard parameters were: V_{in} = 10V, $S_{1,2}$ – IRF540, total switch ON resistance was adjusted to 750mΩ by adding a series resistor, R_O = 11.9Ω, switching frequency of 5 to 150 kHz, C_O = 470μF with R_{ESR} = 44mΩ (for the simulation assumed to be zero), flying capacitor C = 22μF with R_{ESR} = 100mΩ and switch rise/fall times of 50ns to 10μs. The switch in the discharging phase of the converter was driven so as to achieve a slow rise time, while the charging phase was not controlled. Gate signals and flying capacitor current for the 'NC' mode ($T_i << R_iC_i$, f_S = 150 kHz) are shown in Fig. 7. Two current waveforms are shown for the 'CC' mode, ($T_i >> R_iC_i$, f_S = 5 kHz). Fig. 8a shows the case of fast rise time of both phases with an output voltage of 5.63V. Fig. 8b is for the case of a significantly slower rise time in the discharge phase and the output voltage is still 5.63V, as predicted in section II.A. A comparison of experimental and calculated output voltage values is presented in Fig. 9. Experimental points for both fast and slow rise times coincide with the calculated values. As expected, the rise time had no impact on the losses in the 'CC' mode – that was obtained at lower frequencies. At higher frequencies, which induced the 'PC' and 'NC' modes, the impact of rise time becomes more significant, increasing the losses and lowering the output voltage as the frequency goes up. Due to experimental limitations, the gate voltage included a dead time (Fig. 7, lower trace), which also increased the losses due to the higher RMS current for a given average current. However, the contribution of the dead time is much smaller than that of the rise and fall time.

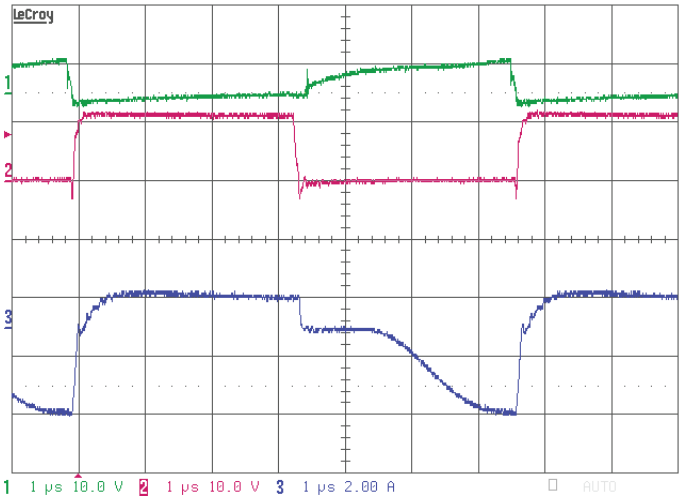

Fig. 7. Experimental waveforms in the 'NC' mode, $T_i << R_iC_i$, f_S = 150kHz: Upper trace – S_2 gate signal, discharging switch; Middle trace – S_1 gate signal, charging switch; Lower trace - Flying capacitor current.

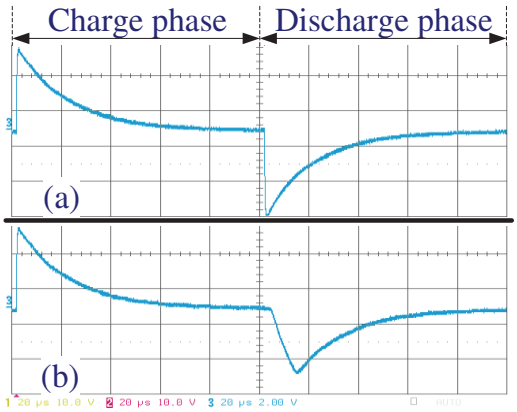

Fig. 8. Flying capacitor current waveforms in 'CC' mode with a different rise time in the discharge phase: (a) Fast rise time, $V_O = 5.63V$; (b) Slow rise time, $V_O = 5.63V$.

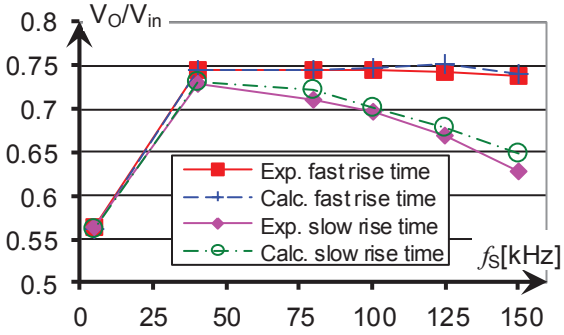

Fig. 9. Output voltage at different operational modes. Experimental results (lines): Square marks - fast rise times, diamond marks - slow rise times. Model calculation results (dashed lines): Plus marks - fast rise times, circle marks - slow rise times.

V. Discussion and Conclusions

The results of this study - that were verified by simulation and experiments - clearly show that in the 'PC' and 'NC' modes the current rise and fall times increase the SCC losses. The additional loss phenomenon can be explained by the fact that the finite transitions reduce the effective current conduction. Hence, for the same average current, the RMS current will be higher, which results in increased losses. This loss increase needs to be taken into account in the design of SCC systems running at high switching frequencies. For the sake of brevity and clarity, the expressions for power loss were developed here in relation to the 1:1 SCC that has recently been proposed as part of an energy storage system for Electric and Hybrid Vehicles, [17]. Nonetheless, the proposed analytical approach can be applied to derive the losses of multi capacitor and multiphase systems [6, 13, 18], as well as in SCC-based DC to AC converters [19], if each of the SCC subcircuits can be described or approximated by a first order RC system [6, 13].

Acknowledgment

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