THE BEST OF BOTH WORLDS: FIBONACCI AND BINARY SWITCHED CAPACITOR CONVERTERS COMBINED

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Abstract

A simple algebraic approach to synthesis Fibonacci Switched Capacitor Converters (SCC) is analyzed and the expected losses are estimated. The proposed approach reduces the power losses by increasing the number of target voltages. The synthesized Fibonacci SCC is compatible with the binary SCC and uses the same switch network. This feature is extremely beneficial since it provides the option to switch between the binary and Fibonacci target voltages, increasing thereby the resolution of attainable conversion ratios. The theoretical results were verified by experiments.

1. Introduction

Switched Capacitor Converters (hereinafter SCC for both singular and plural), which are often referred to as charge pumps, are embedded in VLSI chips and used as standalone power converters for low-power applications. It is well known that the SCC exhibits high efficiency only when its output voltage V_o is very close to the target voltage $V_{TRG}=M\cdot V_{in}$, where M is the no-load conversion ratio. The SCC efficiency can be approximated by $\eta=V_o/V_{TRG}$ and decreases when the SCC is loaded. This efficiency drop is due to the inherent power losses, which can be modeled by an equivalent circuit (Fig. 1) that includes the target voltage source V_{TRG} and a single equivalent resistor R_{eq}. This resistor represents the losses due to power dissipation in switch resistances and capacitors' ESR [1-3]. The simplified model of Fig. 1 does not take into account losses due to gate drives, leakage current and other parasitic effects which are not addressed in this work. Neglecting the parasitic effects, high efficiency is obtained if the equivalent resistor is small. In this case V_o will be very close to V_{TRG}.

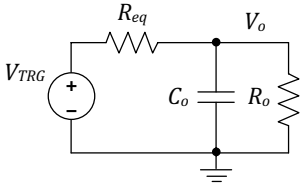


Fig. 1: The equivalent circuit of SCC

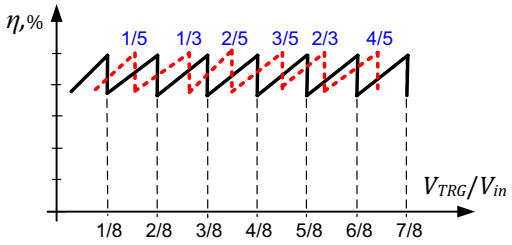


Fig. 2: The expected total efficiency.

In many applications there is a need to maintain a constant output voltage under input voltage variations or to provide different output voltages for different operational modes of a system. Such a voltage control can be accomplished by adjusting the parameters R_{eq} or M or both [4]. The highest efficiency will be obtained if R_{eq} is kept as small as possible and M is changed as required. This, however, is a difficult problem since M depends on the SCC topologies and can take only discrete values. The attempts to introduce multiple values of M have resulted hitherto in a large number of capacitors and switches that increase the power losses.

An effective way to realize many target voltages is the binary SCC [2], [5] that exhibits a binary resolution. That is, for n capacitors the number of target voltages will be 2^n-1 with a resolution of $1/2^n$. This binary behavior is depicted by solid line in Fig. 2 for n=3, while the values on the x-axis represent the binary conversion ratios. The objective of this study was to introduce additional target voltages to the binary SCC without adding capacitors or switches.

This paper covers in detail all the steps involved in the synthesis of a Fibonacci SCC proposed in [6], including the derivation of the analytical expressions of the losses that are R_{eq}. The dashed line in Fig. 2 depicts the additional efficiency peaks, which are obtained by the insertion of the proposed Fibonacci target voltages between their binary counterparts.

2. Signed Fibonacci Representation

The proposed approach to synthesis of Fibonacci SCC is based on the novel number system described in this section. For i >2 the Fibonacci numbers are defined as $F_i = F_{i-1} + F_{i-2}$, where the initial values are F_1=F_2=1. First eight Fibonacci numbers are shown in Table I.

Table I. The Fibonacci numbers for $i \le 8$

i	1	2	3	4	5	6	7	8
F_i	1	1	2	3	5	8	13	21

According to Zeckendorf's theorem [7-12] any integer number N_n in the range $(1, F_{n+2})$ can be represented uniquely as a sum of distinct Fibonacci numbers:

$$N_n = \sum_{j=0}^{n} A_j F_{n-j+2} \tag{1}$$

where A_j takes the values of 0 or 1; and n sets the resolution. Incrementing the index j, we get the largest Fibonacci number F_{n+2} in the leftmost position as shown in Table II for n=6.

Table II. The Fibonacci weights for n=6

j	0	1	2	3	4	5	6
F_{n-j+2}	21	13	8	5	3	2	1

For the sake of brevity the Zeckendorf expansion of N_n is called hereinafter Z-code. Table III shows the Z-codes for different numbers $N_n \le 5$ (n = 1...3). Note that unlike the regular binary code, the Z-code does not comprise two consecutive "1"s.

Table III. The Z-codes for $N_n \le 5$

N_n	A_0	A_1	A_2	A_3
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	0	1	0	1
5	1	0	0	0

We define the Signed Fibonacci Representation (SFN) for fractions $M_n = N_n/F_{n+2}$ in the range (0, 1) as follows: the expression (1) is normalized to the largest Fibonacci number F_{n+2}, and the coefficients A_j ($j \ge 1$) are allowed to take three values of 0, 1, and −1 as was done in [13]. The SFN also includes a leading coefficient A_0, which could be either 0 or 1. Namely,

$$M_n = A_0 + \sum_{j=1}^{n} A_j \frac{F_{n-j+2}}{F_{n+2}} \tag{2}$$

where n sets the resolution. Due to A_j taking the extra value of −1, a number of different SFN codes can represent the same fraction M_n, for example:

$$\begin{aligned} {}^4/_5 &= 1 - 1\cdot({}^3/_5) + 1\cdot({}^2/_5) + 0\cdot({}^1/_5) \rightarrow \{1\ \text{-}1\ \ 1\ 0\} \\ {}^4/_5 &= 1 + 0\cdot({}^3/_5) - 1\cdot({}^2/_5) + 1\cdot({}^1/_5) \rightarrow \{1\ 0\ \text{-}1\ \ 1\} \\ {}^4/_5 &= 1 + 0\cdot({}^3/_5) + 0\cdot({}^2/_5) - 1\cdot({}^1/_5) \rightarrow \{1\ 0\ \ 0\ \text{-}1\} \end{aligned} \tag{3}$$

These different codes can be obtained by the spawning rule, which is based on the identity $2F_i = F_{i+1} + F_{i-2}$.

This identity states in fact that addition of two "1"s in the Fibonacci code induces two carries. One goes one bit left, while the other goes two bits right [14], [15].

A rule for spawning the SFN codes:

This procedure is iterative and starts with the Z-code of M_n. Skipping the zeros from the left add "1" to first A_j = 1. This will turn A_j to "0" and induce two carries. To keep the original M_n value add "−1" to the resulting A_j = 0 and generate thereby a new SFN code. The procedure is repeated for all A_j = 1 in the original code and for all A_j = 1 in each new SFN code.

Corollary 1: For a resolution n, the minimum number of SFN codes for a given M_n is $n + 1$. This is because each of the "1"s in the Z-code with resolution n produces a new SFN code and two carries. Further iterations cause the carries to propagate, so that each "0" in the Z-code is turned to "1", which is also operated on to spawn a new code. So, the minimum number of codes is the original code plus n that is, $n + 1$.

Corollary 2: Each A_j = 1 in either the Z-code or spawned SFN code yields at least one A_j = −1 in the same position j of another SFN code. This is because the spawning procedure turns each "1" to "−1".

The example given in Fig. 3 shows how three different SFN codes for M_3=3/5 are spawned from the Z-code {0 1 0 0}. Note that operating A_3=1 in the code {1 -1 0 1} leads to the overflow, which can be disregarded since F_0/F_5=0. Another overflow takes place when "1" is added to A_2 =1 in the SFN code {1 -1 1 -1}. Since F_1/F_5=1/5 we add "1" to A_3=−1 and obtain "0". The SFN codes for other M_n, n=1...3 are given in Table IV.

1	${}^3/_5$	${}^2/_5$	${}^1/_5$
0	1	0	0
	+1		
1	0	0	1
	−1		
1	−1	0	1

1	${}^3/_5$	${}^2/_5$	${}^1/_5$	${}^1/_5$	0
1	−1	0	1		
			+1		
1	−1	1	0	0	1
			−1		
1	−1	1	−1		

1	${}^3/_5$	${}^2/_5$	${}^1/_5$	${}^1/_5$
1	−1	1	−1	
		+1		
1	0	0	−1	1
		−1		
1	0	−1	0	

Fig.3: Spawning the SFN codes for M_3=3/5 from the initial Z-code {0 1 0 0}.

3. Translating the SFN Codes to SCC Topologies

The rules for translating the SFN codes into SCC topologies follow the rules given in [2], [5]. Consider a step-down SCC including a voltage source V_{in}, a set of n flying capacitors C_j and output capacitor C_o, which is paralleled with load R_o. For a given M_n the interconnections of V_{in}, C_j, and C_o are carried out according to the next rules:

Table IV. The SFN codes for fractions M_n, n = 1...3

M_3=1/5				M_2=1/3			M_3=2/5				M_1=1/2		M_3=3/5				M_2=2/3			M_3=4/5			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_0	A_1	A_2	A_3	A_0	A_1	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_0	A_1	A_2	A_3
0	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	1
0	0	1	-1	0	1	-1	0	1	-1	1	1	-1	1	-1	0	1	1	-1	1	1	-1	1	0
0	1	-1	0	1	-1	0	0	1	0	-1			1	-1	1	-1	1	0	-1	1	0	-1	1
1	-1	0	-1				1	-1	0	0			1	0	-1	0				1	0	0	-1

1) If $A_0 = 1$ then V_{in} is connected in a polarity that charges the output.
2) If $A_0 = 0$ then V_{in} is not connected.
3) If $A_j = -1$ then C_j is connected in charging polarity (same as the output).
4) If $A_j = 0$ then C_j is not connected.
5) If $A_j = 1$ then C_j is connected in discharging polarity (opposite to the output).

The above rules are illustrated by translating the SFN codes of M_3=3/5 to topologies depicted in Fig. 4.

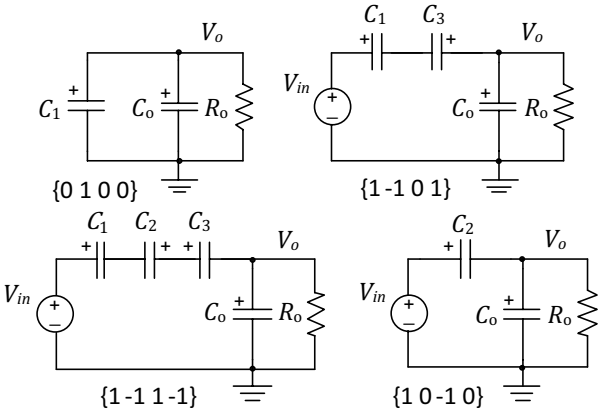


Fig. 4: The topologies of step-down Fibonacci SCC with M_3=3/5.

Let us assume that under the steady-state condition all the capacitors in the topologies of Fig. 4 are charged to constant, but unknown voltages V_1, V_2, V_3, and V_o. To find these voltages we apply Kirchhoff's Voltage Law (KVL) to each topology which leads to a system of four linear equations:

$$\begin{cases} 0\cdot V_{in} + 1\cdot V_1 + 0\cdot V_2 + 0\cdot V_3 = V_o \\ 1\cdot V_{in} - 1\cdot V_1 + 0\cdot V_2 + 1\cdot V_3 = V_o \\ 1\cdot V_{in} - 1\cdot V_1 + 1\cdot V_2 - 1\cdot V_3 = V_o \\ 1\cdot V_{in} + 0\cdot V_1 - 1\cdot V_2 + 0\cdot V_3 = V_o \end{cases} \quad (4)$$

Solving (4) we obtain the voltages across the output and flying capacitors: V_o=V_1=(3/5)V_{in}; V_2=(2/5)V_{in}; V_3=(1/5)V_{in}. Considering the fact that (4) is solvable it should also be solvable if V_{in} and V_o are interchanged. This means switching the input and output terminals and in fact, turning the step-down SCC into a step-up as shown in Fig. 5.

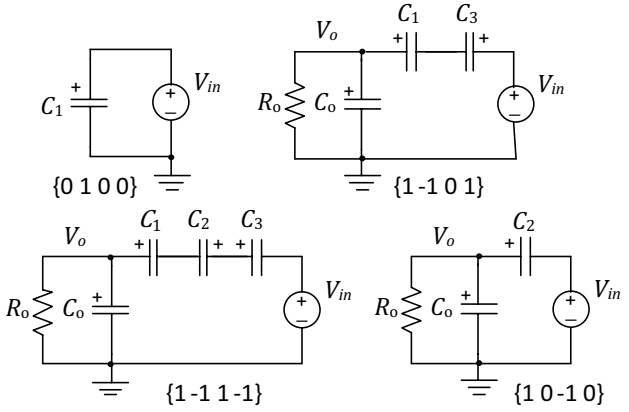


Fig. 5: The topologies of step-up Fibonacci SCC with $1/M_3$=5/3.

The steady-state KVL equations for the topologies of Fig. 5 are:

$$\begin{cases} 0\cdot V_o + 1\cdot V_1 + 0\cdot V_2 + 0\cdot V_3 = V_{in} \\ 1\cdot V_o - 1\cdot V_1 + 0\cdot V_2 + 1\cdot V_3 = V_{in} \\ 1\cdot V_o - 1\cdot V_1 + 1\cdot V_2 - 1\cdot V_3 = V_{in} \\ 1\cdot V_o + 0\cdot V_1 - 1\cdot V_2 + 0\cdot V_3 = V_{in} \end{cases} \quad (5)$$

The solution of (5) is: V_o=(5/3)V_{in}; V_1=V_{in}; V_2=(2/3)V_{in}; V_3=(1/3)V_{in}. It is evident that the step-up Fibonacci target voltage V_o=(5/3)V_{in} is reciprocal to its step-down counterpart V_o=(3/5)V_{in} as in the case of binary SCC [2],[5]. Note that for n flying capacitors, the highest conversion ratio is equal to (n+2)-th Fibonacci number F_{n+2}. Although various Fibonacci step-up SCC with the conversion ratio F_{n+2} have been proposed earlier [16-18], there is no published report on SCC with fractional Fibonacci conversion ratio greater than one.

Taking all the aforesaid into consideration, we have six new Fibonacci conversion ratios: {1/5, 1/3, 2/5, 3/5, 2/3, 4/5} in addition to the seven {1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8} of the binary step-down SCC for the same resolution n = 1...3, which should improve the efficiency as depicted in Fig. 2.

4. Derivation of Equivalent Resistor

As was shown in [1-3] the total equivalent resistor in the class of SCC where the flying capacitors are always connected in series is given as:

$$R_{eq} = \frac{1}{2f_s}\sum_{i=1}^{m}\frac{k_i^2}{C_i}\coth\left(\frac{\beta_i}{2}\right) \quad (6)$$

where i is the topology number, k_i=I_i/I_o is the ratio of the average topology current I_i to the average output current I_o; and β_i=t_i/τ_i is the ratio of the time t_i allotted to topology i to its time constant τ_i=R_iC_i. To find the coefficients k_i we consider the steady state operation of SCC. In this case the charge received by each flying capacitor must be equal to the delivered charge. If all the SCC topologies are configured for equal time intervals t_i=t then the contribution of each I_i to I_o can be found from the next system of linear equations:

$$\sum_{i=1}^{m} A_{i,j} I_i = 0 \quad \text{and} \quad \sum_{i=1}^{m} A_{i,m} I_i = I_o \quad (7)$$

where m is the total number of SCC topologies; and $A_{i,j}$ is the SFN coefficients in topology i. As follows from (7) each equation for a fixed j can be obtained as a product of transposed j-th column $A_{i,j}$ (i=1...m) and column of unknown currents I_i. In the considered case of M_3=3/5 the system (7) is:

$$\begin{cases} I_1 - I_2 - I_3 + 0 = 0 \\ 0 + 0 + I_3 - I_4 = 0 \\ 0 + I_2 - I_3 + 0 = 0 \\ I_1 + I_2 + I_3 + I_4 = I_o \end{cases} \quad (8)$$

The solution of (8) is I_1=(2/5)I_o; I_2=I_3=I_4=(1/5)I_o. For each SCC topology we can find a total capacitor C_i and a total resistor R_i, which are substituted into β_i=t/R_iC_i.

Table VI: The analytical expressions of R_{eq}

M_n	Equivalent resistor expression	$\lim_{\beta\to 0} R_{eq}$
1/5, 4/5	$R_{eq}=\frac{T_s}{25C}\left[2\coth\left(\frac{\beta}{2}\right)+3\coth(\beta)\right]$	$\frac{28}{25}R$
1/3, 2/3	$R_{eq}=\frac{T_s}{9C}\left[\coth\left(\frac{\beta}{2}\right)+\coth(\beta)\right]$	R
2/5, 3/5	$R_{eq}=\frac{T_s}{50C}\left[5\coth\left(\frac{\beta}{2}\right)+2\coth(\beta)+3\coth\left(\frac{3\beta}{2}\right)\right]$	$\frac{28}{25}R$

Let us assume for simplicity that all the flying capacitors have an identical capacitance C. Since in each SCC topology of Fig. 4 the flying capacitors are connected in series, the ratio C_i/C is reciprocal to number of non-zero coefficients A_j (j>0) in Table IV. The coefficients required in R_{eq} derivation for all the M_n, n=1...3 are summarized in Table V.

It can be shown that number of switches used in the experimental setup to configure any SCC topology of Fig. 4 is constant and equal to four. Assuming an identical on-resistance r of all the switches and neglecting other parasitic resistances (e.g. ESR) we define the total on-resistance as R=4r and the common time ratio β=t/RC, so that β_i=$(C/C_i)\cdot\beta$. Substituting it and the coefficients of Table V into (6) we get the analytical expressions of R_{eq} presented in Table VI.

The asymptotic limit of R_{eq} for $\beta\to 0$ was found using the definition T_s=$(n+1)\cdot t$. This limit is called no-charge (NC) operation mode [3], [4] (also known as FSL) and practically reached if the SCC operates with very high switching frequency, so that $t_i \ll R_iC_i$. The momentary topology current in this case is almost constant and therefore its RMS is minimal. Since the same current with minimal RMS flows through the switch resistances, the efficiency of SCC operating in the NC mode is maximal [3], [4]. An important issue on this derivation is that the same R_{eq} was obtained for a pair of complementary conversion ratios M_n and $1-M_n$.

5. Experimental Results

The experimental setup (Fig. 6) followed the same design as in [2], [5] was built around the CMOS bidirectional switches with an on-resistance r=1.2Ω, while C_1=C_2=C_3=4.7μF, C_o=470μF, and V_{in}=8V. The time slot allotted for each topology was 5μs. The output voltage was measured for R_o=300Ω and R_o=100Ω and shown in Fig. 7(a) by solid and dashed line respectively. The SCC efficiency is presented in Fig. 7(b), for R_o=300Ω (diamonds) and R_o=100Ω (squares).

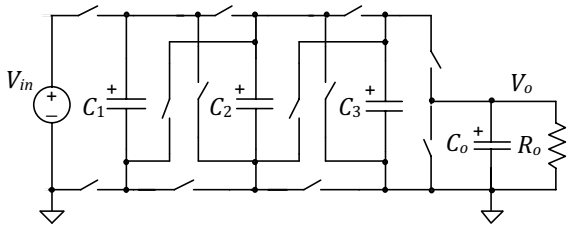
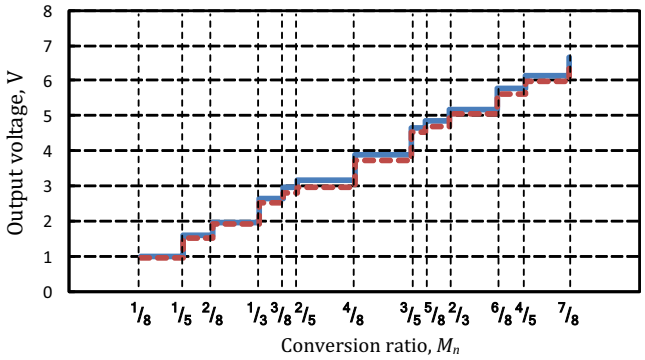
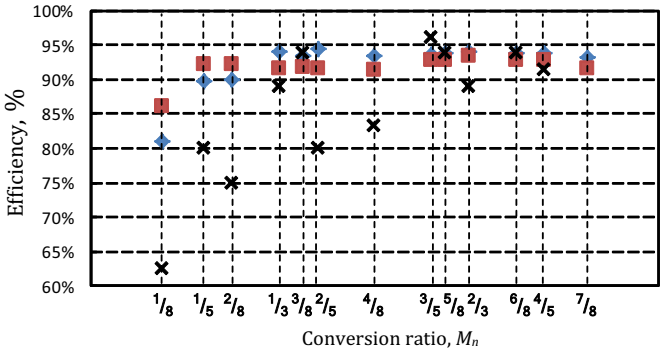


Fig. 6: The switch network used for the Fibonacci and binary SCC.



(a)



(b)

Fig. 7: The output voltage (a) and efficiency (b) of the experimental SCC. Diamonds: R_o=300Ω. Squares: R_o=100Ω. The curve of the higher output voltage in (a) is for R_o=300Ω, while the one of the lower output voltage is for R_o=100Ω. The points marked by "X" in (b) are estimates of minimum efficiency of a regulated version of proposed SCC in between target voltages.

As evident from Fig 7(b), the measured values of efficiency are low for low conversion ratios. This fact could be explained by that the real SCC has some constant losses, which have a larger effect at low conversion ratios. Additional evidence for the constant losses is that for the very conversion ratios the efficiency is lower for light load. The equivalent circuit in Fig. 1 takes into account the conduction losses only, so that measured values of R_{eq}, which include additional losses, should deviate from the theoretical values.

Table V: The coefficients required in R_{eq} derivation

i	M_3=1/5		M_2=1/3		M_3=2/5		M_1=1/2		M_3=3/5		M_2=2/3		M_3=4/5	
	I_i/I_o	C_i/C	I_i/I_o	C_i/C	I_i/I_o	C_i/C	I_i/I_o	C_i/C	I_i/I_o	C_i/C	I_i/I_o	C_i/C	I_i/I_o	C_i/C
1	2/5	1	1/3	1	1/5	1	1/2	1	2/5	1	1/3	1	1/5	1/2
2	1/5	1/2	1/3	1/2	1/5	1/3	1/2	1	1/5	1/2	1/3	1/2	1/5	1/2
3	1/5	1/2	1/3	1	1/5	1/2			1/5	1/3	1/3	1	1/5	1/2
4	1/5	1/2			2/5	1			1/5	1			2/5	1

Fig. 8 compares the measured values of R_{eq} with the calculated ones (Table VI). The dashed line in Fig. 8 corresponds to the case of no-additional losses.

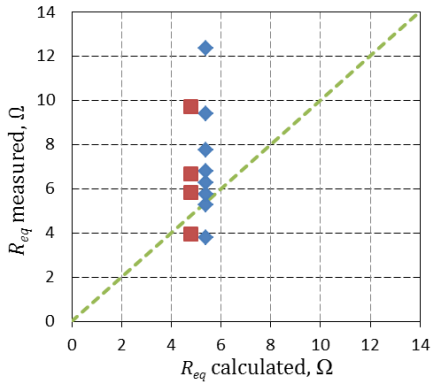


Fig. 8: Measured values of R_{eq} compared to the calculated ones. Diamonds: R_o=300Ω. Squares: R_o=100Ω.

6. Discussion and Conclusions

A new SFN representation was derived from the Fibonacci number system. Based on the SFN representation, a simple algebraic approach to synthesis Fibonacci SCC is developed. This new class of SCC can be considered as computational hardware that solves a system of linear equations defined by the SFN codes. The main feature of the proposed SCC is the compatibility with the binary SCC that allows one to approximately double the number of the target voltages. This would reduce losses in regulated SCC where the output is maintained at a constant voltage under load and input voltage variations. The multi-target feature would also be beneficial in cases when the output voltage of the SCC need to be adjusted to different levels. The proposed approach produces 13 target voltages for the gain range of 0-1. The efficiency at the target voltage will be maximal, limited by the equivalent resistance of the circuit and the parasitic losses. The experimental SCC unit that applied 1.2 Ohm switches reached, for most of the target ratios, above 90% efficiency. Gains in between the target points can be obtained by duty cycle control or frequency control [3, 4]. The gain control in these cases is obtained at the expense of increased losses [3] and consequently a lower efficiency. However, considering the close proximity of the target voltages, the expected efficiency reduction is rather small. The worst case is the gain range between 1/8 and 1/5 (Fig. 7). Applying the relationship $\eta=V_o/V_{TRG}$, the minimum efficiency (just before reaching the 1/8 gain) is 62.5%. For the same gain range, the minimum efficiency of the binary SCC [2], [5] would be 50%. Hence, considerable improvement is obtained even at the very low gains. For higher gains the expected minimum efficiency is considerably higher as is evident from Fig. 7b in which the estimated minimum efficiency in between the target points are marked by "X". It can thus be concluded that the proposed expansion of the multi-phase SCC in which the SFN codes are added to the Extended Binary Codes (EXB), improves the performance of the SCC. It is rather remarkable that this improvement is obtained at no cost since there is no need to add switched and/or capacitors to the circuit.

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