Algebraic Synthesis of Fibonacci Switched Capacitor Converters

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***Abstract* — A simple algebraic approach to synthesis Fibonacci Switched Capacitor Converters (SCC) was developed. The proposed approach reduces the power losses by increasing the number of target voltages. The synthesized Fibonacci SCC is compatible with the binary SCC and uses the same switch network. This feature is unique, since it provides the option to switch between the binary and Fibonacci target voltages, increasing thereby the resolution of attainable conversion ratios. The theoretical results were verified by experiments.**

***Index terms* — Charge pump, Fibonacci numbers, redundant number system, signed-digit representation, switched capacitor.**

I. Introduction

Among the many challenges of power management design of modern VLSI circuits, is the need to supply, from a single input voltage, different voltages to different parts of the chip. One of the techniques that meets the above requirement is the Switched Capacitor Converters (hereinafter SCC for both singular and plural), which are often referred to as charge pumps. SCC are also used as standalone power converters for low-power application.

It is well known that the SCC exhibits high efficiency only when its output voltage V_o is very close to the target voltage $V_{TRG}=M\cdot V_{in}$, where M is the no-load conversion ratio. The SCC efficiency can be approximated by $\eta=V_o/V_{TRG}$ and decreases when the SCC is loaded. This efficiency drop is due to the inherent power losses, which can be modeled by an equivalent circuit (Fig. 1) that includes the target voltage source V_{TRG} and a single equivalent resistor R_{eq}. This resistor represents the losses due to power dissipation in switch resistances and capacitors' ESR [1]. The simplified model of Fig. 1 does not take into account losses due to gate drives, leakage current and other parasitic effects which are not addressed in this work. Neglecting the parasitic effects, high efficiency is obtained if the equivalent resistor is small. In this case V_o will be very close to V_{TRG}.

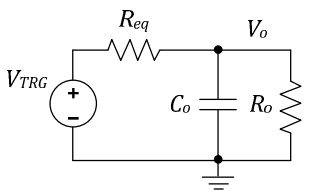

Fig. 1: The equivalent circuit of SCC

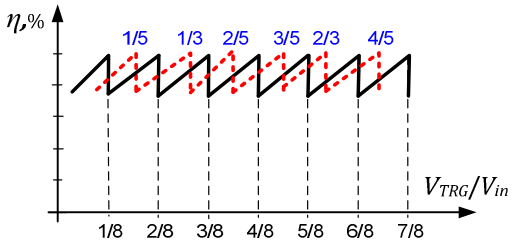

Fig. 2: The expected total efficiency.

In many applications there is a need to maintain a constant output voltage under input voltage variations or to provide different output voltages for different operational modes of a VLSI device. Such a voltage control can be accomplished by adjusting R_{eq} or M or both the parameters [2]. The highest efficiency will be obtained if R_{eq} is kept as small as possible and M is changed as required. This, however, is a difficult problem since M depends on the SCC topologies and can take only discrete values. The attempts to introduce multiple values of M have resulted hitherto in a large number of capacitors and switches that increase the power losses.

An effective way to realize many target voltages is the binary SCC [3], [4] that exhibits a binary resolution. That is, for n capacitors the number of target voltages will be 2^n-1 with a resolution of $1/2^n$. This binary behavior is depicted by solid line in Fig. 2 for $n = 3$, while the values on the x-axis represent the binary conversion ratios. The objective of this study was to introduce additional target voltages to the binary SCC without adding capacitors or switches. The dashed line in Fig. 2 depicts the additional efficiency peaks, which are obtained by the insertion of the proposed Fibonacci target voltages between their binary counterparts.

II. Signed Fibonacci Representation

The proposed approach to synthesis a Fibonacci SCC is based on the novel number system described in this section. For $i>2$ the Fibonacci numbers are defined as $F_i = F_{i-1} + F_{i-2}$, where the initial values are $F_1=F_2=1$. For example, if $i \le 5$ then F_i = 1, 1, 2, 3, 5. Due to Zeckendorf's theorem [5]-[9] any integer number N in the range $(1, F_{n+2})$ can be represented uniquely as a sum of distinct Fibonacci numbers. The main difference between the Zeckendorf representation and its binary counterpart is that the Z-code does not comprise two adjacent "1"s as shown in Table I.

Table I. The Z-codes for $N \le 5$

N	A_0	A_1	A_2	A_3
	5	3	2	1
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	0	1	0	1
5	1	0	0	0

Based on the Zeckendorf representation we define Signed Fibonacci Representation (SFN) for fractions $M_n=N/F_{n+2}$ in the range (0, 1) as follows:

$$M_n = A_0 + \sum_{j=1}^{n} A_j \frac{F_{n-j+2}}{F_{n+2}} \tag{1}$$

where A_0 can take the values of 0 or 1; A_j takes any of the three values −1, 0, 1; and n sets the resolution. Unlike the Zeckendorf representation, a number of different SFN codes represent a single M_n value, for example:

$$\begin{aligned} {}^4/_5 &= 1 - 1\cdot({}^3/_5) + 1\cdot({}^2/_5) + 0\cdot({}^1/_5) \rightarrow \{1\ \text{-}1\ \ 1\ 0\} \\ {}^4/_5 &= 1 + 0\cdot({}^3/_5) - 1\cdot({}^2/_5) + 1\cdot({}^1/_5) \rightarrow \{1\ 0\ \text{-}1\ \ 1\} \\ {}^4/_5 &= 1 + 0\cdot({}^3/_5) + 0\cdot({}^2/_5) - 1\cdot({}^1/_5) \rightarrow \{1\ 0\ \ 0\ \text{-}1\} \end{aligned} \tag{2}$$

These different codes can be obtained by the spawning rule, which is based on the identity $2F_i = F_{i+1}+F_{i-2}$. This identity states in fact that addition of two "1"s in the Fibonacci code induces two carries. One goes one bit left, while the other goes two bits right.

A rule for spawning the SFN codes:

This procedure is iterative and starts with the Z-code of M_n. Skipping the zeros from the left add "1" to first $A_j = 1$. This will turn A_j to "0" and induce two carries. To keep the original M_n value add "−1" to the resulting $A_j = 0$ and generate thereby a new SFN code. The procedure is repeated for all $A_j = 1$ in the original code and for all $A_j = 1$ in each new SFN code.

Corollary 1: For a resolution n, the minimum number of SFB codes for a given M_n is $n + 1$. This is because each of the "1"s in the Z-code with resolution n produces a new SFB code and two carries. Further iterations cause the carries to propagate, so that each "0" in the Z-code is turned to "1", which is also operated on to spawn a new code. So, the minimum number of codes is the original code plus n that is, $n+1$.

Corollary 2: Each $A_j = 1$ in either the Z-code or spawned SFB code yields at least one $A_j = -1$ in the same position j of another SFB code. This is because the spawning procedure involves the substitution of a "1" by "−1".

The example in Fig. 3 shows how three different SFN codes for M_3=3/5 are spawned from the Z-code {0 1 0 0}. Note that operating A_3=1 in the code {1 -1 0 1} leads to the overflow, which can be disregarded since F_0/F_5=0. Another overflow takes place when "1" is added to A_2 =1 in the code {1 -1 1 -1}. Since F_1/F_5=1/5 we add "1" to A_3=−1 and obtain "0". The SFB codes for other M_n, n = 1...3 are summarized in Table II.

1	${}^3/_5$	${}^2/_5$	${}^1/_5$
0	1	0	0
	+1		
1	0	0	1
	−1		
1	−1	0	1

1	${}^3/_5$	${}^2/_5$	${}^1/_5$	${}^1/_5$	0
1	−1	0	1		
			+1		
1	−1	1	0	0	1
			−1		
1	−1	1	−1		

1	${}^3/_5$	${}^2/_5$	${}^1/_5$	${}^1/_5$
1	−1	1	−1	
		+1		
1	0	0	−1	1
		−1		
1	0	−1	0	

Fig.3: Spawning the SFN codes for M_3=3/5 from the Z-code {0 1 0 0}.

III. Translating the SFN Codes to SCC Topologies

The rules for translating the SFN codes into SCC topologies follow the rules given in [3], [4]. Consider a step-down SCC including a voltage source V_{in}, a set of n flying capacitors C_j and output capacitor C_o, which is paralleled with load R_o. For a given M_n the interconnections of V_{in}, C_j, and C_o are carried out according to the next rules:

1) If $A_0 = 1$ then V_{in} is connected in a polarity that charges the output.
2) If $A_0 = 0$ then V_{in} is not connected.
3) If $A_j = -1$ then C_j is connected in charging polarity (same as the output).
4) If $A_j = 0$ then C_j is not connected.
5) If $A_j = 1$ then C_j is connected in discharging polarity (opposite to the output).

The above rules are illustrated by translating the SFN codes of M_3=3/5 to topologies depicted in Fig. 3.

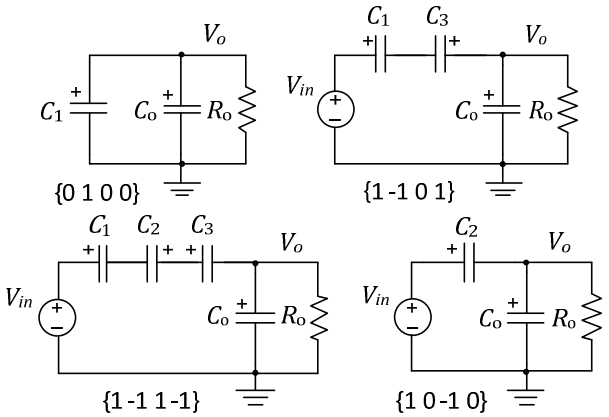

Fig. 3: The topologies of Fibonacci SCC with M_3=3/5.

Table II. The SFB codes for fractions M_n, n = 1...3

M_3=1/5				M_2=1/3			M_3=2/5				M_1=1/2		M_3=3/5				M_2=2/3			M_3=4/5			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_0	A_1	A_2	A_3	A_0	A_1	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_0	A_1	A_2	A_3
0	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	1
0	0	1	-1	0	1	-1	0	1	-1	1	1	-1	1	-1	0	1	1	-1	1	1	-1	1	0
0	1	-1	0	1	-1	0	0	1	0	-1			1	-1	1	-1	1	0	-1	1	0	-1	1
1	-1	-1	1				1	-1	0	0			1	0	-1	0				1	0	0	-1

Let us assume that under the steady-state condition all the capacitors in the topologies of Fig. 3 are charged to constant, but unknown voltages V_1, V_2, V_3, and V_o. To find these voltages we apply Kirchhoff's Voltage Law (KVL) to each topology which leads to a system of four linear equations:

$$\begin{cases} 0\cdot V_{in}+1\cdot V_1+0\cdot V_2+0\cdot V_3=V_o \\ 1\cdot V_{in}-1\cdot V_1+0\cdot V_2+1\cdot V_3=V_o \\ 1\cdot V_{in}-1\cdot V_1+1\cdot V_2-1\cdot V_3=V_o \\ 1\cdot V_{in}+0\cdot V_1-1\cdot V_2+0\cdot V_3=V_o \end{cases} \quad (3)$$

Solving (3) we obtain the voltages across the output and flying capacitors: $V_o=V_1=(^3/_5)V_{in}$; $V_2=(^2/_5)V_{in}$; $V_3=(^1/_5)V_{in}$. Considering the fact that (3) is solvable it should also be solvable if V_{in} and V_o are interchanged. This means switching the input and output and in fact, turning the step-down SCC to a step-up SCC.

$$\begin{cases} 0\cdot V_o+1\cdot V_1+0\cdot V_2+0\cdot V_3=V_{in} \\ 1\cdot V_o-1\cdot V_1+0\cdot V_2+1\cdot V_3=V_{in} \\ 1\cdot V_o-1\cdot V_1+1\cdot V_2-1\cdot V_3=V_{in} \\ 1\cdot V_o+0\cdot V_1-1\cdot V_2+0\cdot V_3=V_{in} \end{cases} \quad (4)$$

The solution of (4) is: $V_o=(^5/_3)V_{in}$; $V_1=V_{in}$; $V_2=(^2/_3)V_{in}$; $V_3=(^1/_3)V_{in}$. It is evident that the step-up Fibonacci target voltage $V_o=(^5/_3)V_{in}$ is reciprocal to its step-down counterpart as in the case of binary SCC. Note that for n flying capacitors, the highest conversion ratio is equal to $(n+2)$-th Fibonacci number F_{n+2}. Although various Fibonacci step-up SCC with the conversion ratio F_{n+2} have been proposed earlier [10]-[12], there is no published report on SCC with fractional Fibonacci conversion ratio greater than one.

Taking all the aforesaid into consideration, we have six new Fibonacci conversion ratios: $\{^1/_5,\ ^1/_3,\ ^2/_5,\ ^3/_5,\ ^2/_3,\ ^4/_5\}$ in addition to the seven $\{^1/_8,\ ^1/_4,\ ^3/_8,\ ^1/_2,\ ^5/_8,\ ^3/_4,\ ^7/_8\}$ of the binary SCC for the same resolution n = 1...3, which should improve the efficiency as depicted in Fig. 2.

IV. Experimental Results

The experimental setup (Fig. 4) followed the same design as in [3], [4] and was built around the bidirectional switches with an on-resistance of 1.2Ω, while $C_1=C_2=C_3=4.7\mu F$, $C_o=470\mu F$, and V_{in}=5V. The time slot allotted for each topology was $5\mu s$. The output voltage was measured for R_o=300Ω and R_o=100Ω and shown in Fig. 5(a) by solid and dashed line respectively. The SCC efficiency is presented in Fig. 5(b), for R_o=300Ω (diamonds) and R_o=100Ω (squares).

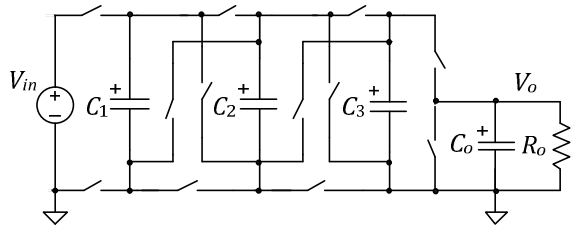

Fig. 4: The switch network used for the Fibonacci and binary SCC.

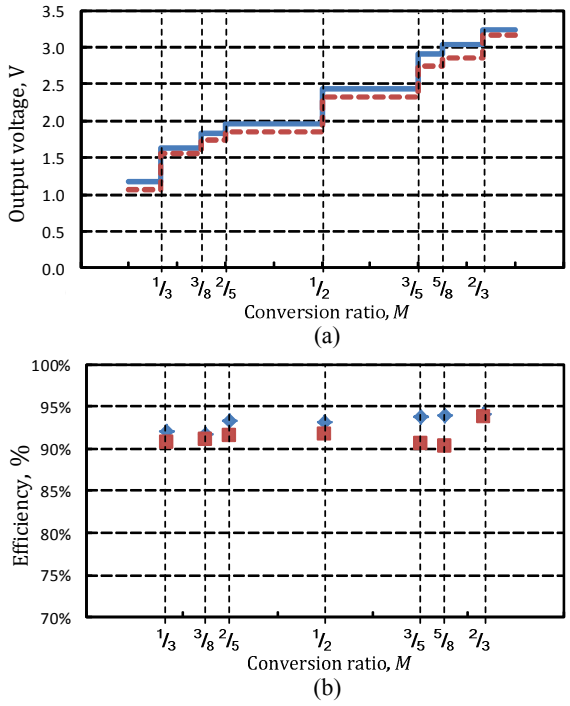

Fig. 5: The output voltage (a) and efficiency (b) of the proposed SCC

V. Conclusions and Discussion

A new SFN representation was derived from the Fibonacci number system. Based on the SFN representation, a simple algebraic approach to synthesis Fibonacci SCC is developed. This new class of SCC can be considered as computational hardware that solves a system of linear equations defined by the SFN codes. The main feature of the proposed SCC is the compatibility with the binary SCC that allows one to approximately double the number of the target voltages. This would reduce losses in regulated SCC where the output is maintained at a constant voltage under load and input voltage variations. The multi-target feature would also be beneficial in cases when the output voltage of the SCC need to be adjusted to different levels.

Acknowledgement

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