Analysis and Implementation of Output Voltage Regulation in Multi-Phase Switched Capacitor Converters

Sam Ben-Yaakov, *Fellow, IEEE* and Alexander Kushnerov, *Student Member, IEEE*

Power Electronics Laboratory
Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev
P.O. Box 653, Beer-Sheva, 84105 Israel
E-mails: sby@ee.bgu.ac.il; kushnero@ee.bgu.ac.il
Website: www.ee.bgu.ac.il\~pel

***Abstract*—A new regulation technique based on duty cycle control of the average currents in the multi-phase switched capacitor converters (SCC) is proposed, analyzed, and verified experimentally for the No effective Charging (NC) case, also known as the fast switching limit (FSL). The regulation is accomplished by adjusting the value of the SCC equivalent resistor. To this end the time slots allotted to each of the SCC topologies are adjusted, while the total switching period is kept constant. The time slots are represented by master and slave duty cycles. By this, the SCC output voltage is expressed analytically as a function of the master duty cycle. In a similar way, analytical expressions for the voltages across the flying capacitors and for the average currents in each of the topologies can be obtained. Excellent agreement was found between the theoretical and experimental results.**

I. Introduction

Switched Capacitor Converters (denoted hereinafter as SCC for singular and plural) have inherent losses that make their use prohibitive in many applications. Still, SCC are preferred in some cases due to their IC compatibility, relatively small size and the lack of magnetic elements. It is well known that the SCC exhibits high efficiency only when its output voltage V_o is close to the target voltage $V_{TRG}=M\cdot V_{in}$, where M is the no-load conversion ratio. However, the efficiency, which can be expressed as $\eta = V_o/V_{TRG}$ decreases when the SCC is loaded since the output voltage is less than the target voltage. This efficiency drop is due to the SCC inherent power loss, which can be modeled by an equivalent circuit that includes the target voltage source and a single equivalent resistor R_{eq} as depicted in Fig. 1.

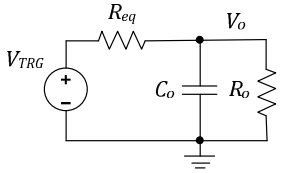


Fig. 1: The equivalent circuit of SCC

The average behavior of SCC was analyzed in numerous earlier studies [1-7], where various techniques for output voltage regulation are described. However, these studies considered regulation in the two-phase SCC only, while the objective of this study was to develop a simple regulation technique for the multi-phase SCC.

II. The Multi-Phase SCC and Regulation Method

The proposed regulation technique is demonstrated by considering the binary multi-phase SCC [9, 10] with a conversion ratio M = 3/8. In normal operation, the switches commutate the capacitors C_j according to the topologies of Fig. 2 with equal time slots t_i for each topology i. All the parasitic resistances in the actual circuit, namely $R_{ds(on)}$ of the switches and ESR of the capacitors are modeled by the resistors R_1...R_4.

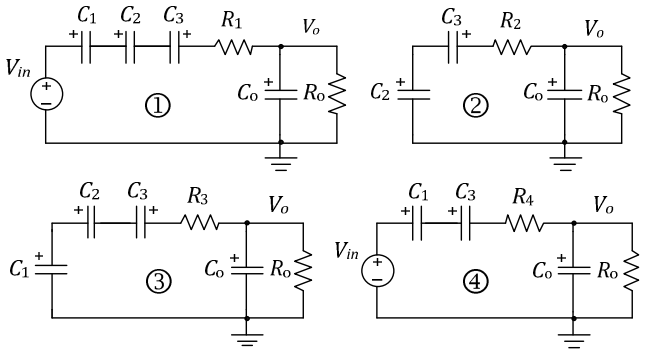


Fig. 2: Topologies of the SCC with the conversion ratio M = 3/8.

Once topology i is configured, an equivalent capacitor $C_i=1/\sum(1/C_j)$ starts to charge (or discharge), such that the current in this topology $i_i(t) = I_{0i}e^{-t/\tau_i}$, where I_{0i} is the initial current, and $\tau_i = R_iC_i$. Depending on the ratio t_i/τ_i the current $i_i(t)$ can take one of three possible waveforms presented in Fig. 3. The charging of C_i is practically completed if $t_i \geq 5\tau_i$ and this case is denoted by CC. In the case when $t_i \approx \tau_i$ the charging is partial (PC) and if $t_i \ll \tau_i$ there is no effective charging (NC), so that during t_i the current through C_i is almost constant as well as the voltage across it.

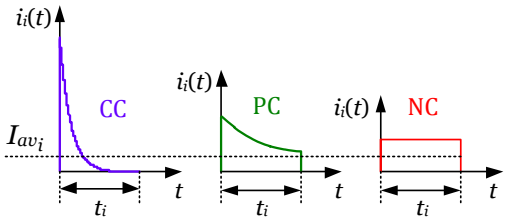


Fig. 3: Possible forms of the current through the equivalent capacitor C_i in topology i.

The current I_{avi} depicted in Fig. 3 is averaged over the total switching period. Considering it as a common reference, one can conclude that the RMS of $i_i(t)$ will be minimal in the NC mode and consequently, the efficiency of SCC operating in this mode is maximal [8, 11]. Furthermore, in this case the SCC output voltage is the most sensitive to the changes of duty cycle as compared to the CC and PC cases. Based on the above, the NC mode was adopted in this study. Similarly to the regulation methods presented in [1-7] for the two-phase SCC, the proposed method is based on duty cycle control. To achieve regulation in the multi-phase SCC the time slots t_i could be varied, whereas the total switching period T_s need to be kept constant. By this, the value of SCC equivalent resistor is adjusted to regulate the output voltage.

III. Model Derivation

The topologies of Fig. 2 are synthesized by the extended binary (EXB) representation [9, 10], which in the case of M=3/8 yields a set of the coefficients $a_{i,j}$ given in Table I. These coefficients represent the connection polarity of the flying capacitors C_j (-1 implies that C_j is charging, 1 implies that it is discharging, and 0 implies that C_j is not connected). The values of $a_{i,0}$ are restricted to be either 1 or 0 depending whether V_{in} is connected or not, while $a_{i,4}$ is equal to -1 for all i, since C_o is always charging.

TABLE I:
Set of the coefficients $a_{i,j}$ for M=3/8

j / i	$a_{i,0}$	$a_{i,1}$	$a_{i,2}$	$a_{i,3}$	$a_{i,4}$
$a_{1,j}$	1	-1	-1	1	-1
$a_{2,j}$	0	0	1	1	-1
$a_{3,j}$	0	1	-1	1	-1
$a_{4,j}$	1	-1	0	-1	-1

Since the topologies of Fig. 2 are denoted by the index i, and the flying capacitors by the index j, we can use the coefficients $a_{i,j}$ of Table I to compose the KVL equations for each topology under steady state condition:

$$\sum_{j=1}^{3} a_{i,j}V_j - k_i I_i R_i + a_{i,4}V_o = -a_{i,0}V_{in} \tag{1}$$

where V_j are the voltages across C_j, and I_i are the currents in each of the topologies averaged over the total switching period T_s. The factors $k_i = T_s/t_i$ scales up I_i to the value of the actual current flowing during t_i. Under steady state condition, the sum of the I_i through each capacitor C_j ($j \le 3$) should be equal to zero, while the sum of the I_i through the output capacitor C_o (j=4) is equal to the output current $I_o = V_o/R_o$.

$$\sum_{i=1}^{4} a_{i,j}I_i = 0 \quad \text{and} \quad \sum_{i=1}^{4} a_{i,4}I_i = \frac{1}{R_o}V_o \tag{2}$$

Equation (2) can be obtained as the vector product of the columns j=1...4 of Table I and the vector of currents I_i. Summarizing (1) and (2) in a matrix form we get:

$$\begin{pmatrix} \begin{bmatrix} -1 & -1 & 1 & -1 \\ 0 & 1 & 1 & -1 \\ 1 & -1 & 1 & -1 \\ -1 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} -k_1R_1 & 0 & 0 & 0 \\ 0 & -k_2R_2 & 0 & 0 \\ 0 & 0 & -k_3R_3 & 0 \\ 0 & 0 & 0 & -k_4R_4 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_o} \end{bmatrix} \begin{bmatrix} -1 & 0 & 1 & -1 \\ -1 & 1 & -1 & 0 \\ 1 & 1 & 1 & -1 \\ -1 & -1 & -1 & -1 \end{bmatrix} \end{pmatrix} \times \begin{pmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_o \end{bmatrix} \\ \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \end{pmatrix} = \begin{pmatrix} \begin{bmatrix} -V_{in} \\ 0 \\ 0 \\ -V_{in} \end{bmatrix} \\ \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \end{pmatrix} \tag{3}$$

Designate the number of unknowns in (3) by $2m$, so that all the sub-matrices will be of size $m \times m$. Thus, the system of equation (3) can be extended to the general case and written concisely as:

$$\begin{pmatrix} [\boldsymbol{A}]\,[\boldsymbol{kR}] \\ [\boldsymbol{G}_o][\boldsymbol{A}^T] \end{pmatrix} \times \begin{pmatrix} [\boldsymbol{V}] \\ [\boldsymbol{I}] \end{pmatrix} = \begin{pmatrix} [\boldsymbol{V}_{in}] \\ [\boldsymbol{0}] \end{pmatrix} \tag{4}$$

where $\boldsymbol{A}$ is the incidence matrix (Table 1, without the first column); $\boldsymbol{kR}$ is the diagonal matrix comprising $-k_iR_i$; $\boldsymbol{G}_o$ is the matrix where all the coefficients, except for $g_{m,m} = 1/R_o$ are zeros; $\boldsymbol{V}$ and $\boldsymbol{I}$ are the column-vectors of the unknown voltages and currents respectively; $\boldsymbol{V}_{in}$ is a column-vector consisting of $-V_{in}$ and zeros.

Solving (3) for the case of $R_i = R$, we find the conversion ratio V_o/V_{in} as a function of the coefficients k_i and the normalized resistor $p = R_o/R$:

$$\frac{V_o}{V_{in}} = \frac{3}{8 + \dfrac{k_1 + 4k_2 + 9k_3 + 16k_4}{8p}} \tag{5}$$

Since $k_i = T_s/t_i = 1/D_i$, the output to input voltage ratio can be expressed as a function of the partial duty cycles D_i:

$$\frac{V_o}{V_{in}} = \frac{3}{8 + \dfrac{1\dfrac{1}{D_1} + 4\dfrac{1}{D_2} + 9\dfrac{1}{D_3} + 16\dfrac{1}{D_4}}{8p}}; \quad \sum_{i=1}^{4} D_i = 1 \tag{6}$$

Expression (6) clearly shows that the output voltage can be regulated by controlling the partial duty cycles. This is on par with the results of [8] that evaluated the effect of the duty cycle on the SCC conduction losses. As was revealed in [8], the effect of duty cycle is the largest in the NC mode that is the major reason for selecting this mode in the present study. One of the simplest regulation strategies is to define one topology as the pivoting and select its duty cycle as the master duty cycle D. The control algorithm can further be simplified by making all the "slave" duty cycles equal. Namely, for a SCC with m topologies:

$$D_i\big|_{i \neq master} = \frac{1-D}{m-1} \tag{7}$$

It would be desirable that the selected master duty cycle will produce smooth regulation over the required range.

In the case of the binary SCC the required range is the incremental resolution of the converter. That is, the deviation between on target voltage to the lower next. For the M=3/8 case, deviation of interest will be the range from M=3/8 to M=2/8. To test this sensitivity issue, one can express the output to input voltage ratio for the four master duty cycle possibilities (8) and plot the responses (Fig. 4).

$$\left.\frac{V_o}{V_{in}}\right|_{(D=D_1)} = 3(1-D)\Big/\left[8(1-D)+\left(\frac{1+86D}{8Dp}\right)\right]$$
$$\left.\frac{V_o}{V_{in}}\right|_{(D=D_2)} = 3(1-D)\Big/\left[8(1-D)+\left(\frac{2+37D}{4Dp}\right)\right] \quad (8)$$
$$\left.\frac{V_o}{V_{in}}\right|_{(D=D_3)} = 3(1-D)\Big/\left[8(1-D)+\left(\frac{9+54D}{8Dp}\right)\right]$$
$$\left.\frac{V_o}{V_{in}}\right|_{(D=D_4)} = 3(1-D)\Big/\left[8(1-D)+\left(\frac{8+13D}{4Dp}\right)\right]$$

The graphs of Fig. 4 suggest that a good choice for the master duty cycle would be $D=D_1$, since it yields a smooth and moderate regulation curve even below the level of M=2/8 (1/4) conversion ratio.

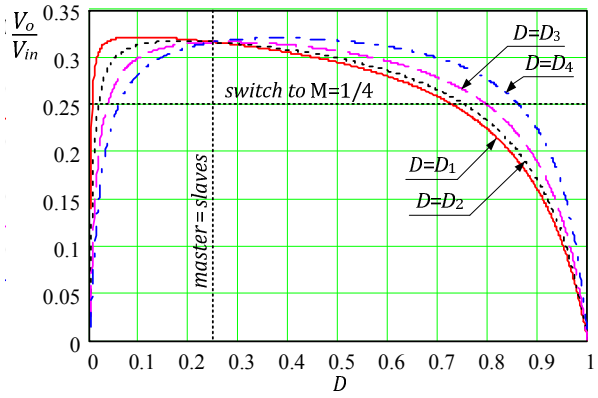


Fig. 4: The transfer functions V_o/V_{in} for different master duty cycles $D=D_i$ selections and $p=10$.

For any selected master duty cycle, the voltages across the flying capacitors will also be affected by the value of this master control variable. The expressions for the capacitors' voltages normalized to the input voltage are given by (9), where $D=D_1$. It is evident from (8) and (9) that for high value of p (very low losses) the output voltage will converge asymptotically to $V_{TRG}=(3/8)V_{in}$, while the voltages across the flying capacitors become binary weighted [9, 10].

$$\frac{V_1}{V_{in}} = \left[4(1-D)+\left(\frac{2+55D}{8Dp}\right)\right]\Big/\left[8(1-D)+\left(\frac{1+86D}{8Dp}\right)\right]$$
$$\frac{V_2}{V_{in}} = \left[2(1-D)+\left(\frac{1+23D}{8Dp}\right)\right]\Big/\left[8(1-D)+\left(\frac{1+86D}{8Dp}\right)\right] \quad (9)$$
$$\frac{V_3}{V_{in}} = \left[(1-D)-\left(\frac{1+5D}{8Dp}\right)\right]\Big/\left[8(1-D)+\left(\frac{1+86D}{8Dp}\right)\right]$$

IV. Experimental Results

The experimental setup used to realize the topologies of Fig. 2 is depicted schematically in Fig. 5. It was built around the CMOS switches MAX4678 with a $R_{ds(on)}=1.2\Omega$, which were controlled by a microcontroller dsPIC33FJ12GP202, while $C_1=C_2=C_3=4.7\mu F$, $C_o=470\mu F$, $R_o=4.7k\Omega$, $T_s=180\mu s$, and $V_{in}=8V$. To provide the NC operation at the limited switching frequency that could be achieved by the present setup, an external resistor $R=470\Omega$ was connected in series with C_3 (Fig. 5).

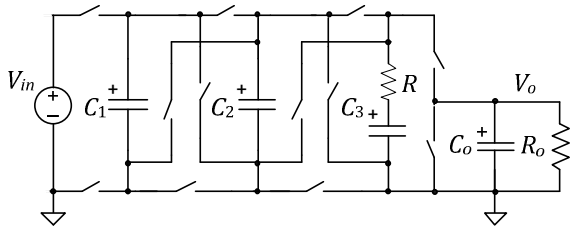
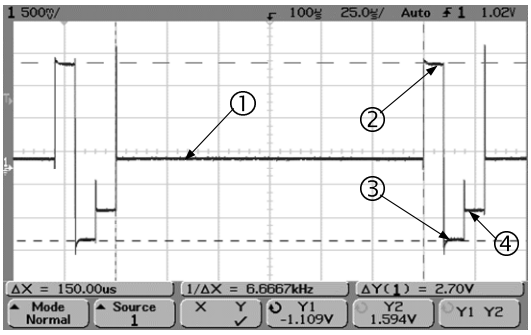
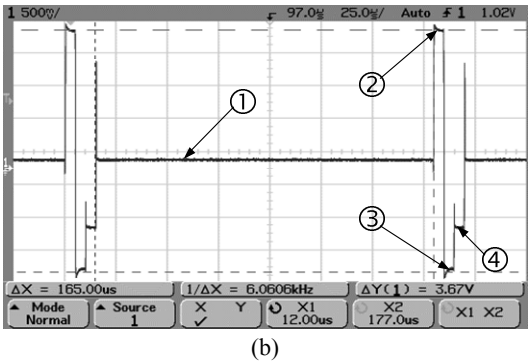


Fig. 5: The structure of the experimental setup circuit.

All experiments were carried out for $D=D_1$ and $p=10$. The actual currents k_iI_i measured as the voltage drop across R are depicted in Fig. 6, while the theoretically predicted by (8) and the experimental regulation characteristics are presented in Fig. 7 by solid and dashed lines respectively. The behavior of the voltages across the flying capacitors is depicted in Fig. 8, where the solid lines represent the voltages calculated by (9), and the dashed lines are those verified experimentally.



(a)



(b)

Fig. 6: The instantaneous currents in all the topologies of Fig. 1 (M=3/8) for $D=D_1=0.833$ (a) and $D=D_1=0.916$ (b). The circled numbers correspond to the topologies of Fig. 2.

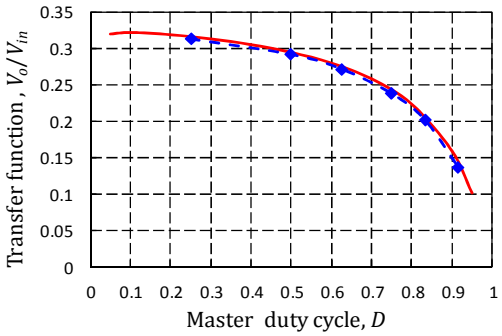


Fig. 7: The SCC regulation characteristics for M=3/8 and D=D_1. Solid line: model prediction; Dashed line: experimental results.

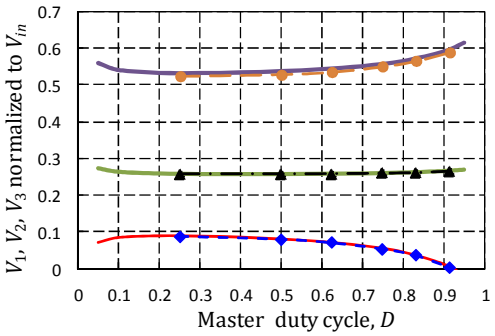


Fig. 8: The voltages across C_1, C_2, C_3 normalized to V_{in} for M=3/8 and D=D_1. Solid line: model prediction; Dashed line: experimental results.

V. Discussion and Conclusions

A new analytical model was developed and applied to examine the viability of output voltage regulation by duty cycle control of multi-phase SCC operating in the NC mode. The proposed control was verified experimentally and found to achieve almost 50% variation of the output voltage. This range should suffice to provide continuous output voltage control in multi-target SCC in which the coarse control is accomplished by moving from one target voltage to another.

The proposed regulation method does not require any additional hardware and can be easily implemented by analog or digital controllers. Like in all SCC systems, regulation is accomplished by increasing losses, which are emulated by the SCC equivalent resistor [8, 11]. In the present case, duty cycle control is used to increase the losses. This is achieved by increasing the RMS currents of the slave topologies. For example, comparing Fig. 6a with Fig. 6b, one can clearly notice that the RMS current of, say, topology 2 is higher in Fig. 6b, in which the master duty cycle is higher (D=0.916) as compared to the case of Fig. 6a (D=0.833). However, the regulation characteristics (8) are not only a function of the master duty cycle D but also depend on the ratio of the load and the topologies' resistances (assumed to be equal for the sake of simplicity) p=R_o/R. As the load resistance R_o increases, the regulation depth in the range 0<D<1 will decrease, reaching eventually the point at which it is insufficient (smaller than the multi-target SCC resolution). This situation is of course common in any converter, including those which are based on the switched inductor technology.

A number of control strategies can be used to resolve the problem of SCC regulation at very light loads. Clearly, any of these methods needs to increase the losses when the output current is low. One possible approach will be to reduce the switching frequency, pushing thereby the topologies into the PC mode and eventually into the CC mode, both of which have higher losses [11]. Another approach could be frequency hopping or dithering [9, 10], which have the disadvantage of introducing a low frequency ripple at the output.

The proposed control was verified experimentally and the results were found to match very well the model predictions. However, due to experimental constraints the switching frequency was limited to 5.5kHz. At this frequency, the effect of the parasitic inductances is very small. One should be aware though that parasitic inductance may introduce a significant change in the behavior of the SCC when operated at high switching frequency as discussed and analyzed in [8].

Acknowledgment

This research was supported by the Israel Science Foundation, ISF (grant No. 476/08).

References

[1] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor DC-DC converter," *IEEE Trans. Aerosp. Electron. Syst.*, Vol. 3, 1994, pp.92-100.

[2] M. Keskin, N. Keskin, and G. C. Temes, "An efficient and accurate DC analysis technique for switched capacitor circuits," Analog Integrated Circuits and Signal Processing, Vol. 30, №3, 2002, pp. 239-242.

[3] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched capacitor DC-DC converters," *IEEE Trans. Power Electronics,* Vol. 23, №2, 2008, pp.841-851.

[4] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Trans. Power Electronics*, Vol. 26, №1, 2011, pp.127-136.

[5] G. Zhu and A. Ioinovici, "Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation," IEEE Int. Symp. Circuits and Systems (ISCAS), Vol. 1, 1996, pp.553-556.

[6] G. Zhu and A. Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters," *Journal of Circuits, Systems, and Computers* (JCSC), Vol. 7, №2, 1997, pp.69-91.

[7] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," IEEE Power Electronics Specialists Conference (PESC) 2008, pp.4008-4015.

[8] S. Ben-Yaakov and M. Evzelman, "Generic and unified model of switched capacitor converters," IEEE Energy Conversion Congress and Expo. (ECCE) 2009, pp.3501-3508.

[9] S. Ben-Yaakov and A. Kushnerov, "Algebraic foundation of self-adjusting switched capacitor converters," IEEE Energy Conversion Congress and Expo. (ECCE) 2009, pp.1582-1589.

[10] A. Kushnerov, *High-efficiency self-adjusting switched capacitor DC-DC converter with binary resolution*, M.Sc. thesis, Ben-Gurion University of the Negev, 2009, 115p.

[11] S. Ben-Yaakov, "On the influence of switch resistances on switched capacitor converters losses," *IEEE Trans. Ind. Electronics,* 2011 (in print).