Optimization of a Multi-Target Voltages Switched Capacitor Converter

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***Abstract*—In this paper, an efficient voltage scalable switched capacitor converter (SCC) for 1.1V battery-powered system is presented. The SCC employs a binary resolution technique to step-down the input voltage to a range of voltages, while keeping the efficiency high. An optimization strategy for designing multi-topology SCC is presented to improve the effectiveness of the circuit and to preserve efficiency over large load voltages.**

I. INTRODUCTION

The growing quest for power saving techniques in digital systems has raised the need for an integrated DC-DC converter which is compatible with sub-threshold operation levels [1]. To minimize power dissipation in ultra low power systems, the DC-DC converter needs to supply variable sub-threshold load voltages [2]. The most efficient technique for step-down conversion is based on the Buck converter. However, the employment of an off-chip inductor for each voltage domain causes serious EMI noise and a large pin requirement, which makes such implementation impractical in many applications. Switched capacitor converters (SCC) have become more attractive for battery operated systems because they can minimize the number of off-chip components and have flexibility in sizing switches and capacitors [3], [4]. The challenge associated with the realization of an efficient low voltage and ultra low power SCC has led to several recent developments [5]-[7]. These studies have shown that the efficiency of multiple conversion ratios SCC can be maintained effective over wider input voltage range than that of a single topology converter. It is shown that a combination of two standard divide by two SCC cells can support two additional topologies, which provide 2/3 and 1/3 conversion ratios [8]. This circuit and its variants were systematically designed in numerous works, utilizing one or more of its possible conversion ratios. For example, an interleaved SCC structure partitioned into multiple circuits to reduce the input current and output voltage ripples has been explored in [8].

The most common loss mechanisms of an integrated SCC are:

1) Charge transfer conduction losses,
2) Switching losses,

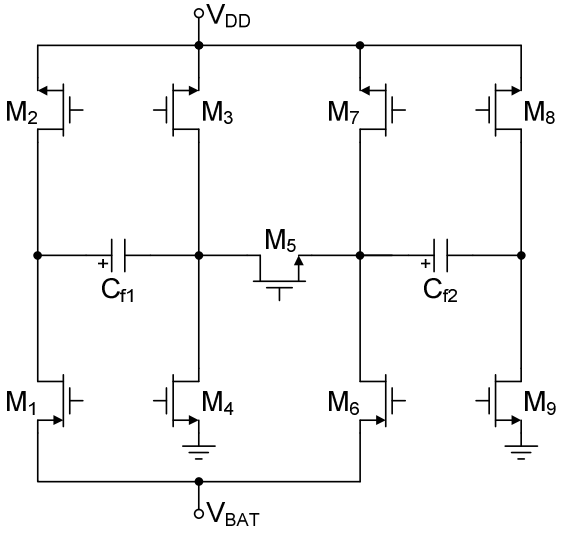

Fig. 1. Conventional 9 switch SCC with three conversion ratios G={1/3,1/2,2/3}.

3) Bottom-plate parasitic capacitors,
4) Output voltage ripple,
5) Switch parasitic losses,
6) Gate drive loss.

In light of these, it is clear that the main challenge in SCC design is the optimization [9] of the converter parameters, while meeting various constraints on efficiency, silicon area and output voltage V_{DD}. If, for instance, a traditional design approach is adopted, such as sizing the switches of the SCC to the same $R_{ds(on)}$ or, alternatively, adjusting it to allow operation in the complete charge transfer mode, one might end up with a non-optimal design.

Motivated by the above concerns, this work presents an optimization procedure of a 40nm 1.1V CMOS voltage scalable SCC, which is suitable for mobile sub-threshold applications supporting output levels of 0.18V-0.6V. It should be noted that the presented concept is general and not depends on particular implementation technology. The core of the proposed circuit is a classical SCC shown in Fig. 1. This circuit is composed of nine switches and two flying capacitors to support three conversion ratios (this topology denoted henceforth as conventional SCC). Typical candidates for this SCC are applications require ultra-low dissipation

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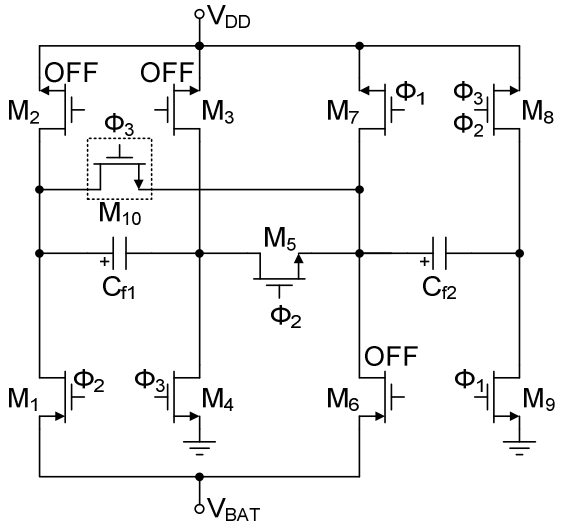


Fig. 2. Proposed 10 switch SCC with four conversion ratios G={1/4,1/3,1/2,2/3}. With gain setting of G=1/4, the switches M_2, M_3, M_6 are in off state, while the remaining switches are clocked by a 3 phase timing template $\{\Phi_1,\Phi_2,\Phi_3\}$.

with low to moderate circuit performance. To enhance the efficiency of this SCC in the vicinity of V_{DD}=0.2V a single extra power switch was introduced (Fig. 2) as compared to the topology of the conventional SCC (Fig. 1). Hence, a total of only 10 power switches are able to support four topologies with conversion ratios of 2/3, 1/2, 1/3 and 1/4. The proposed G=1/4 topology employs the technique of binary SCC [5].

Since the proposed SCC is supposed to work over four different topologies, it is hard to define a single optimized operating point that can constitute an optimization criterion for all topologies. As far as author's knowledge this subject has received limited attention over the years. Therefore, this paper outlines an optimization methodology of a multi-objective optimization approach.

II. Proposed Switched Capacitor Converter

It is well established that any SCC can be modeled with an equivalent no-load voltage source connected in a series with an equivalent resistor R_{eq} [10], [11]. Loss contributors in SCC power stage are collected into that equivalent resistor. The maximum theoretical efficiency of the SCC for a given conversion ratio G can be expressed by,

$$\eta_{max} = \frac{V_{DD}}{G \cdot V_{BAT}} = \frac{R_L}{R_L + R_{eq}} \quad (1)$$

where V_{DD} and V_{BAT} are the loaded output and input battery voltages, respectively and R_L is the load resistance. Equation (1) however, does not take into account the power losses that stem from leakages, the bottom plate capacitor, the gate drive and the control circuitry. A more accurate representation of (1) will be with all loss contributors as follows,

$$\eta = \frac{P_L}{P_L/\eta_{max} + P_{BP} + P_{Drive} + P_{Leak} + P_{Control}} \quad (2)$$

where P_L, P_{BP}, P_{Drive}, P_{Leak}, $P_{Control}$ are respectively the output power, the bottom-plate parasitic capacitor related losses, the gate drive loss, the power consumption due to leakage current and the power lost in the control circuitry.

In practice, employing the circuit of Fig. 1 to produce an ultra low V_{DD} voltage such as 0.2V from 1.1V battery is possible but the resulting efficiency will be very poor. For example, using the smallest possible ratio of G=1/3, it follows from (1) that for V_{DD}=0.2V, the obtainable efficiency is limited to 54%. It would appear that a conversion ratio of G=1/4 can be realized by cascading two divide by two SCC in order to increase the efficiency up to 73%. However, this requires an additional number of power switches that need to be considered.

A. The Approach

The configuration of the proposed power stage converter is depicted in Fig. 2. This circuit consists of a conventional SCC (Fig. 1) and an additional switch M_{10}. The SCC is designed to implement 4 different conversion ratios, excluding the trivial case G=1. The reader is referred to [6] and [8] for a detailed analysis of the ordinary conversion ratios and their corresponding topologies. When the circuit is supposed to operate with G=1/4, essentially it consists of three sub-circuits extended over three non-overlapping time sessions $\{\Phi_1,\Phi_2,\Phi_3\}$. Following the theory in [5], the sub-circuits of the SCC can be represented by an equivalent system of linear equations. Designating the voltages across C_{f1} and C_{f2} by V_{C1} and V_{C2}, the system of linear equations is composed as follows,

$$\begin{pmatrix} 1 & 0 & -1 \\ 1 & 1 & 1 \\ 1 & -1 & 1 \end{pmatrix} \cdot \begin{pmatrix} V_{DD} \\ V_{C1} \\ V_{C2} \end{pmatrix} = \begin{pmatrix} 0 \\ V_{BAT} \\ 0 \end{pmatrix} \quad (3)$$

The solution of (3) is: $V_{DD}=(1/4)V_{BAT}$, $V_{C1}=(1/2)V_{BAT}$ and $V_{C2}=(1/4)V_{BAT}$. These results determine that, in a steady state irrespective of the order in which the three sub-circuits repeat (Fig. 2), the voltages V_{DD}, V_{C1} and V_{C2} eventually converge to the above calculated values.

B. Architecture

The block diagram architecture of the considered SCC is shown in Fig. 3. Apart from the SCC circuit, all control blocks were implemented with the Verilog-A language (See Appendix). The SCC block contains the flying capacitors (C_{f1}, C_{f2}) and the power switches, as shown in Fig. 2. Eight clock waveforms are generated inside the non-overlapping

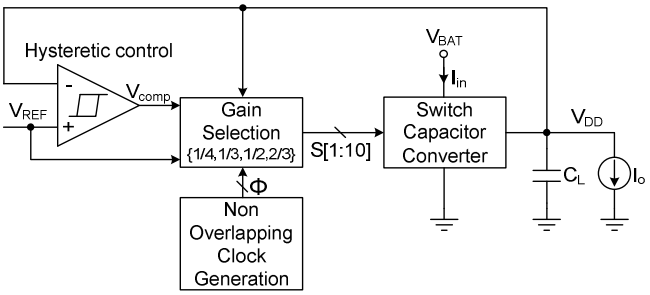
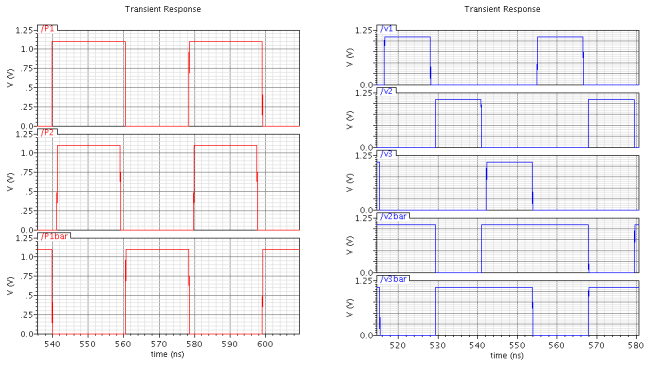


Fig. 3. Block diagram of the Hysteretic mode control regulated SCC.



(a) (b)

Fig. 4. Clock waveforms of topologies: (a) G={1/3,1/2,2/3}and (b) G=1/4.

clock generation block (Fig. 3). Fig. 4 illustrates the clock waveforms which are involved in the operation of the converter. The gain selection block activates one of the four topologies, depending on the proximity of its target voltage to the load voltage being delivered and its ability to provide the load power demand. To facilitate a tight regulation and achieve high efficiency, the converter should employ a feedback controller. A typical hysteretic mode control (burst mode) is used, although other techniques such as PFM are also feasible. The converter uses the hysteretic mode control to maintain the feedback voltage V_{DD} within the hysteretic band of ±ΔV, where ΔV is set to 10mV. In this method, the converter remains idle until the output voltage falls below V_{REF}-ΔV. At this point, the output of the comparator V_{comp} switches to a high state and thereby enables the SCC to transfer charge packets to the load.

III. OPTIMIZATION

The proposed circuit was tested and characterized in a standard low power 40nm TSMC CMOS process. To avoid a short channel effect, the channel length was set three times larger than the minimum technology L_{min} namely, L=120nm. The widths of the switches and additional parameters are adjusted by a global optimization procedure using a parallel simulated annealing algorithm. A global optimization was performed by evaluating the average efficiency and unregulated output V_{DD} over a range of switches' widths and flying capacitors C_{f1}=C_{f2}, until the system specifications were satisfied. As mentioned above, to facilitate a variable output V_{DD}, the following optimization is based on a behavioral Verilog-A controller which switches conveniently between the four possible topologies.

The optimization procedure was conducted using the following assumptions and conditions:

7) All losses are considered except the losses of the control circuit, which is reasonable to assume negligible compared with major loss factors,
8) The switching frequency f_{sw} was set for simplicity to a fixed value of f_{sw}=26MHz.
9) The SCC was implemented with low V_t MOS transistors of the process library,
10) The output capacitor (Fig. 3) was set to C_L=1nF to fulfill a requirement of Δ_{ripple}=8mV maximum output ripple by the relation $C_L=I_o/(\Delta_{ripple}f_{sw})$ [12].

TABLE I
OPTIMIZATION OF SCC PARAMETERS

Optimized Parameter	Optimization range (min:step:max)	Final value
W_1=W_6	1µm:30:400µm	18.03µm
W_4=W_9	1µm:30:400µm	62.30µm
W_2	1µm:30:400µm	27.26µm
W_3	1µm:30:400µm	115.8µm
W_5	1µm:30:400µm	41.21µm
W_7	1µm:30:400µm	27.26µm
W_8	1µm:30:400µm	264.6µm
W_{10}	1µm:30:400µm	33.52µm
m_{f1}= m_{f2}	1:30:1000	386

The parameter W_i corresponds to the width of the switch M_i where i=1,2,…,10. The parameters m_{f1}=m_{f2} define the number of 1.14pF @ 1.1V nMOS capacitors connected in parallel to implement the flying capacitors C_{f1}=C_{f2}.

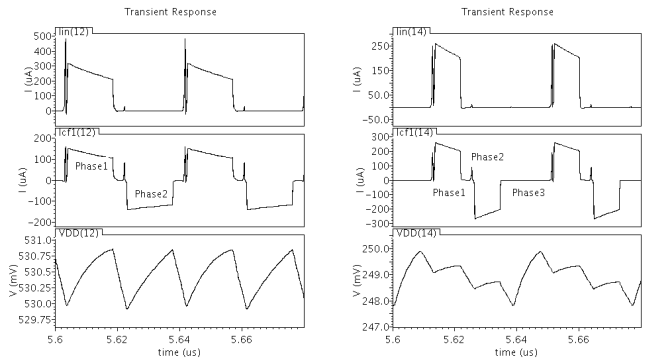
Each designable parameter was constrained to take values from a limited range. The performance function of the circuit, which also serves as goal function with highest weight, is the average efficiency of the four topologies defined as

$$\eta_{avg} = \frac{\eta_{14} + \eta_{13} + \eta_{12} + \eta_{34}}{4} \quad (4)$$

where η_{14}, η_{13}, η_{12} and η_{23} are the efficiencies of topologies G={1/4,1/3,1/2,2/3}, respectively. The efficiencies were evaluated at a maximum current of I_o=200uA and with the corresponding unregulated output voltages (open loop control). Unregulated output voltage is the obtainable steady state output voltage of a topology, while the output of the comparator V_{comp} (Fig. 3) is maintained in a high state. The average efficiency η_{avg} and the four efficiencies at the respective unregulated maximum output voltages were constrained to satisfy the following,

$$78\% \le \eta_{avg} \le 83\% \quad (5)$$

and simultaneously,



(a) (b)

Fig. 5. Open loop key waveforms of the SCC at I_o=200µA. Traces from top to bottom i_{in}, i_{Cfl}, v_{DD} for: (a) G=1/2, (b) G=1/4.

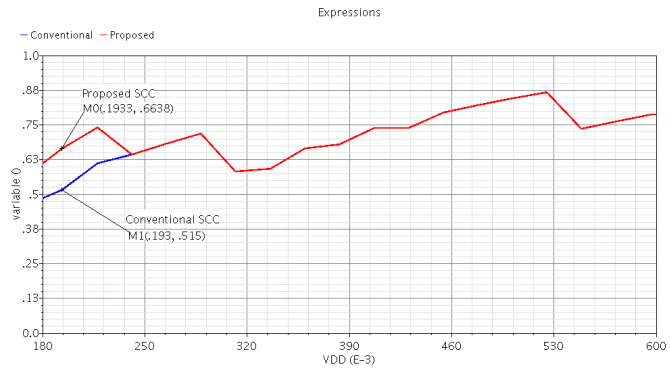


Fig. 6. SCC efficiency versus load voltage V_{DD} with and without G=1/4 topology over 0.18V≤V_{DD}≤0.6V for I_o=200µA.

$$\begin{aligned} V_{DD(14)} &\geq 0.2V \\ V_{DD(13)} &\geq 0.3V \\ V_{DD(12)} &\geq 0.5V \\ V_{DD(23)} &\geq 0.6V \end{aligned} \qquad (6)$$

while letting the optimizer engine to choose values such that the SCC comply with constraints (5) and (6). In our case the average efficiency η_{avg} constrained between 78% and 83%, which is acceptable since most SCC designs actually fall into this range.

TABLE I summarizes all design variables involved in the optimization procedure, corresponding optimization ranges of legal values and the final optimum values. We note that the notation MIN:STEPS:MAX in TABLE I represents optimization scanning range in which MIN and MAX are the lower and upper bounds, respectively. The parameter STEPS defines number of unequally spaced values between MIN and MAX limits. For example, the format 1µm:30:400µm indicates that the engine searches automatically up to 30 different unequally spaced widths values within 1µm to 400µm to comply with the optimization criteria.

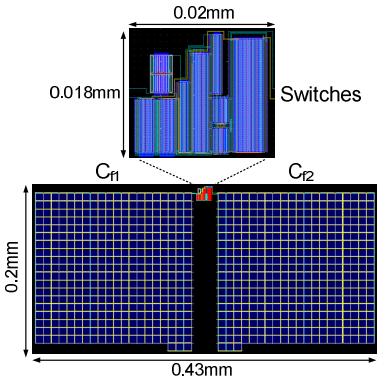
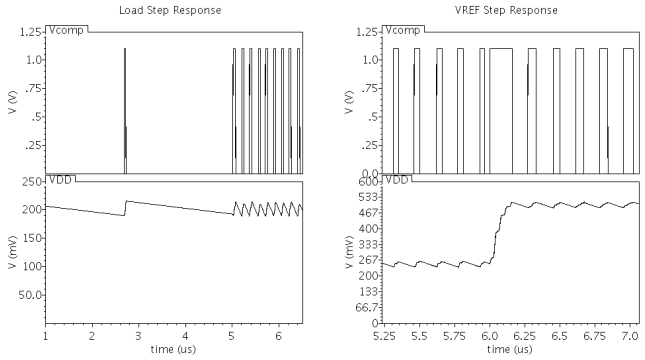


Fig. 7. Layout of the proposed SCC.



(a) (b)

Fig. 8. Closed loop dynamic step response of v_{comp} (top) and v_{DD} (bottom) with: (a) output current I_o step from 10µA to 200µA at V_{DD}=0.2V, (b) output voltage V_{DD} step from 0.25V to 0.5V at I_o=200µA.

IV. SIMULATION RESULTS

The SCC was implemented and simulated using Cadence Spectre simulator. Flying capacitors are obtained using nMOS capacitors connected in parallel. In this design, the bulk of all nMOS transistors have been tied to ground while the bulk of the pMOS transistors were tied to V_{BAT}=1.1V. No level shifters were used hence, the input voltage V_{BAT} has been used as a rail for the gate drive of all transistors, causing to a gate voltage swing between ground and V_{BAT}.

Fig. 5 shows key waveforms of the SCC at two operating points. As evident from the figure the parameters of the SCC are optimized to work in incomplete transfer mode. It can be noticed that using G=1/2 topology the operation is governed by two clock phases while with G=1/4 topology, one clock period is divided into three time sessions.

The efficiency plot of both conventional and proposed SC converters, while delivering a load current of 200µA is depicted in Fig. 6. The result shows that the proposed SCC dramatically improves the efficiency at low output voltages. Specifically, the SCC efficiency is improved by 16% in the vicinity of V_{DD}=200mV as compared to the one using a conventional 9 switch topology [6], [8] while remaining with the same efficiency at the rest of the range. The SCC achieves a peak efficiency of 87% at V_{DD}=0.53V with 200µA load current.

Fig. 7 shows the layout of the SCC power stage. The total active area that is consumed by the switches and the flying capacitors is 0.086mm^2. Fig. 8 depicts the post-layout simulation transient response of the SCC when the reference voltage V_{REF} and the output load current I_o are allowed to change.

Theoretically, the load current could be higher however the aim of the study is to present a general concept of SCC optimization. Furthermore, in higher output power the SCC is subject to performance degradation due to higher voltage/current ripples, parasitical effects and larger driver. Nevertheless, it is evident that the proposed circuit has a comparatively small number of power switches and silicon area, while supporting four different conversion ratios.

V. CONCLUSIONS

This work has presented an SC converter with four conversion ratios. We have shown that the proposed converter can deliver scalable load voltages using the core 40nm 1.1V CMOS devices. The presented concept is general and not depends on particular implementation technology. Four different conversion ratios were employed by the addition of a single power switch to the conventional topology (Fig. 1). The additional conversion ratio of G=1/4 was obtained by dividing the charge transfer process into three time sessions. Simulation results showed that the proposed SCC dramatically improves the efficiency in sub-200mV load voltages. The SCC achieves an efficiency improvement of 16% in the vicinity of V_{DD}=200mV as compared to the conventional topology (Fig. 1) and a peak efficiency of 87% at V_{DD}=0.53V.

It can thus be concluded that the proposed optimization procedure provides an effective solution for designing SCC along with constraints on parameters' values.

ACKNOWLEDGMENT

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APPENDIX

HYSTERETIC CONTROL BLOCK IN VERILOG-A

```
`include "constants.vams"
`include "disciplines.vams"

module Hysteretic_Control(comp,ref,dc);

input ref,dc;
output comp;
electrical comp,ref,dc;

parameter real period=1n;
parameter real offset=0;
parameter real hyst=0.01;
parameter real logic_high=1.1;
real samp;
integer q;

analog begin
        @(timer(offset,period)) begin
                samp=V(dc);
        end
        if (samp>(V(ref)+hyst)) begin
                q=1;
        end
        else if (samp<(V(ref)-hyst)) begin
                q=0;
        end

V(comp) <+ logic_high*!q;

end
endmodule
```