Generic Average Modeling and Simulation of the Static and Dynamic Behavior of Switched Capacitor Converters

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***Abstract*—A generic behavioral average circuit model of a Switched Capacitor Converter (SCC) is proposed and verified. The model is based on the average currents concept and assumes that each of the SCC subcircuits can be described or approximated as a first order network. The model can be used to calculate or simulate the average static, dynamic and small signal responses of the SCC. The model is valid for all operational modes of a SCC (complete, partial and no charge) and is compatible with any circuit simulator that includes dependent sources. Excellent agreement was found between the behavior of the proposed average model, full circuit simulation, and experimental results.**

I. INTRODUCTION

Switched Capacitor Converters (denoted as SCC for singular and plural instances), also referred to as 'Charge Pumps,' are preferred in a number of cases due to their IC compatibility, relatively small size, and the absence of magnetic elements. SCC can be modeled as a network that is configured by the switches to a set of subcircuits that charge and discharge flying capacitors. The average behavior of SCC systems was analyzed in numerous earlier studies (e.g. [1-10]), in which the expressions of the voltage transfer ratios and the expected losses were derived.

The objective of this study was to develop an average model of SCC systems that would be compatible with any circuit simulator and would be capable of reproducing the static and dynamic behavior of the converter including the small signal control-to-output transfer function. The proposed simulation model is in fact a translation of the analytical results of [10] into average equivalent circuits. As such, the accuracy of the model is identical to the results of [10] and it is limited by the assumptions of its derivation (such that the subcircuits can be represented or approximated by a first order RC circuit). As experienced in the case of switched inductor converters, average circuit simulation [11-14] could alleviate convergence problems and can provide additional information and a better insight into the simulated converter.

This work was supported by the ISRAEL SCIENCE FOUNDATION (Grant 476/08 and Grant 517/11)

II. BASIC THEORETICAL CONSIDERATIONS

For the sake of clarity and brevity, we consider first a 1:1 SCC system depicted in Fig. 1. The converter includes a flying capacitor C_f, with a lossy component ESR, two switches S_1 and S_2 with 'on' resistances of R_{s1} and R_{s2} respectively, an output filter capacitor C_o with ESR_o and load resistance R_o. As the switches run at a frequency of f_s, the circuit toggles between two subcircuits: one during T_1, when S_1 is 'on', and the other during T_2, when S_2 is 'on.'

Each of the subcircuits can be represented by a generic charging circuit (Fig. 2) that includes a voltage source ΔV_i (where i is 1 for duration T_1 and 2 for T_2) a resistor R_i and a capacitor C_i with an initial condition of zero voltage [10].

For the 1:1 converter:

$$R_1 = R_{s1} + ESR \quad (1); \qquad R_2 = R_{s2} + ESR + ESR_o \quad (2)$$

$$C_1 = C_f \quad (3); \qquad C_2 = \frac{C_f \cdot C_o}{C_f + C_o} \quad (4)$$

ΔV_i is the initial voltage difference between the capacitor and the input voltage (for T_1) or the output voltage (for T_2) just before the relevant switch is turned on.

Once a switch is turned on, the equivalent capacitor will start charging (by a positive or negative ΔV_i) and a current $i_i(t)$ will build up. Depending on the relationship between the duration T_i and the time constant R_iC_i, the current can take one of three possible shapes. For $T_i >> R_iC_i$, the charging will be completed within T_i (Fig. 3a); this case is denoted as CC.

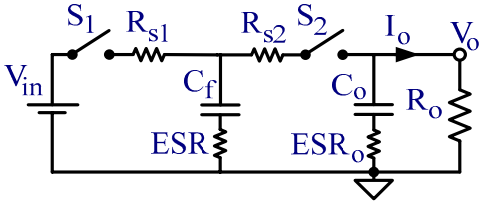

Figure 1. A unity conversion ratio SCC.

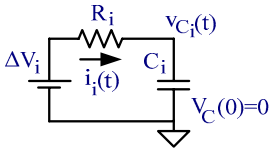

Figure 2. The generic capacitor-charging equivalent circuit.

For $T_i \cong R_iC_i$, the charging will be partial (PC, Fig. 3b). For $T_i << R_iC_i$, there will be no effective charging (NC,) and the current will be practically constant (Fig. 3c). In this latter case, the capacitor voltage will stay about constant within T_i [15].

As was proven in an earlier publication [10], the average power P_i dissipated by a given subcircuit i during a switching phase duration T_i can be expressed as a function of the average current I_{avi} in the subcircuit (averaged over the switching period $T_s=1/f_s$):

$$P_i = \left(I_{av_i}\right)^2 \cdot \left\{\frac{1}{2f_sC_i}\cdot\frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})}\right\};\ \beta_i = \frac{T_i}{R_iC_i} \qquad (5)$$

The term in brackets can be defined as the equivalent resistance R_{ei} of subcircuit i:

$$R_{e_i} = \left\{\frac{1}{2f_sC_i}\cdot\frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})}\right\} = \frac{1}{2f_sC_i}\cdot\coth\left(\frac{\beta_i}{2}\right) \qquad (6)$$

The behavior of R_{ei} over the full range of the charge/discharge regions (CC, PC, and NC) is given in Fig. 4. The plot presents the normalized equivalent resistance of a single charge or discharge subcircuit as defined by (7). The definition is based on (6) which is normalized by the factor $1/(m\cdot R_i)$ and assumes symmetrical operation (same switching duration for each of the m subcircuits). For the two switching phases in the unity SCC of Fig. 1, m = 2.

$$R^*_{e_i} = \frac{R_{e_i}}{m\cdot R_i} = \frac{\beta_i}{2}\cdot\coth\left(\frac{\beta_i}{2}\right) \qquad (7)$$

Based on these results, the average behavior of the instantaneous equivalent circuit for duration T_i (Fig. 2) can be represented by a generic **average equivalent subcircuit** (Fig. 5), in which all the variables are average values (averaged over the switching period): V_{Cavi} is the value of the capacitor voltage during the time frame T_i, I_{avi} is the average current in the subcircuit, calculated by integrating the charge transferred in the i^{th} subcircuit during T_i, and divided by the full switching period T_s, R_{ei} is the equivalent resistance of subcircuit i, as per (6), and C_i is the total capacitance of subcircuit i.

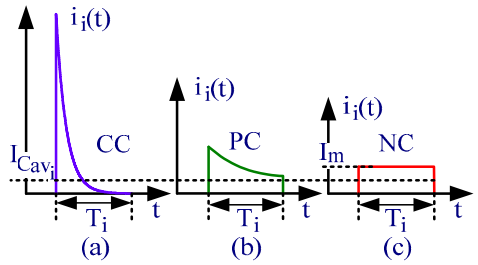

Figure 3. Possible charging current shapes. (a) Complete charge (CC). (b) Partial charge (PC). (c) No charge (NC).

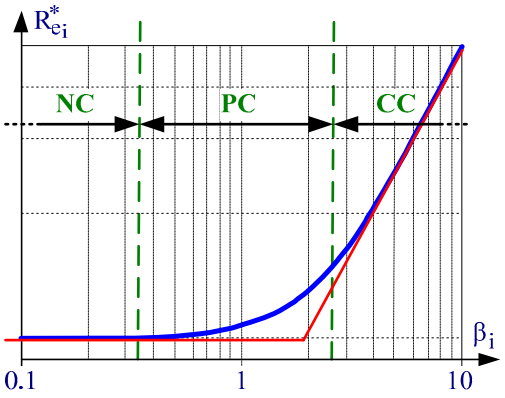

Figure 4. Behavior of the normalized equivalent resistance of a single RC subcircuit as a function of β_i (5) (which defines the different operational modes).

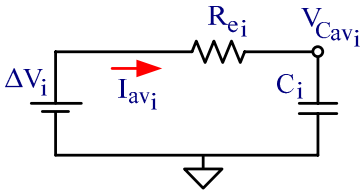

Figure 5. Generic average equivalent subcircuit.

It should be noted that consistent with the conventional assumption of average models, V_{Cavi} and I_{avi} are assumed to be constant during the switching period T_s. However, these variables are still time dependent under the normal restriction that their bandwidth is much smaller than the switching frequency of the SCC.

III. The SCC Average Modeling Approach

Based on the above observations regarding the generic average circuit behavior, one can conclude that the average current and average voltages of each subcircuit can be obtained by eliminating the switching action altogether and replacing the physical resistances by R_{ei} for each subcircuit. The two subcircuits of the 1:1 SCC discussed here (Fig. 6a) can then be combined into one average circuit (Fig. 6b). This fusion is allowed considering the following two fundamental key points. First, the average potentials of the flying capacitor C_f terminals in the two subcircuits are identical. The second point is the fact that this flying capacitor connection is restoring the real total average current via the capacitor. That is, the fact that the capacitor is charged by subcircuit 1 and discharged by subcircuit 2. In steady state these currents are equal and the net charging/discharging current is zero. In transient or small signal analysis the momentary charging/discharging current may not cancel each other which will cause the capacitor voltage to change. Hence, the average model of Fig. 6b not only retains the correct power dissipation of the circuit by virtue of (5), but also retains the dynamics of the system since the capacitors are exposed to the correct average currents that flow in the physical SCC. Considering the above the average equivalent circuit of Fig. 6b represents the average static and dynamic behavior of the unity gain converter of Fig. 1, while being transparent to the switching action.

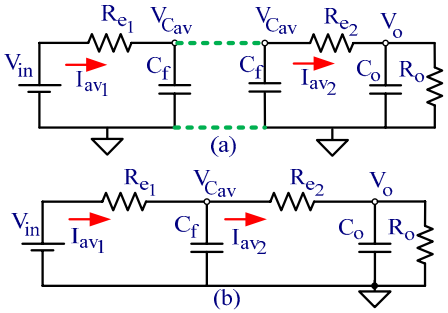

Figure 6. Average equivalent circuit model of the unity SCC of Fig. 1. (a) The two separated subcircuits. (b) The subcircuits combined.

The average equivalent circuit (Fig. 6b) is linear for any given switching mode since the R_{ei} values are voltage and current independent if R_i, f_s, and T_i are kept constant (the possible change of R_i when MOSFET switches are used is neglected in the present average model). The static steady-state DC values of the SCC voltage and currents can be easily obtained from the average model by simple circuit analysis or by simulation (only "Bias Point" analysis will be required). In the private case of the 1:1 SCC considered here the DC values can be obtained by inspection. At steady state the net average currents via the flying capacitor C_f and the output capacitors are zero and hence:

$$I_{av_1} = I_{av_2} = I_o = I_{in} \tag{8}$$

this implies:

$$V_o = V_{in}\frac{R_o}{R_o + R_{e_1} + R_{e_2}} \tag{9}$$

which conforms to the classical equivalent circuit model of the SCC [10, 15] that represents it as a voltage source $M \cdot V_{in}$ (M is the open circuit conversion ratio of the SCC) and an internal resistance R_e (Fig. 7) which, for the 1:1 SCC discussed here, are equal to M = 1, and $R_e = (R_{e1}+R_{e2})$.

Notwithstanding the ability of the proposed model to follow the steady state behavior of the SCC, its novelty is in the ability to emulate the dynamic responses. Being a linear circuit, the proposed equivalent circuit model can be analyzed or simulated, as is, to examine the dynamic large signal behavior at start up and the large and small signal responses to input voltage or load changes. For example, a straightforward small signal analysis can be used to yield the input (v_{in}) to output (v_o) response (audio susceptibility):

$$\frac{v_o}{v_{in}}(s) = \frac{1}{a \cdot s^2 + b \cdot s + c}$$

$$\left\{ a = C_f C_o R_{e_1} R_{e_2};\ c = \left(\frac{R_{e_1} + R_{e_2} + R_o}{R_o} \right) \right\}$$

$$\left\{ b = C_o (R_{e_1} + R_{e_2}) + C_f R_{e_1} \left(\frac{R_{e_2} + R_o}{R_o} \right) \right\} \tag{10}$$

An experimental validation of this transfer function is given in the experimental section (Part VI).

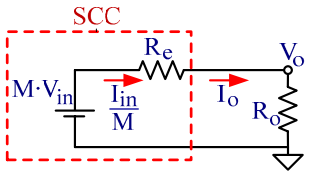

Figure 7. Static equivalent circuit of SCC.

The proposed model can also be used in a simple way to evaluate the effect of a step change in the switching frequency and/or the duty cycle. This will be illustrated by considering the case of a step in switching frequency. Based on (6) a step in f_s will cause, in general, a change in the value of R_{ei}. This can be represented as a switched circuit in which the equivalent resistances are replaced at the instance of the frequency change by new values (Fig. 8).

The large signal response of the resulting switched equivalent circuit of Fig. 8 can be derived analytically or simulated by any circuit simulator. For example, in the PSpice environment the switches will be replaced by Sbreak elements that will be controlled by voltage pulse sources (VPULSE).

In the above example the proposed average model was treated as a linear circuit or a switched linear circuit. When considering regulated SCC, the small signal response between the control signal and the output voltage is of interest. These nonlinear relationships can be obtained by the proposed average model but require some circuit preparation as discussed next.

IV. CONTROL TO OUTPUT RESPONSE

Two basic approaches can be used to regulate the output voltage of a SCC: duty cycle control [16] and frequency control [17], including frequency hopping and dithering [18] (control methods that are based on current sources that charge one or more of the flying capacitors [19-21] are beyond the scope of this paper). These methods are in fact based on the control of one or more R_{ei} of the subcircuits. That is, regulation is accomplished by increasing/decreasing the losses of the SCC. This stems from the observation, as discussed in many papers [e.g. 4, 22, 23], that the efficiency, η, of SCC systems is linked to input to output voltage ratio by (11).

$$\eta = \frac{V_o}{M \cdot V_{in}} \tag{11}$$

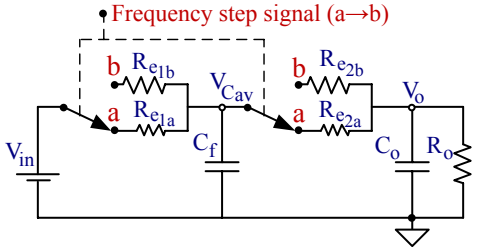

Figure 8. Average model of the 1:1 SCC for simulating a step change in switching frequency. State "a" is an initial state with equivalent resistance of $R_{e,ia}$ (i = 1,2), state "b" is after the frequency step with equivalent resistance of $R_{e,ib}$.

Hence, for a fixed M, output voltage regulation is accomplished by controlling the efficiency namely, by increasing/decreasing one or more of the equivalent resistances of the SCC which are responsible for the conduction losses [23]. This can be elucidated by considering the general equivalent circuit of the SCC (Fig. 7), which implies that the output voltage of an SCC can be expressed as:

$$V_o = M \cdot V_{in} \frac{R_o}{R_e + R_o} \tag{12}$$

Equation (12) explicitly shows the dependence of the output voltage on R_e which, in turn, is a linear function of the subcircuits' equivalent resistance, R_{ei} [10, 15].

Considering (6), the required adjustment of the equivalent resistance of one or more of the subcircuits for regulation purposes can be carried out by changing the switching frequency f_s, and/or by controlling T_i. For example, in the case of regulation by frequency control the relationship between the subcircuits' equivalent resistance and the switching frequency can be expressed as:

$$R_{e_i}(f_s) = \left\{ \frac{1}{2f_s C_i} \cdot \frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})} \right\} = \frac{1}{2f_s C_i} \cdot \coth\left(\frac{\beta_i}{2}\right) \tag{13}$$

where $\beta_i = 1/(mf_sR_iC_i)$.

Based on the above, modeling the large signal control-to-output voltage response can be accomplished by emulating the equivalent resistances of the proposed model by dependent resistors. This can be conveniently realized by dependent current sources that are a function of the voltage across them V_R and a control variable I_G (Fig. 9) such that $I_G = V_R/r$. In this case the emulated resistance R will be equal to r.

This dependent resistance compatible with standard circuit simulators such as SPICE based simulator (e.g. OrCAD PSpice [Cadence design systems, Inc., ver. 16.3]) and discrete event simulation (such as PSIM [Powersim Inc., ver. 9.0]). An example of an implementation that applies the PSpice capabilities is depicted in Fig. 10. In this case the switching frequency is emulated by a voltage ($V \equiv f_s$, node *V_inj* Fig. 10) which is the variable in the expression of GVALUE (14). A convenient emulation factor would be 1Hz = 1V.

The expression of the GVALUE (Fig. 10) will thus be:

$$\text{EXPRESSION} = \frac{\{V(\%IN+) - V(\%IN-)\}}{\left\{ \frac{1}{2 \cdot V(V\_inj) \cdot C\_1} \cdot \frac{1+e^{-\frac{1}{2 \cdot V(V\_inj) \cdot R\_1 \cdot C\_1}}}{1-e^{-\frac{1}{2 \cdot V(V\_inj) \cdot R\_1 \cdot C\_1}}} \right\}} \tag{14}$$

where R_1, C_1 are the total resistance and capacitance of the subcircuit '1'; V(%IN+)-V(%IN-) is the input voltage to the GVALUE, and V(V_inj) is the voltage of node *V_inj* (Fig. 10).

The (static) dependence of V_o on the switching frequency f_s can be obtained by running a DC analysis on the circuit in which the DC voltage source (Switching_Frequency, Fig. 10)

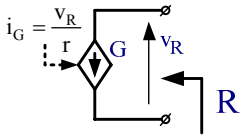

Figure 9. Emulation of a dependent resistor by a dependent current source, R = r.

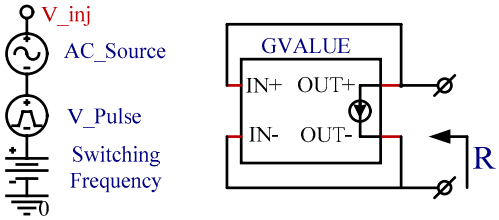

Figure 10. Implementation of a dependent equivalent resistance in PSpice.

is swept over the desired range. This same schematic can also be used to simulate the output voltage response to a step change in switching frequency. The relevant analysis in this case is TRANSIENT analysis, and the excitation source that mimics the frequency change will be V_Pulse (Fig. 10).

Notwithstanding the simulation capabilities listed above, the real power of the proposed modeling approach is the ability to obtain the small signal, control to output voltage response of an SCC. This response is a prerequisite for optimal design of the compensator. Since the control to output voltage response is in general a nonlinear function (as evident from (6)), analytical derivation of this function will require extensive effort using techniques such as perturbation or linearization by differentiation. However, a simpler and more "user friendly" approach would be to apply simulation tools to extract the required small signal responses by taking advantage of the automatic linearization algorithm embedded in the AC analysis of SPICE. No mathematical derivation will be required in this case and the circuit (Fig. 6b) can be run, as is, to obtain the small signal response. The relevant excitation will be the VAC source (AC_Source, Fig. 10) and the analysis will be carried out around the operating point set by the DC source (Switching_Frequency, Fig. 10) that emulates the switching frequency at the operating point.

PSIM users could also easily simulate the small signal control to output voltage response even though this simulator does not have a linearization capability. Instead, PSIM applies time domain analysis to obtain the "small signal response" by injecting sinusoidal signals at various frequencies over the desired range. The controlled resistor can be realized in the PSIM environment by the built in "nonlinear element" (Fig. 11) which is in fact also a controlled current source. The current of this element is i = v/x, where "i" is the current thorough the element, "v" the voltage across the element and "x" is the control parameter.

In Fig. 11, x = *V_req_i* and represents the equivalent resistance of phase i. This voltage is calculated on the fly during the simulation as a function of the control parameter (frequency, or duty cycle). The calculation can be carried out

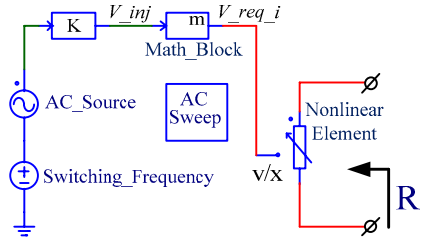

Figure 11. Implementation of dependent equivalent resistance in PSIM.

in PSIM by a "Math_Block". The example of Fig. 11 shows the arrangement for obtaining the small signal response in frequency control. The operating point is set by the DC voltage source "Switching_Frequency", while the "AC_Source" provides the time domain excitation at the specified frequency range. The "Math Block" expression for emulation of R_{el} as a function of variable frequency in the 1:1 inverting SCC case (Fig. 13) is given in (15), which is the implementation of (6) using PSIM syntax:

$$V\_req\_i = \frac{1}{2 \cdot V\_Inj \cdot C\_1} \cdot \frac{1 + e^{-\frac{1}{2 \cdot V\_Inj \cdot R\_1 \cdot C\_1}}}{1 - e^{-\frac{1}{2 \cdot V\_Inj \cdot R\_1 \cdot C\_1}}} \qquad (15)$$

where *V_req_i* is the output voltage of the "Math_Block", and *V_inj* is the input voltage to the "Math Block". The unity gain block - "K" (Fig. 11) is required for signal integrity within PSIM.

"AC analysis" in PSIM is carried out by specifying the range of frequencies for the "AC_Source" using the "AC Sweep" element (Fig. 11). The signal generated by the "AC_Source" is added to the steady state frequency emulated by "Switching_frequency" DC source and fed to the "Math_Block" which calculates the equivalent resistance value that is fed to the "Nonlinear Element". The waveforms involved are depicted in Fig. 12. Fig. 12a represents the momentary frequency (coded into voltage). Fig. 12b is the calculated equivalent resistance and Fig. 12c shows the resultant effect on the output. These time domain signals are used by PSIM to plot the "small signal" frequency to output voltage response.

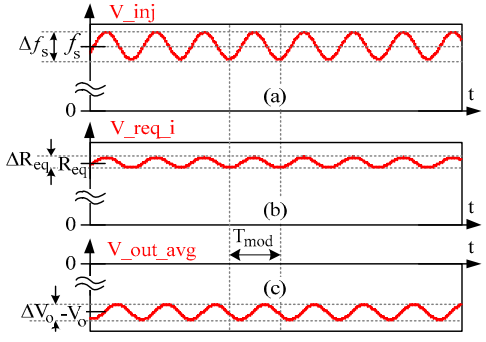

Figure 12. Typical waveforms along the generation chain of frequency dependent resistor (Fig. 10) in PSIM. (a) The voltage signal that represents the momentary frequency (V_inj Fig. 10); (b) The voltage signal that represents the equivalent resistance (*V_req_i* Fig. 10a); (c) The resulting voltage modulation on the SCC output voltage.

Duty cycle dependent signals could be generated in a similar way, with the difference that the input sources will represent duty cycle rather than frequency, and the expressions in the "Math Block" in PSIM, or GVALUE in PSpice will be a function of the duty cycle rather than frequency.

It should be pointed out that the small signal responses could be obtained in PSIM by running it in the full switched circuit mode. That is, running the original circuit with all the switches and physical resistances. The small signal frequency to output voltage response will be obtained in this case by modulating the switching frequency. The advantage of using the average circuit model rather than the full switched circuit is twofold. First, running time will be shorter since smaller steps would suffice. Another advantage of the average model is the transparency to the switching frequency. The full circuit will include a ripple component that might interfere with the PSIM "AC analysis".

Experimental verifications of the small signal responses obtained by the proposed average model are given below.

V. Extension to More Complex Structures

The modeling concept outlined above can be easily extended to more complex SCC structures including multiphase implementations as long as the subcircuits can be described or approximated by a first order RC network [10]. Also, the model can handle SCC topologies that include diodes. This will be demonstrated by considering an inverting, two phase 1:1 SCC (often referred to as a charge pump) (Fig. 13). The first modeling step will be, as discussed in section II, to identify the two subcircuits according to the operational phases, corresponding to the charge (i = 1, Fig. 14a), and the discharge (i = 2, Fig. 14b) durations.

Total subcircuit resistances and capacitances are calculated for both phases to be (16),

$$\begin{aligned} R_1 &= R_{s1} + ESR; & R_2 &= R_{s2} + ESR + ESR_o \\ C_1 &= C_f; & C_2 &= \frac{C_f \cdot C_o}{C_f + C_o} \end{aligned} \qquad (16)$$

and following (5) and (6), β-s (17), and equivalent resistances (18), are expressed.

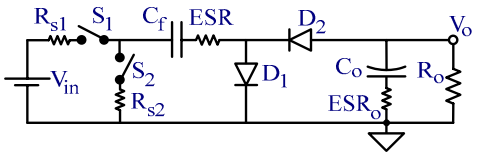

Figure 13. The demonstrated SCC (Inverting, 1:1 ratio).

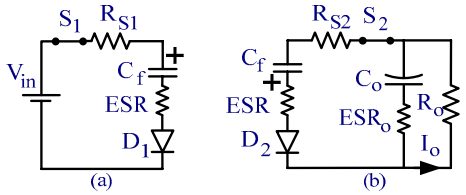

Figure 14. Inverting 1:1 SCC, instantaneous subcircuits: (a) Charging (i = 1), (b) Discharging (i = 2).

$$\beta_1 = \frac{1}{2f_s \cdot (R_{S_1} + ESR) \cdot C_f}$$
$$\beta_2 = \frac{1}{2f_s \cdot (R_{S_2} + ESR + ESR_o) \cdot \left(\frac{C_f \cdot C_o}{C_f + C_o}\right)} \quad (17)$$

$$R_{e_1} = \frac{1}{2f_s C_f} \cdot \coth\left(\frac{\beta_1}{2}\right) - R_{e_2} = \frac{1}{2f_s\left(\frac{C_f \cdot C_o}{C_f + C_o}\right)} \cdot \coth\left(\frac{\beta_2}{2}\right) \quad (18)$$

For each of the instantaneous subcircuits of Fig. 14 an equivalent average subcircuit is created according to Fig. 5, and finally these equivalent average subcircuits are connected into the complete average equivalent model circuit (Fig. 15). This average model is an implementation of the concepts outlined above, except that in this case there is a need to overcome the fact that the flying capacitor in the two subcircuits is indeed flying. Namely, none of its terminals share a common potential in the two circuits. This is resolved by placing the capacitor in one subcircuit and reflecting it to the other subcircuit by a "DC transformer", which is realized by dependent sources E_T and G_T (Fig. 15). The relationships between currents and voltages of the "DC transformer" are given in (19), consistent with the notation of Fig. 15.

$$\begin{bmatrix} V_{T1} \\ I_{T_1} \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & 1/n \end{bmatrix} \begin{bmatrix} V_{T2} \\ -I_{T2} \end{bmatrix} \quad (19)$$

Where n is the transformation ratio between the primary and the secondary of the transformer. In the discussed inverting 1:1 SCC (Fig. 13), n = 1.

Furthermore, based on the results of [10], the effect of the diodes on the operation of the circuit is modeled by voltage sources V_{D1} and V_{D2} (Fig. 15). This is correct considering the fact that the proposed average model emulates the average currents in the SCC and that diode losses are a function of the average currents (assuming some equivalent average voltage across the diode while conducting). Here we neglect the incremental resistances of the diodes. The model of Fig. 15 is correct under the assumption $R_o >> ESR_o$ and neglects the effect of ESR_o on the dynamics of the system.

The equivalent circuit of Fig. 15 can be used, as is, to simulate the large and small signal responses of the studied SCC. These responses can also be derived analytically by solving the state space equations of the circuit or by Kirchhoff - Laplace equations. However, analytical derivation of the control to output responses will require extensive analytical work considering the non-linearity of the model. Comparison of experimental results to average model simulations of this inverting 1:1 SCC is given in Section VI.

VI. Model Verification

The proposed SCC generic behavioral average circuit model was verified against full circuit simulation (Cycle-By-Cycle) carried out on two different software packages – PSIM and OrCAD PSpice, and against experimental results carried out on a laboratory breadboards. The experimental devices and parameters were as follows: Duty Cycle = 50%;

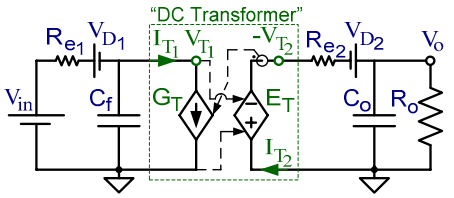

Figure 15. Equivalent circuit based, average model of the inverting SCC of Fig. 13.

Dead Time = 120ns; Input voltage V_{in} = 12V; Switches S_1 - SMU10P05, S_2 - SMU15N05; Flying capacitor C_f = 22μF and ESR = 0.1Ω; Output capacitor C_o = 560μF. For the inverting SCC Diodes V_{D1} and V_{D2} - MBR320P; and ESR_o = 33mΩ were also used. Experiments and simulations covered all operational modes: CC with f_s = 5kHz, PC with f_s = 50kHz, and NC with f_s = 250kHz.

Fig. 16 shows the input (v_{in}) to output (v_o) response (audio susceptibility) of the unity 1:1 SCC (Fig. 1). The figure includes the amplitude and phase responses as obtained by (a) plotting the analytical expression (10), which was obtained by signal analysis circuit model of Fig. 6, (b) results of full (switched) circuit AC analysis simulation by PSIM, and (c) Experimental results. In this experimental test, higher switching noise was observed due to the reduced input capacitance making phase readings in experiments above 1 kHz to be erroneous. Therefore, experimental phase readings above 2 kHz in Fig. 16 are omitted.

Fig. 17 shows start up transients, Fig. 18 depicts a load step response, and Fig. 19 shows the small signal responses of $\{v_o/f_s(f)\}$ obtained by the average model simulation and experimentally. The small deviations of the experimental results from average model simulations are probably due to experimental uncertainties such as errors in the exact values of the capacitances and resistances (ESR), nonlinearities, etc.

VII. Discussion and Conclusions

The main attributes of the proposed new modeling approach is that it is based on average modeling and that the resulting SPICE and PSIM compatible equivalent circuits, emulate the large and small signal responses of the modeled SCC. The model covers all operational modes (CC, PC, and NC) and can be used to examine the effects of individual elements such as the resistance of each switch, the ESR of each capacitor, the influence of the capacitors' values and the effect of the switching frequency and duty cycle. A powerful feature of the model is its seamless compatibility with SPICE based AC simulation in which the linearization is done by the simulator. The model is also compatible with the PSIM simulator, and similar discrete event simulators for both large and "small signal" analyses. These powerful capabilities can be used conveniently to obtain the small signal control to output responses for various control methods such as duty cycle control or frequency control.

Although discussed and demonstrated by a simple 1:1 SCC, the proposed modeling methodology can be easily applied to multi-capacitor and multi-phase SCC systems such as those described in [18]. A fundamental limitation of the model is that it assumes that all subcircuits can be represented

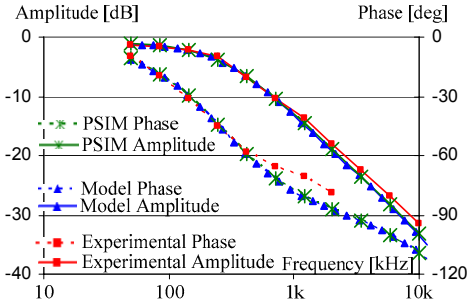

Figure 16. Input (v_{in}) to output (v_o) response (audio susceptibility) of the unity SCC ofFig. 1. Asterisks – Full circuit simulation results; Triangles – Traces of the Average model based analytical derivation (10); Squares - Experimental results; Solid traces – Amplitude response; Dashed traces – Phase response.

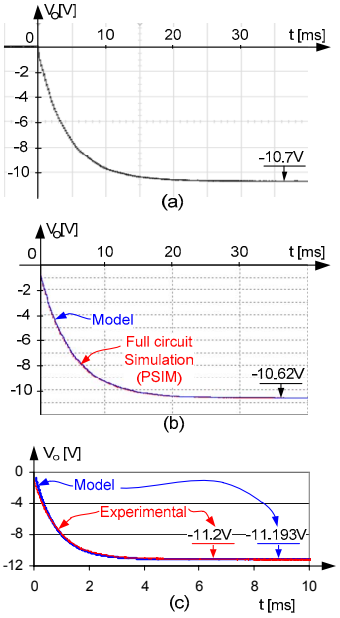

Figure 17. Start-up transients of the inverting 1:1 SCC: (a) Experimental - CC mode, (b) Full (switched circuit) simulation and model based average simulation - CC mode, (c) Experimental and average model simulation - NC mode. Please note: in (b) and (c) the two traces are on top of each other.

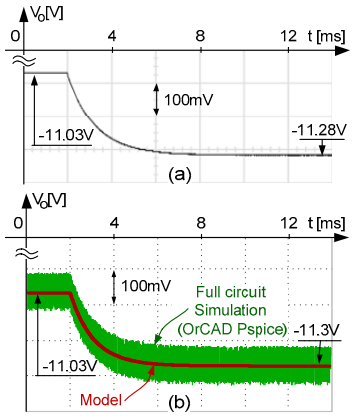

Figure 18. Load-step response of the inverting 1:1 SCC - PC Mode (a) Experimental, (b) Wide trace – full circuit simulation; Solid thick trace – Average model simulation.

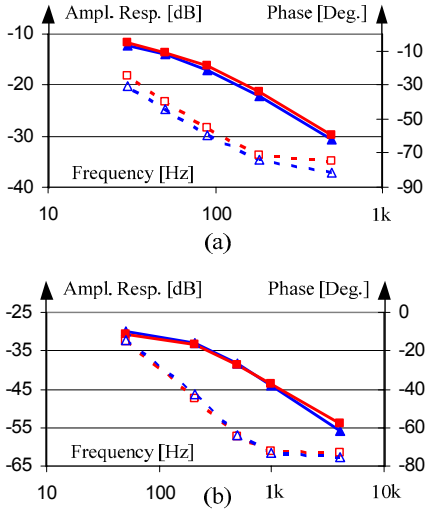

Figure 19. Small signal, control to output responses {$v_o/f_s(f)$} of the inverting 1:1 SCC, obtained by the model (AC analysis) and experimentally: (a) CC mode, (b) PC mode; Triangles – Average model simulation results; Squares - Experimental results; Solid traces – Amplitude response; Dashed traces – Phase response.

as first order networks. This assumption leads to the closed form solution for R_e (6). However, as already demonstrated [10, 15], popular SCC topologies, which do not conform to the first order requirement, can still be approximated as one, and modeled by proposed approach. This is especially true in systems that include capacitors of the same capacitance and ESR values and switches with identical $R_{ds(on)}$.

Although this paper emphasized the simulation approach which is the fastest way for getting final numerical results, the proposed average model is by no means restricted to this type of analysis. Once the average equivalent circuit is formulated; it can be analyzed symbolically to derive the relationships of interest. This was demonstrated for the small signal audio susceptibility transfer function (10). In this case, when the frequency and duty cycle are kept constant, the average equivalent circuit is linear and can be probed by any analytical technique. However, considering the non-linearity of (6) derivation of analytical expression for the control to output transfer functions would require the use of some linearization techniques.

A major conclusion that emerges from the results of this study is that the average behavior of SCC systems (both static and dynamic) is a function of the equivalent resistances (R_{ei}) rather than the physical resistances of the SCC (ESR and $R_{ds(on)}$). In fact, based on (6) when $\beta_i >> 1$ ($T_i >> R_iC_i$, CC mode)

$$R_{e_i}\Big|_{\beta_i >> 1} = \frac{1}{2f_sC_i} \qquad (20)$$

and the SCC behavior will be independent of the resistive elements.

On the other hand, when $\beta_i << 1$ ($T_i << R_iC_i$, NC mode) the limiting value of R_{ei} will be according to (21),

$$R_{e_i}\Big|_{\beta_i << 1} = \frac{R_i}{f_s T_i} \qquad (21)$$

and the equivalent resistance is only a function of the resistive elements, independent of the switching frequency.

The above observation can explain the experimental and model derived results obtained for the small-signal frequency-to-output response. As evident from the plots of Fig. 19, this response is larger in amplitude for the CC case (Fig. 19a) than for the PC case (Fig. 19b). This is due to the fact that in the CC case the equivalent resistances are a function of f_s (21) (Fig. 4), and hence an excitation in the switching frequency will cause a marked effect on R_e and hence on the output voltage. In the NC case the equivalent resistance is independent of f_s (21) (Fig. 4), and consequently the control by frequency variation will not yield any change in the output. The PC case (Fig. 19b), which is in-between the CC and the NC cases (Fig. 4), will be affected by the frequency control but to a less degree than the case of CC. For NC operation, duty cycle control would be a good choice [24] since the equivalent resistance is a strong function of the subcircuits' switch duration T_i (21).

It is believed that the proposed intuitive and straightforward modeling methodology could be helpful to researchers, design engineers, and for educational purposes. The suggested approach can be used to gain a better understanding of SCC and charge pumps behavior, to optimize the circuit and to design the control.

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