Current Sourcing ZCS Magnetron Driver for Low Input Voltage Applications

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Abstract **- The use of topologies that have an output current sourcing behavior could be advantageous when driving constant voltage loads that call for the stabilization of the output current rather than output voltage. The load characteristic of the magnetron considered in this study can be modeled as a voltage source of about 3.9kV with a relatively small internal resistance of about 1.5kOhm that needs to be driven by a current of about 300mA. This study proposes a one-stage, zero current switched, high voltage gain, and current sourcing converter, to drive such a load. The topology is based on the parallel resonant converter but includes blocking diodes at the input bridge to assist the soft switching operation. The theoretical analyses were verified by simulations and experimentally on a 1.3kW magnetron driver which was fed from a low voltage source in the range of 20V to 32V. The circuit was controlled by dsPIC30F2020 (Microchip, USA) in closed loop.**

I. Introduction

Various loads, such as high and low pressure discharge lamps, the power line (in grid connected inverters) and magnetrons, have a constant voltage or "voltage source"-like characteristic. For example, the load characteristic of the magnetron considered in this study (Fig. 1) shows that for a current range of 20mA to 350mA, the voltage across the magnetron varies by only 13%. This implies that the magnetron can be modeled as a voltage source of about 3.9kV with a relatively small internal resistance of about 1.5kOhm. The objective of this study was to develop a low input voltage (24V), one stage driver for this class of high power magnetrons (1.3kW).

The optimal drive for constant voltage loads is a current sourcing converter that will help sustain power regulation and dynamic stability. It has been shown that converters with triangular shaped inductor current can be considered to have a current sourcing behavior while operating under ZVS [1-3].

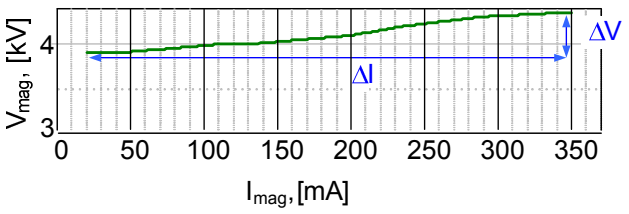

Figure 1. Output characteristic of magnetron.

However, ZVS has a number of drawbacks in high power, low input voltage (and hence very high primary current) applications. In such cases, the current fed back to the bus at the commutation instance will cause considerable ringing due to the parasitics, increasing EMI emission and power loss. Another drawback is the fact that these converters are turned off under extremely high currents which again increases EMI emission and power loss. Other approaches based on series resonant converters [4-9] also have a number of deficiencies in the application domain considered here. A major one is the fact that they require a series resonant capacitor that needs to carry the large primary current. Consequently, these capacitors need to have extremely low ESR values which are just about beyond the specifications of present day commercially available capacitors. Furthermore, true soft switching in series resonant converters is normally achieved at the expense of high peak and rms currents [7].

Considering the above, this study explored the possibility of applying a parallel resonant converter that does not require a series capacitor, has a current sourcing output characteristic and runs under ZCS conditions.

II. Analysis of Proposed Topology

Typical waveforms of the traditional parallel resonant converter [10-13] with a parallel capacitor located at the secondary side of the isolating transformer (Fig. 2), a reflected voltage V_{refl} that is higher than the input voltage V_{in} and a voltage doubler at the output, are depicted in Fig. 3. Output power is controlled by varying the switching frequency f_s. In the conventional operation of this converter, the turn off of transistors Q4 and Q1 at time instance t_2 (point "A", Fig. 3) occurs at non-zero current.

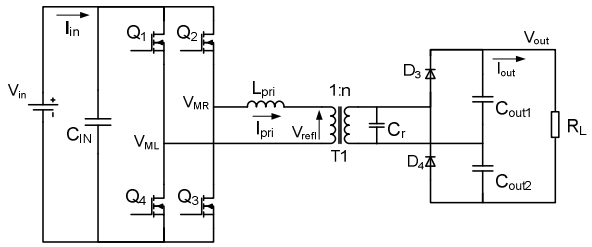

Figure 2. Parallel resonant converter with output voltage doubler.

In high input current applications, this non-zero current turn off, posses a severe problem due to the switching losses and the injection of the high current back to the bus. This could be circumvented by operating at the matching switching frequency that will reduce the inductor current at t_2 to zero. However, this is possible for one power point only while for other power levels, non-zero current switching will still persist.

To preserve true soft switching at turn off while still enabling output power control, it is proposed to introduce two series diodes as shown in Fig. 4. These would allow the inductor current to drop to zero while blocking the discharge current of the resonant capacitor C_r.

The key waveforms of this topology are sketched in Fig. 5. The switching frequency, f_s, at nominal (maximum) power is denoted f_{cr}. At power levels other than nominal power, the switching frequency is always below f_{cr}. It is further assumed that the forward voltage drop of the diodes D_1 and D_2 is much lower than the input voltage.

For this topology, four operational stages can be identified (Fig. 5):

a: time period t_0-t_1 (resonant phase).

Q2, Q4 and D1 are turned on under ZCS condition (at t_0) and the voltage across capacitor C_r charges from $-V_{out}/2$ to $V_{out}/2$ by the sinusoidal shaped inductor current due to the resonance of L_r and C_r.

The inductor current and the capacitor voltage are given as follows:

$$I_L^*(t) = (1+k)\sin(2\pi f_r t) \qquad (1)$$

$$V_c^*(t) = n[1-(1+k)\cos(2\pi f_r t)] \qquad (2)$$

where $I_L^*(t) = I_L^*(t)/(V_{in}/Z_R)$ is the normalized inductor current, and Z_r represents the characteristic impedance of the resonant network defined as:

$$Z_R = \sqrt{\frac{L_r}{n^2 C_r}} \qquad (3)$$

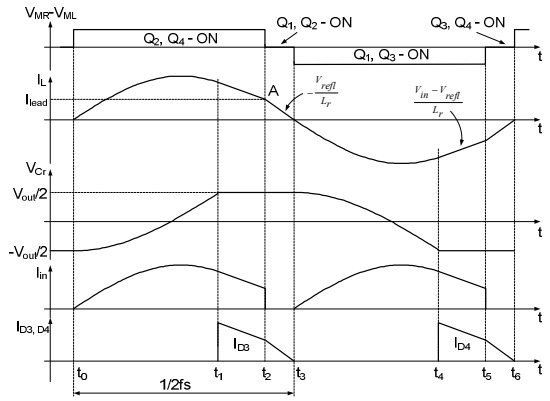

Figure 3. Key waveforms of the converter of Fig. 2

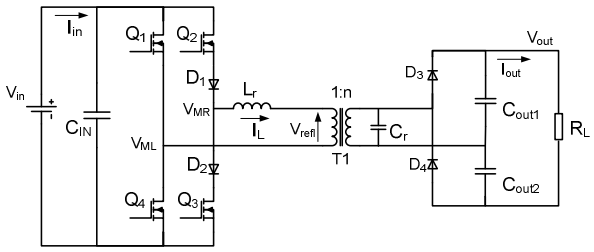

Figure 4. Proposed topology with input diodes.

$V_c^*(t) = V_c(t)/V_{in}$ is the normalized capacitor voltage, $k = V_{out}^*/2n$, $V_{out}^* = V_{out}/V_{in}$ is normalized output voltage, and $f_r = \dfrac{1}{2\pi\sqrt{L_r C_r}}$.

This time interval ends when the voltage across the capacitor reaches half of the output voltage (in the voltage doubler configuration). At this point in time, the relevant output diode starts to conduct (diode D_3 in Fig. 4), clamping the voltage across the capacitor C_r to $V_{out}/2$.

The time t_1 can be calculated by substituting $V_c^*(t_1) = V_{out}^*/2 = kn$ into (2):

$$t_1 = \frac{1}{2\pi f_r}\arccos\left(\frac{1-k}{1+k}\right) \qquad (4)$$

The normalized inductor current at the end of this interval, I_{t1}^*, will be found by substituting (4) into (2):

$$I_{t1}^* = (1+k)\sin\left(\arccos\frac{1-k}{1+k}\right) = 2\sqrt{k} \qquad (5)$$

where $I_{t1}^* = I_{t1}/(V_{in}/Z_R)$

b. time interval t_1-t_2:

During this time interval the voltage across the capacitor is clamped to $V_{out}/2$, output diode D_3 conducts and current is

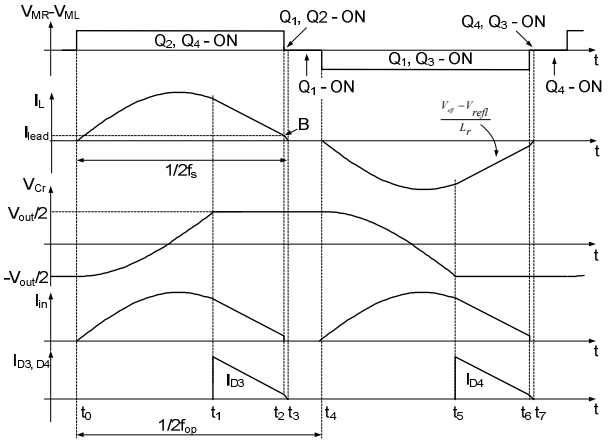

Figure 5. Key waveforms of the proposed converter.

delivered to the load (I_{D3} in Fig. 5). Since the inductor is now clamped to constant voltages (V_{in} and $V_{out}/2n$), its current drops linearly. During this time interval, I_L, can be expressed as follows:

$$I_L^*(t) = I_{t1}^* - \omega_r(k-1)(t-t_1) = 2\sqrt{k} - \omega_r(k-1)(t-t_1) \quad (6)$$

where $\omega_r = 1/\sqrt{L_r \cdot n^2 C_r}$

After the inductor current drops to zero, transistor Q4 can be turned off at zero current. If some residual current, I_{lead}, is allowed (point "B", Fig. 5), it will maintain zero voltage switching at turn on of transistor Q1.

The duration of this time interval can be calculated from (2) by setting $I_L^*(t_2) = 0$ (I_{lead} assumed to be negligibly small):

$$t_2 - t_1 = \frac{2}{\omega_r}\frac{\sqrt{k}}{k-1} \quad (7)$$

c. time interval t_2-t_3:

During this time interval the residual current of the inductor, if allowed, flows via D1, Q2 and recharges the body capacitors of Q1, Q4 (not shown in Fig. 5). Assuming that enough energy is stored in the inductor at the beginning of this time interval (depends on I_{lead}), the voltage across the transistor Q1 will drop to zero and the body diode will conduct, so it can be turned on under zero current and zero voltage at the next switching half cycle.

d. time interval t_3-t_4:

Transistor Q2 is turned off under zero current. The inductor current is zero during this time interval.

Based on the fact that the current is outputted to the load only during t_1-t_2 and assuming that I_{lead} is negligibly small, the normalized average load current can be derived from (5) and (7) to be:

$$I_{avout}^* = \frac{1}{2n}\left[\frac{I_{t1}^*}{2}\cdot(t_2-t_1)\cdot 2f_{op}\right] = \frac{k}{\pi n(k-1)}\frac{f_{op}}{f_r} \quad (8)$$

where $I_{avout}^*(t) = I_{avout}^*/(V_{in}/Z_R)$, f_{op} is operating frequency.

And the output power delivered to the load is:

$$P_{out}^* = I_{avout}^* 2kn = \frac{2k^2}{\pi(k-1)}\frac{f_{op}}{f_r}, \quad P_{out}^* = \frac{P_{out}}{V_{in}^2/Z_r},\ f_r = 1/2\pi\sqrt{L_r \cdot n^2 C_r} \quad (9)$$

To find the incremental output impedance of the converter, R_o, one can take the derivative of $I_{av\ out}$ with respect to V_{out}:

$$\frac{1}{R_o} = \frac{\partial I_{out}}{\partial V_{out}} = \frac{1}{Z_r}\frac{\partial I_{out}^*}{\partial V_{out}^*} = \frac{1}{2n\cdot Z_r}\frac{\partial I_{out}^*}{\partial k} \quad (10)$$

and $\frac{\partial I_{out}^*}{\partial k}$ can be found from (8):

$$\frac{\partial I_{out}^*}{\partial k} = \frac{1}{\pi n(k-1)^2}\frac{f_s}{f_r} \quad (11)$$

Substituting into (10) and rearranging for R_o yields

$$R_o = -2\pi \cdot Z_r \cdot n^2(k-1)^2\frac{f_r}{f_{op}} \quad (12)$$

IV. Analysis of the Proposed Converter with Resistive Load

When operated with a resistive load, the output voltage of this converter will depend on the value of the load resistance R_L. We assume that the converter is running at nominal power, i.e., $f_s = f_{cr}$. The inductor and output diodes' current under this assumption are sketched in Fig. 6.

Half a switching period in this case can be found as a sum of the two time intervals t_0–t_1 and t_1–t_2 (Fig. 6). Taking into account (3) and (7) and rearranging for f_s one gets

$$f_s = f_{cr} = \frac{1}{\frac{2}{\omega_r}\left(\arccos\frac{1-k}{1+k} + \frac{2\sqrt{k}}{k-1}\right)} \quad (13)$$

In the case of a resistive load the output current is

$$I_{avout} = \frac{V_{out}}{R_L} \quad (14)$$

By defining the normalized load of the converter as

$$R_{ch} \equiv \frac{R_L}{Z_r} \quad (15)$$

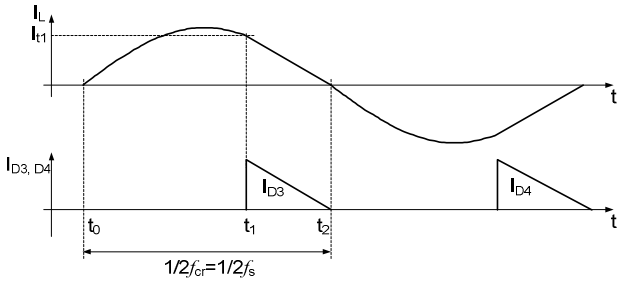

Figure 6. Inductor and output diode current of the converter with series diodes while operating at $f_s = f_{cr}$.

(14) can be rewritten as follows:

$$I^*_{av\,out} = \frac{V^*_{out}}{R_{ch}} \tag{16}$$

Equating (14) and (8), substituting (13), and rearranging yields

$$\arccos\left(\frac{1-k}{1+k}\right) = \frac{R_{ch}}{2}\frac{1}{k-1} - \frac{2\sqrt{k}}{k-1} \tag{17}$$

The left side of (17) can be approximated by a Taylor series expansion. Only the two first terms will be kept, i.e.,

$$\arccos\left(\frac{1-k}{1+k}\right) \approx \frac{\pi}{2} - \frac{1-k}{1+k} \tag{18}$$

Substituting this into (17) and rearranging yields

$$R_{ch} = \left(4\sqrt{k} + \pi k + \frac{2(k-1)^2}{k+1} - \pi\right)n^2 \tag{19}$$

By further rearranging, (19) can be rewritten as

$$\begin{aligned}&(2+\pi)k^2n^2 + 4n^2k\sqrt{k} - \left(4n^2 + R_{ch}\right)\cdot k + \\ &+ 4n^2\sqrt{k} + (2-\pi)n^2 - R_{ch} = 0\end{aligned} \tag{20}$$

Solving (20) gives the gain ratio, k. If k is much larger than unity, the reactive current in the primary will be relatively high. This is because the voltage across the resonant capacitor, reflected to the primary of the transformer, will be high, and hence one will need to transfer a relatively high charge to this capacitor, to recharge it in the beginning of every half switching cycle. Consequently, for practical designs, k will usually not be much larger than one. Therefore, (20) can be approximated by a function of lower order in the proximity of 1. This was accomplished by using the Taylor series expansion around $k = 1$. The resulting function is:

$$(3+\pi)k^2n^2 + \left(2n^2 - R_{ch}\right)\cdot k + (3-\pi)n^2 - R_{ch} = 0 \tag{21}$$

Solving it for k yields:

$$k = \frac{1}{2n^2(3+\pi)}\times \left[R_{ch} - 2n^2 + \sqrt{\left(R_{ch} - 2n^2\right)^2 + 4n^2(3+\pi)\left(R_{ch} + (\pi-3)n^2\right)}\right] \tag{22}$$

Considering $k = V^*_{out}/2n$, we get

$$V^*_{out} = \frac{1}{(3+\pi)n}\times \left[R_{ch} - 2n^2 + \sqrt{\left(R_{ch} - 2n^2\right)^2 + 4n^2(3+\pi)\left(R_{ch} + (\pi-3)n^2\right)}\right] \tag{23}$$

The last expression gives the normalized output voltage (gain) of the converter for the case of nominal (maximum power). This equation has been derived under the assumption that at nominal power the converter is running at the critical switching frequency f_{cr}. For power levels other that nominal, the switching frequency, f_s, will always be lower than f_{cr}.

It follows from (23) that for a given load R_L, the required voltage gain can be obtained by adjusting either the transformer ratio n or the characteristic impedance Z_r of the resonant tank. To increase the gain of the converter one should either decrease the transformer ratio n or lower the characteristic impedance of the resonant tank. The considerations for choosing the optimum combination of Z_r and n are discussed below.

V. Losses

Since all the switches are turned on and off under zero current conditions, the switching losses will be negligibly small. The conduction losses of the input diodes D_1, D_2 are proportional to the input average current and consequently dictated by the power level and the input voltage. This is because in every switching half cycle one of these diodes is on and connected in series to the input voltage.

The conduction losses of the transistors Q_1–Q_4 are function of the rms current in the input side of the converter. The maximum rms current is expected at nominal power when the switching frequency f_s is set to f_{cr}. This current was found by using (2), (4), (5), (7) and (13) and assuming the inductor current shape shown in Fig. 6. It was further assumed that the voltage drop of the diodes D_1, D_2 is negligibly small as compared to the input voltage. Under these assumptions the normalized rms current was found to be

$$I^*_{rms\,norm} = (1+k)\sqrt{\frac{\frac{1}{2}\arccos\frac{1-k}{1+k} + \frac{\pi\sqrt{k}}{3}\times \frac{3k^2+2k+3}{(k+1)^2}}{\left[(k-1)\arccos\frac{1-k}{1+k} + 2\sqrt{k}\right]}} \tag{24}$$

where $I^*_{rms\,norm} = \dfrac{I_{rms}}{V_{in}/Z_r}$.

Under the same assumptions, the normalized output average current reflected to the primary side of the transformer can be expressed as a function of k as follows:

$$I^*_{av\,norm} = k\frac{2}{(k-1)\arccos\frac{1-k}{1+k} + 2\sqrt{k}} \tag{25}$$

where $I^*_{av\,norm} = \dfrac{I_{av}}{V_{in}/Z_r}$.

VI. PARAMETER OPTIMIZATION

For every practical design one needs to select the optimal combination of the resonant inductor, capacitor, and transformer ratio. One possible goal of the optimization may be keeping the losses as low as possible.

To compare the losses at various operating conditions, the ratio of the output average current reflected to the primary side of the transformer over the rms inductor current, I_{av}/I_{rms}, was examined (I_{av}/I_{rms} plot in Fig. 7). For a given load, this ratio is proportional to the efficiency since a higher ratio means a lower rms current and consequently lower conduction losses of the main switches, and lower copper losses of the main transformer. Putting this in other words, the design goal needs to be to operate the system at as high an I_{av}/I_{rms} ratio as possible. According to I_{av}/I_{rms} plot in Fig. 7, a higher ratio is obtained at lower k.

Next, the normalized critical switching frequency is defined as:

$$f_{norm} = \frac{f_{cr}}{f_r} = \frac{\pi}{\arccos\frac{1-k}{1+k} + \frac{2\sqrt{k}}{k-1}} \qquad (26)$$

where f_{cr} is defined as in (13) and $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$,

The expression for normalized power (9) will be rewritten by setting f_s=f_{cr} and substituting (13) into it:

$$P_{norm} = P^*_{out}\Big|_{f_s=f_{cr}} = \frac{2k^2}{(k-1)\arccos\frac{1-k}{1+k} + 2\sqrt{k}} \qquad (27)$$

Fig. 7 combines I_{av}/I_{rms} plot with plots of (26) and (27):

Moving in the direction of lower k (Fig. 7) decreases both the normalized power and the normalized frequency. Lower normalized power means that, for a given input voltage and power, one needs to select the resonant network with lower characteristic impedance Z_r. Lower normalized frequency, in turn, means that for some predefined critical (maximum) switching frequency the resonant frequency f_r needs to be higher. Decreasing Z_r concurrently with increasing f_r is only possible by reducing the resonant inductance L_r. Conversely, higher k ratios will call for larger resonance inductors.

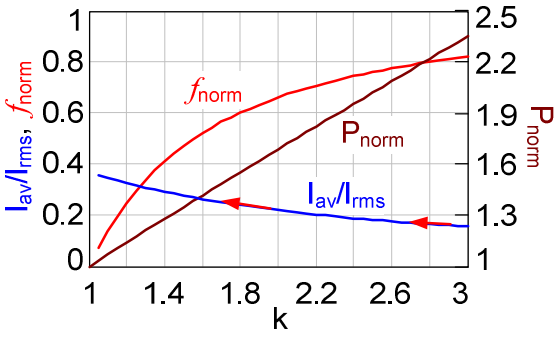

Figure 7. Parametric plots of the converter.

It follows from Fig. 7 that to obtain higher I_{av}/I_{rms} and consequently higher efficiency, one needs to select as low a k as possible. The procedure for selecting optimum k value is discussed in the next section.

VII. DESIGN CONSIDERATIONS FOR THE ISOLATION TRANSFORMER

To reduce the physical dimensions of the converter it would be advantageous to use the leakage inductance of the transformer as a resonance inductor [14-17]. Leakage inductance of the transformer seen at the primary can be estimated by the following equation [18]:

$$L_{lkg} = \frac{\mu_0 \cdot N_1^2 \cdot ATL}{a}\left[\frac{b_1 + b_2}{3} + c\right] \qquad (28)$$

where L_{lkg} is the leakage inductance of the isolation transformer (reflected to the primary side), μ_0 is the air permeability constant ($4\pi \cdot 10^{-7} H/m$), N_1 is the number of turns in the primary winding, ATL is the average length of a turn, a is the winding height, b_1 and b_2 are the thicknesses of the primary and secondary windings, respectively, and c is the distance between the primary and the secondary windings (i.e., the thickness of the insulation layer(s)).

Examination of (28) reveals that the resulting leakage inductance, reflected to the primary, depends on the core dimensions and number of turns of the primary. For a given effective core area, the number of turns of the transformer's secondary, N_2, will be dictated by the maximum output voltage of the converter and the minimum operating frequency. The number of turns of the primary, N_1, will depend on the turn ratio ($n = V_o / 2kV_{in}$) which in turn is a function of the k ratio. This implies that the leakage inductance depends on k and that a large leakage inductance can be obtained by increasing k. However, k is a pivotal parameter that has many effects on the design of proposed converter. As pointed out earlier and depicted in Fig. 7, large k increases the rms current and hence increases the losses. Also, the value of k dictates the required resonance inductance for a given design. This can be seen by expressing the resonance inductance as the ratio of Z_r/ω_r which can then be calculated from (26) and (27), assuming $Z_r = P_{norm}\frac{V_{in}^2}{P_{out}}$ (see (9)). This calculation reveals that a larger k will dictate a larger resonance inductance. Hence, a larger k implies a large leakage inductance but at the same time the required resonance inductance (that is to be realized by the leakage inductance) is increasing. These trends are depicted in Fig. 8 that plots the resonance inductance and the leakage inductances for different k values. The plot was drawn for Vin=24V, Pout=1kW,

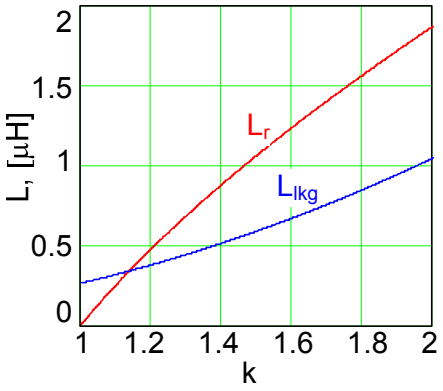

Figure 8. Leakage and resonance inductances for different k's.

switching frequency of 55kHz, and assuming two E65 cores that are attached together.

It appears from Fig. 8 that for this particular case, $k \approx 1.14$ is an optimal choice since the obtained leakage inductance meets the resonance inductance requirement and the k is not too high so the loss penalty is reasonable (Fig. 7). Like most, if not all, design cases the transformer design for proposed converter is subject to conflicting requirements and calls for a compromise between opposing objective.

VII. Experimental

The behavior of the proposed converter was tested experimentally on a 1.3 kW prototype that was built according to the topology shown in Fig. 4. The transformer ratio n was set to 48. The primary winding of the transformer had four turns. The leakage of the transformer T1, used as a main inductor L_r, was about 0.8 μH. The resonant capacitor C_r was chosen to be 2.2 nF, and the output capacitors C_{out1} and C_{out2} were 0.5 μF each. The input voltage range was from 22 V up to 32 V and the switching frequency varied from about 30 kHz at the maximum input voltage up to about 55 kHz when the input voltage was at its low end.

The input bridge consisted of IRFP4368 (International Rectifiers, USA) MOSFETs with typical Rdson of 1.46 mΩ@250^{0}C. The input diodes D1, D2 were DSS 2x160-01A (IXYS, USA) (each 2 Schottky diodes that were connected in parallel). The output diodes D3, D4 were HVUFS7500 (HV Components/CKE, USA). The circuit was controlled by dsPIC30F2020 (Microchip, USA). The experiments were carried out with a resistive load and with a magnetron.

Fig. 9 shows the experimental results measured with a resistive load of about 16 kΩ. The input voltage was set to 21.5V, the switching frequency to 45kHz. Output voltage was 4.3 kV and the power measured at the output was 1150W. The efficiency was as high as 89%.

Fig. 10 shows typical experimental results with a magnetron at nominal output power. The input voltage was 23V and the output was about 4.3kV. In this experiment the

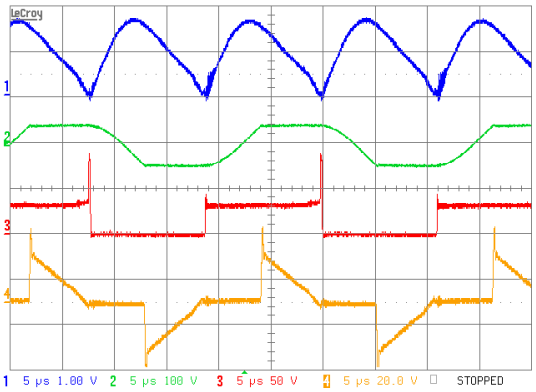

Figure 9. Experimental results. Resistive load (~16kΩ). Upper trace: rectified inductor current 100A/div. Second trace from the top: transformer's primary voltage 100 V/div. Third trace from the top: drain voltage of transistor Q3, 50 V/div. Lower trace: I_{D3}–I_{D4} (see Fig. 4) 1 A/div. Horizontal scale: 5 μs/div.

magnetron was attached to a waveguide that was terminated by a heatsink. The microwave power was measured by means of diode detector 423B (Agilent, USA). The electrical efficiency at nominal output power (1.3kW), measured at different operating points varied from 85% at low input voltage (22 V) up to 88% at Vin=28V.

V. Discussion and Conclusions

This paper describes a one stage, high voltage gain, current sourcing converter topology that was implemented in the design of a battery operated (24V) 1.3kW magnetron driver. The converter does not require a series capacitor which makes possible the operation at high input currents (100Arms and above). The output current was regulated by varying the switching frequency. The experimental circuit can be fed from a low input voltage source (such as a battery) in the range of 20V to 32V while maintaining a high voltage (about 4.3kV) at the output with a regulated current of about 300mA.

The analytical results of this study were verified by simulations and experimental results. All are in good agreement with theoretical predictions.

The overall efficiency measured for the case of V_{in}=22V, V_{out}=4.3kV at P_{out}=1.3kW was about 85%. The main losses were estimated to be: conduction losses of the diodes (3.5% of input power), transformer losses (2%), PCB and wiring losses (4.5%), MOSFETs losses (3%), input bus capacitors (1%), and output diodes (1%). The reason for the high PCB conduction loss was the fact that the copper gauge was 3Oz while only two layers were used to carry the current, and that the small packages of the MOSFETs (TO247) dictated a layout with sections of narrow traces.

The major advantages of the proposed topology and mode of operation are soft switching and output current sourcing. All the switches and input diodes are operated at ZCS at turn on and turn off while the output diodes (high voltage low current) are turned on under ZVS and turned

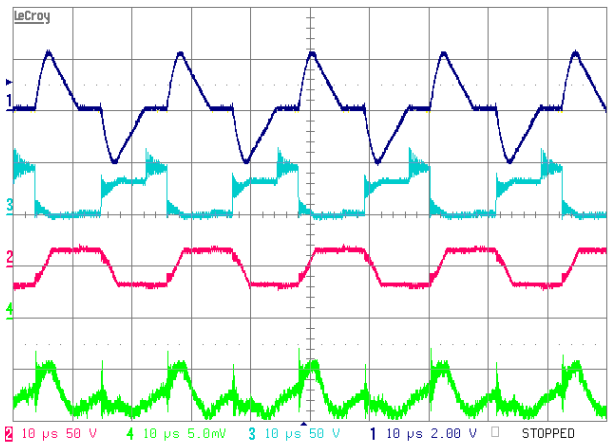

Figure 10. Typical experimental results. Loaded by magnetron. Upper trace: Inductor current 200A/div; Second trace from top: V_{MR} (Fig. 4) 50V/div; Third trace from top: Transformer primary voltage 100V/div; Lower trace: Microwave power 880W/div; Horizontal scale: 10us/div.

off under ZCS. The ZCS operation at the primary and the smooth, sinusoidal-like, current is extremely beneficial in high primary current cases since it reduces the ringing due to the parasitic inductances of the power elements and the wiring. The inherent current sourcing at the output of the proposed converter eases the current control task by reducing the sensitivity of the output current to source and load voltage variations. This reduced sensitivity of the output current can be explained by relatively high output incremental resistance (eq. (12)). For example, in the converter under study the open loop incremental output resistance is in the range of several kilo ohms. In the conventional (e.g. PWM) converter the open loop output resistance will be determined by the parasitic resistances of the inductor and the wirings and consequently will be in the order of several ohms or even less. This high output resistance attribute is especially important in the present Magnetron driver application considering the low incremental resistance of the Magnetron. The high output impedance is a direct consequence of the fact that the converter under study exhibits a current sourcing behavior at the output.

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