Optimal Switch Resistances in Switched Capacitor Converters

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***Abstract*— Switched Capacitor Converters (SCC) losses are analyzed and the rules for the selection of SCC parameters (such as switch resistances, capacitors values and switching frequency) to meet specific efficiency requirements, are developed. This is done by first applying an advanced methodology for calculating the equivalent resistance (R_e) of the SCC in general. The impact of each of the parameters on the equivalent resistance is then analyzed and the results are used to develop design rules to meet efficiency targets as defined. The paper clarifies an apparent paradox related to the role of switch resistances in SCC which seem not to affect the efficiency considering the fact that the efficiency is determined by the SCC voltage transfer ratio. The results of this study could help designers of SCC to select optimal values of the SCC parameters that will meet specifications. The analysis developed in this study can also assist users of SCC to better understand the characteristics and limitations of commercially available SCC.**

I. Introduction

Switched capacitor converters (SCC), also known as a charge pumps, became very popular during the last decade, due to their IC compatibility, relative high efficiency in open loop high gain applications and the absence of magnetic components that helps lower EMI. One of the main dilemmas in the design of SCC is the size of the active switches, which of course affects the cost of the converter. The classical approach of presenting SCC losses is to express their efficiency as a function of the voltage transfer ratio independent of switch resistances [1]:

$$\eta = \frac{V_o}{M \cdot V_{in}} = \frac{V_o}{V_T} \quad (1)$$

where V_T - is the target voltage, or open circuit SC converter output voltage and M - is the conversion ratio.

Expression (1) might give the impression that SCC can operate with any switch resistance, contrary to the common sense feeling which predicts lower efficiency when the switch resistances are large. This apparent paradox is examined in this paper by theoretical analysis, simulation and experimental results, which delineate the role of switch resistance in SCC operation. An analytical method that assists in the selection of optimal switch resistances for SCC is also presented. The proposed approach employs generic modeling methodology as developed in [2] and is related to the work of [3, 4]. The method enables optimal SCC parameter optimization including switching frequency, capacitors sizes and switch resistances. The proposed approach can handle two and multiphase SCC, takes into account different capacitances and/or switch resistances which are operational in each switching phase and considers asymmetric phase timing. The proposed analysis method is demonstrated on two representative SCC and shown to be robust and reliable.

II. Conduction losses in SC converter

A SCC can be described as a two port networks in which the power components are switches, capacitors and resistances (Fig.1). It has been previously shown that any SCC can be modeled, for DC operation and loss calculations, as an equivalent voltage source, defined as the target voltage V_T, connected in series with the equivalent system resistor (R_e) that represents the internal power loss (Fig. 2). R_L is the load, C_o is the output capacitor and I_o is the output current. The calculation of R_e is carried out by dividing the SCC circuits into sub circuits according to the switching phases. Next, the expression for losses is found for each sub circuit as a function of the average current through the capacitor. Since the average current through the capacitors is linearly proportional to the average output current, the losses can be represented as a series resistor connected to the load. Repeating the calculation

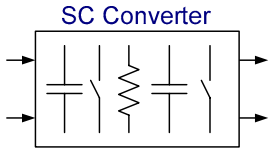

Fig. 1: SC converter components.

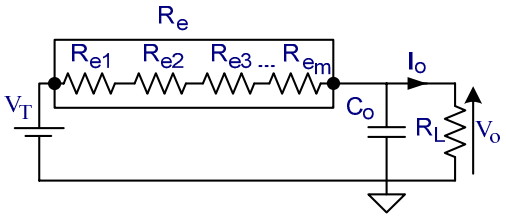

Fig 2: SC converter equivalent circuit.

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for each switching phase, these partial equivalent resistances for "m" switching phases, R_{e1}, R_{e2} … R_{em}, are then connected in series to form the total equivalent resistance R_e, of the converter Fig. 2.

$$R_e = \sum_m \left(R_{e_i}\right) \tag{2}$$

A more detailed discussion of the procedure for extracting R_e is given in [2].

The general form of the R_{ei} expression, assuming equal time intervals for each i-th switching phase out of "m" possible phases, is:

$$R_{e_i} = k_i^2 \cdot \frac{1}{2 f_s C_i} \cdot \coth\left(\frac{\theta_i}{2}\right) \qquad \theta_i = \frac{1}{n \cdot f_s \cdot R_i C_i} \qquad \frac{1}{n \cdot f_s} = t_i \tag{3}$$

where k_i is the ratio between the average capacitor current and the average output current, f_s is the switching frequency, t_i – is the time interval for the phase i, C_i is the total capacitance of the phase i, and R_i is the total resistance of the phase i, which includes the ESRs of the capacitors and the resistances of the switches that conduct during the i-th phase. According to (3) R_e is inversely proportional to the product f_sC. This is due to the fact that higher frequency and/or larger capacitor, result in lower voltage differences across the charging/discharging capacitor, and thus lower the converter's losses. Fig. 3 presents the normalized equivalent resistance of a single charge or discharge phase, derived from (3) and normalized by the factor $1/(n \cdot R_i)$ (4). The curve can be approximated by two linear sections (marked red in Fig. 3), one for high thetas and one for low thetas. For high thetas, one over f_sC is a dominant term forcing the equivalent resistance to rise linearly, while for low thetas R_e is maintained constant due to the convergence of (4) to a constant value as theta approaches zero.

$$R^*_{e_i} = \frac{R_{e_i}}{n \cdot R_i} \qquad R^*_{ei} = \frac{\theta_i}{2} \cdot \coth\left(\frac{\theta_i}{2}\right) \tag{4}$$

III. SC Parameters Optimization Method

SCC can be operated in a regulated or unregulated mode. In the case of an unregulated converter R_e will be determined by the required efficiency of the SCC. In this case the lower R_e the higher will be the efficiency since the R_e forms a voltage divider with the load (Fig. 2) and the efficiency will be:

$$\eta = \frac{R_L}{R_L + R_e} \tag{5}$$

In the case of a regulated SCC, regulation is achieved by increasing R_e. The limiting case is when the converter is supposed to sustain a voltage equal to V_T which can be accomplished only if R_e is equal to zero. In some commercial SCC this limitation is overcome by having multiple target voltages to cover a wide input to output voltage range at a higher efficiency. In such cases, the change from one target voltage to another is dependent on R_e. The change is carried

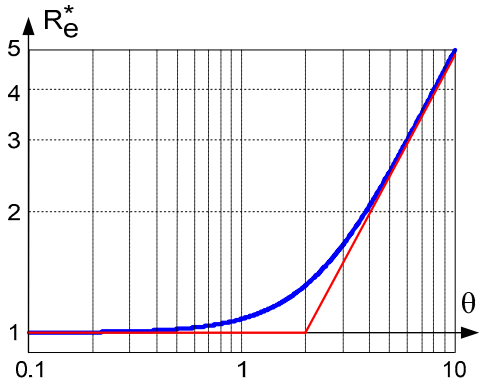

Fig. 3: Normalized equivalent resistance.

out when the SCC cannot sustain any more the required output voltage and to remedy this, the SCC switches to a higher target voltage. This of course will increase the loss according to (1). Hence, in the regulated case, R_e determines in fact the maximum efficiency that the SCC will have over the input output voltage ratio range. It is thus evident the R_e will be set in each case by the required specifications and desired performance of the SCC. Once the R_e is set, the required switch resistance can be determined as discussed in the followings.

As an example, we consider a case of a divide by 2 SCC (Fig. 4) and assume that the required specifications are according to Table I. The worst case is clearly when the input voltage is at its minimum (4V) and the output power is at its maximum. For this case V_T is 2V while the required output is 1.8V and the maximum current is 550mA. This implies that R_e should not exceed 0.36 Ohm (Fig. 5). Assuming equal time intervals for each sub-circuit, and n = 2 sub-circuits (charge and discharge).

$$R_e = \sum_i \left(R_{e_i}\right) = \frac{1}{4} \cdot \frac{1}{f_s C} \cdot \coth\left(\frac{\theta}{2}\right) \qquad \theta = \frac{1}{2 f_s C \cdot (ESR + 2R_s)} \tag{6}$$

This relationship is plotted in Fig. 6 as a function of R_i - the total resistance of phase i, (ESR+2R_s in our case) with (f_sC) as a parameter. By drawing a horizontal line at the required value of R_e (0.36 in this example) one can identify the various combinations of (f_sC) and R_i that are possible. For example, selecting (f_sC) product of 0.7 will force to use switches of maximum 0.17 Ω. On the other hand, selecting larger capacitor or higher frequency and enlarging (f_sC) product will permit the use of smaller and hence lower cost switches with higher resistance of around 0.36 Ω.

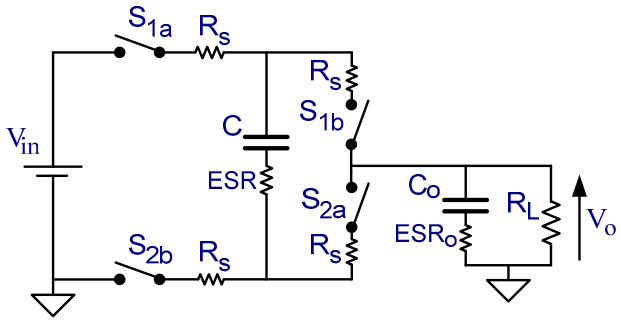

Fig. 4: Divide by two SCC.

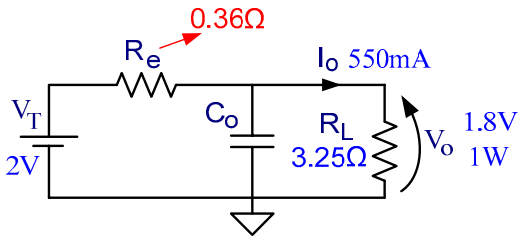

Fig. 5: Equivalent circuit of divide by two SCC.

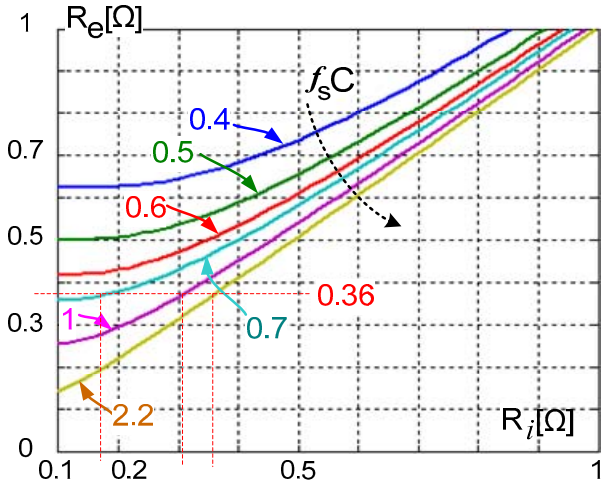

Fig. 6: R_e as a function of R_i with (f_sC) as a parameter.

IV. Simulation & Experimental

To illustrate the proposed design method, an inverting SCC is considered (Fig. 7) with target requirements as summarized in Table II. For this topology k = 1, and assuming equal charge and discharge time periods ($t_1 = t_2 = 1/2f_s$), the expression for R_e takes the form:

$$R_e = \frac{1}{2f_s \cdot C_1} \cdot \left[\coth\left(\frac{\beta_A}{2}\right) + \left(\frac{C_1 + C_o}{C_o}\right) \cdot \coth\left(\frac{\beta_B}{2}\right) \right] \quad (7)$$

$$\beta_A = \frac{t_1}{(R_{s1} + ESR_1)C_1} \qquad \beta_B = \frac{t_2}{(R_{s2} + ESR_1 + ESR_o)\left(\frac{C_1 \cdot C_o}{C_1 + C_o}\right)}$$

The required minimum equivalent resistance value, per the system requirements as summarized in Table II, was calculated by (7) and by taking into account diode voltage drop [2], to be 1.92 Ω.

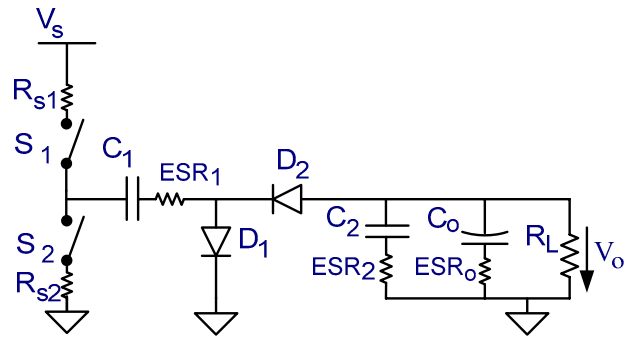

Fig. 7: Inverter schematics.

TABLE I
DESIGN EXAMPLE: SYSTEM REQUIREMENTS

Input voltage range V_{in}	4 to 5.5 VDC
Output voltage (minimum) V_O	1.8 VDC
Nominal output Power	1 W
Switching frequency range	50 to 150 kHz
Switching capacitor range C	0.1 to 22 µF

TABLE II
EXPERIMENTAL SYSTEM PARAMETERS & REQUIREMENTS

Input voltage V_{in}	12 to 14 VDC
Output voltage V_o (not lower than)	10 VDC
Nominal output Power	~ 10 W
Nominal switching frequency	100 kHz
Switching capacitor selection range C_1	0.1 to 100 µF
Duty cycle	50%
Dead Time	150 ns
Approximate Diode voltage drop V_d	0.2 V
C_2; ESR$_2$	1 µF; 0.033 Ω
C_o; ESR$_o$	470 µF; 0.18 Ω

Switches S_1 and S_2 could be chosen to be of different resistances when, for example, using P-Channel MOSFET for S_1 and N-Channel MOSFET for S_2. To illustrate the design steps for different switch resistances, we analyze the equivalent resistances for each phase, i.e. charge and discharge processes separately, and then accumulate the results to the total equivalent resistance (Fig. 2). The expressions for the equivalent resistance of the charge - R_{eA} and discharge - R_{eB} phases are:

$$R_{eA} = \frac{1}{2f_s \cdot C_1} \cdot \coth\left(\frac{\beta_A}{2}\right) \qquad \beta_A = \frac{1}{f_s \cdot R_1 C_1} \quad (8)$$

$$R_1 = R_{s1} + ESR_1$$

$$R_{eB} = \frac{1}{2f_s \cdot \left(\frac{C_1 \cdot C_o}{C_1 + C_o}\right)} \cdot \coth\left(\frac{\beta_B}{2}\right) \qquad \beta_B = \frac{1}{f_s \cdot R_2 \left(\frac{C_1 \cdot C_o}{C_1 + C_o}\right)} \quad (9)$$

$$R_2 = R_{s2} + ESR_1 + ESR_o$$

Fig. 8 presents the R_{eA} and R_{eB} as a function of R_1 and R_2 for different (f_sC) values. Once (f_sC) is chosen, R_1 and R_2 can be selected such that the sum of R_{eA} and R_{eB} will be equal to the required R_e (1.92 Ω in this example).

For the experimental design a (f_sC) value of 2.2 was selected, which translates into 22 µF capacitor (C_1) at 100 kHz switching frequency. R_1 and R_2 were selected to be 0.6 and 0.4 Ω, resulting in R_{eA} and R_{eB} of 1.2 and 0.8 Ω (Fig. 8), which brings the total equivalent resistance - R_e to comply

with the requirement of 2 Ω. Switch resistances $R_{s1} \approx 0.5$ Ω and $R_{s2} \approx 0.14$ Ω were found by subtracting the ESR values of $ESR_o = 0.18$ Ω and $ESR_1 = 0.085$ Ω according to (8) and (9) from R_1 and R_2.

The proposed design was evaluated mathematically, simulated in PSIM ver. 7.0.5, and tested experimentally on a breadboard with the following components: switches S_1 - SMU10P05, S_2 - SMU15N05 with 0.28 and 0.1 Ω respectively at room temperature, diodes V_{D1} and V_{D2} - MBR320P, with forward voltage drop of 0.2 V at room temperature and nominal converter current. The results are summarized in Table III. The comparison of experimental results and theoretical predictions under nominal load and switch resistance ratio between P-channel and N-channel of 3.5:1 respectively and switching-phase loop resistances R_1 and R_2 ratio of 1.5:1 are presented in Fig. 9. Stars in the figure represent experimental operating points of the converter. N-channel resistance - R_{s2} was measured to be around 0.2 Ω and P-channel resistance - R_{s1} around 0.55 Ω, the major difference between these values to datasheet specifications is the operation temperature of the switches under nominal load.

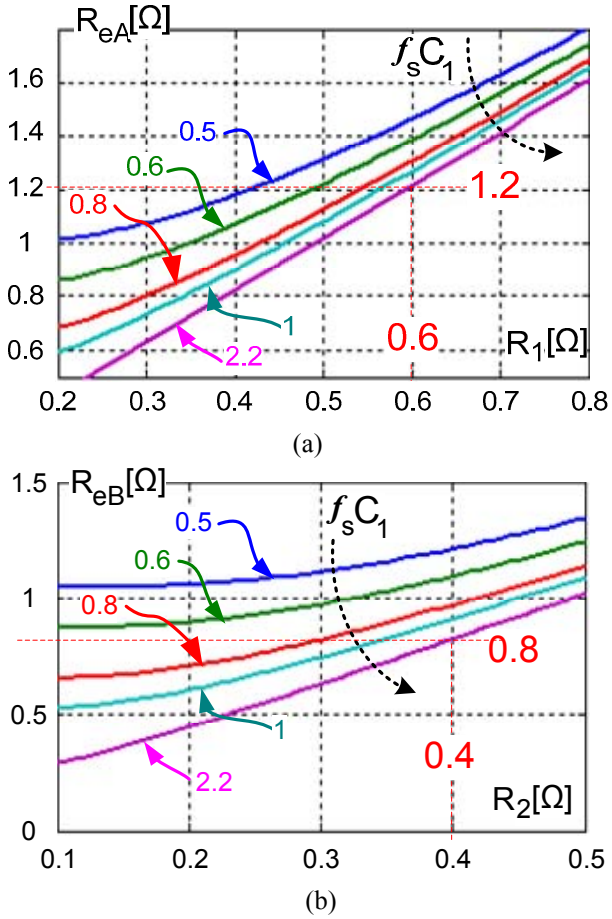

Fig. 8: R_e as a function of R_s and ESR for (a) charge and (b) discharge phases.

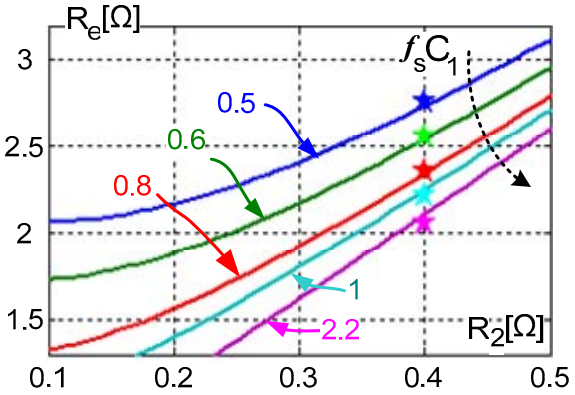

Fig. 9: Experimental waveforms.

TABLE III
MATHEMATICAL, SIMULATION AND EXPERIMENTAL RESULTS

Parameters	Theoretical (R_e)	PSIM Simulation (Cycle-by-cycle)	Experimental (Measurements)
R_L	V_o	V_o	V_o
12 Ω	10 V	10.1 V	9.9 V
20 Ω	10.6 V	10.65 V	10.64 V
30 Ω	10.92 V	10.95 V	10.87 V
50 Ω	11.18 V	11.2 V	11.14 V
100 Ω	11.39 V	11.39 V	11.36 V

V. CONCLUSION

A method of loss analysis in SCC was presented and design guidelines and rules for selecting of the SCC components were proposed. The direct dependency between switch resistances and the equivalent resistance of SCC was emphasized, and the apparent paradox that stems from (1) was clarified.

Two SCC topologies were analyzed mathematically and by simulation and a breadboard SCC was build and tested experimentally to verify the theoretical conjectures. The mathematical analysis predictions were found to be in a good agreement with simulation and experimental results.

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