CURRENT SOURCING ISOLATED GRID CONNECTED INVERTER

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Abstract: **This study proposes a soft switched Output Current Sourcing (OCS) grid connected inverter that applies a high frequency isolation transformer. Current sourcing at the output implies that, ideally, the injected current will be independent of the load voltage. The current injected to the line is controlled by varying the switching frequency and PWM at low currents. The system does not require the sensing of the output current or even the line voltage - except for synchronization. This is in contrast to the conventional voltage sourcing inverters where the small disturbance at the line voltage may lead to current run away and consequently a tight current feedback loop must be applied.**

The proposed topology and several proposed control approaches were analyzed and verified by simulations and by experiments. The simulation and experimental results confirm the theoretical analysis and show that the proposed inverter can be operated with no sensing of the line current or voltage except for synchronization.

I. INTRODUCTION

Grid connected inverters are important building blocks in renewable energy conversion systems. As described in earlier publications, they can be realized by a two stage topology [1, 2] or as a one stage system [3-5]. When isolation is required, it can be accomplished by introducing a line frequency transformer between the output filter and the grid utility [6]. Reduction of the physical size and cost of the inverter can be achieved by placing the isolation transformer at a high frequency branch as proposed in [7, 8]. A high frequency PWM non-isolated inverter that operates under soft-switching conditions was proposed in [9] while an isolated soft-switched inverter was shown in [10].

Notwithstanding the disparity of the many solutions proposed hitherto for grid connected inverters, most of them share a common feature - their outputs are basically voltage sources. Consequently, any mismatch between the synthesized output waveforms of these inverters and the grid voltage will generate large erroneous currents unless a current feedback is used to control the magnitude and phase of injected current.

An alternative approach to the grid connected inverter design, explored in this study, is to apply an inverter with an Output Current Sourcing (OCS) behavior rather than the voltage sourcing one. The OSC inverter is defined here as an inverter that behaves as a current source at its output. Current sourcing at the output implies that, ideally, the injected current will be independent of the load voltage. Grid connected OCS inverters were presented in [11] applying a flyback converter and in [12] based on a series resonant converter followed by a diode rectifier and a polarity commutator. To exhibit the OCS characteristics, the circuit in [12] must be operated below half the resonant frequency (discontinuous current conduction mode) and consequently, the reactive current in the resonant tank is expected to be high, especially at high power levels, while the resonant capacitor will have large physical dimensions.

This study describes a soft switched OCS grid connected inverter that applies a high frequency isolation transformer and does not include a resonant capacitor. The inverter's topology is based on the "AC inductor" concept described in [13]. The system does not require the sensing of the output current or even the line voltage - except for synchronization. The current in the main inductor of the proposed topology reverses its polarity every switching cycle making it easier to achieve soft switching. The OCS behavior implies that the output impedance of the proposed inverter is rather high and hence it is less sensitive to the output voltage waveform shape and distortion and to disturbances at either input or load side.

II. SYSTEM DESCRIPTION

The proposed inverter comprises two H bridges Q_1-Q_4 and Q_5-Q_8 (Fig. 1), a main inductor L_{in}, high frequency isolating transformer T1, and output rectifier D_1-D_4.

The input bridge, which operates under zero voltage switching conditions at turn on, generates a high frequency symmetrical square wave that is applied to the main inductor. The triangular current of the inductor is reflected to the secondary of the isolating transformer T1 and rectified by D_1-D_4. The rectified current is filtered by the output filter (C_F, L_F in Fig. 1) and fed to the line through the output bridge Q_5-Q_8 that is synchronized to the line and acts as a polarity commutator.

The theoretical analysis of the proposed inverter was carried out under the assumption that the switching frequency of the input bridge is much higher than that of grid, and hence one can assume that the voltage V_{out} applied to the output rectifier, at every given time instant (t) of the line cycle, is practically constant.

Consequently, the high frequency portion of the inverter can be analyzed by assuming that the output voltage is

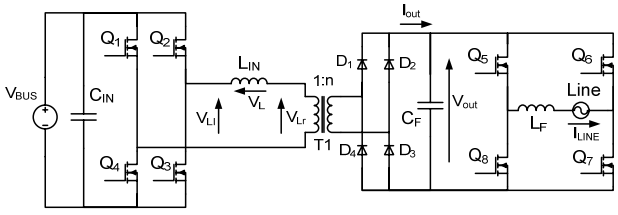

Figure 1. The proposed grid connected inverter.

constant as was described in [13]. For the sake of brevity only the essentials of the analysis are repeated here.

During the time interval t_1-t_2 (Fig. 2) of the high frequency switching cycle, the peak inductor current Ipk is:

$$Ipk = \frac{V_{bus} - V_{out}/n}{L_{in}}(t_2 - t_1) \quad (1)$$

where Lin is the inductance of the inductor. Similarly, during the time interval t_2-t_3 Ipk is expressed as:

$$Ipk = \frac{V_{bus} + V_{out}/n}{L_{in}}(t_3 - t_2) \quad (2)$$

From (1) and (2), and taking into account that (t_3-t_1) is half a switching cycle:

$$(t_2 - t_1) + (t_3 - t_2) = I_{pk} L_{in} \frac{2V_{bus}}{V_{bus}^2 - (V_{out}/n)^2} = \frac{1}{2F} \quad (3)$$

where F is the switching frequency.

Rearranging (3) back for Ipk we get:

$$Ipk = \frac{V_{bus}^2 - (V_{out}/n)^2}{4L_{in}FV_{bus}} \quad (4)$$

The output current is the rectified current of the inductor (reflected to the secondary of the isolation transformer) as depicted in Fig. 3. Since the output current is of a triangular shape, its average value is half its peak value:

$$\bar{I}_{out} = \frac{1}{2}\frac{Ipk}{n} = \frac{V_{bus}^2 - (V_{out}/n)^2}{8nL_{in}FV_{bus}} \quad (5)$$

where $\bar{I}_{out}$ is the output current averaged over the switching cycle.

It is assumed that the line voltage, which absolute value equals to the output voltage, i.e. $V_{out}=|V_{line}(t)|$, is of form:

$$V_{line}(t) = V_{rms}\sqrt{2}\sin 2\pi f_{line} t \quad (6)$$

where V_{rms} is rms value of the line voltage, f_{line}- line frequency.

Considering (6), (5) can be rewritten as follows:

$$\bar{I}_{out}(t) = \frac{V_{bus}^2 - V_{line}^2(t)/n^2}{8 \cdot n \cdot L_{in} \cdot F(t) \cdot V_{bus}} \quad (7)$$

where $\bar{I}_{out}(t)$ is the average output current of the inverter and F(t) is the switching frequency at time instant t.

Since energy will be delivered to the grid if and only if the nominator of (7) is positive, the lower limit for "n" will be :

$$n > V_{rms}\sqrt{2}/V_{bus} \quad (8)$$

To deliver a current which is in phase with, and of the shape of the line voltage, the inverters output current should be of form:

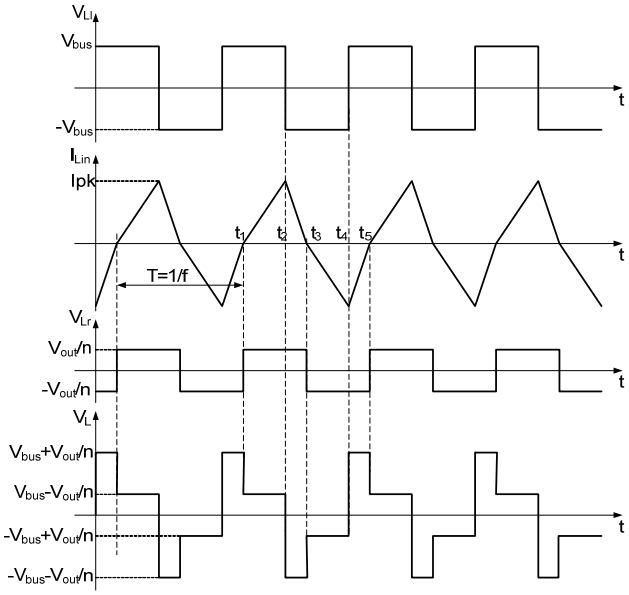

Figure 2. Basic waveforms of the proposed inverter. From top to bottom: V_{L1}, Inductor current, V_{Lr}, voltage across inductor.

$$\bar{I}_{out}(t) = I_{rms}\sqrt{2}\sin 2\pi f_{line} t = \frac{P_{out}}{V_{rms}}\sqrt{2}\sin 2\pi f_{line} t \quad (9)$$

where I_{rms} is rms value of the line current, P_{out} – average power delivered to the line.

Considering (6), (9) can be rewritten as follows:

$$\bar{I}_{out}(t) = P_{out} V_{line}(t)/V_{rms}^2 \quad (10)$$

Equations (10) and (7) can now be used to obtain the expression for the switching frequency as a function of time F(t), that will ensure a sinusoidal current injection into the grid:

$$F(t) = K_P \frac{V_{bus}^2 - (V_{line}(t)/n)^2}{V_{line}(t)},$$

$$\text{where } K_p = \frac{V_{rms}^2}{8nL_{in}P_{out}V_{bus}} \quad (11)$$

Based on (11), three different control approaches can be considered. One option is to measure the instantaneous line voltage $V_{line}(t)$ and apply the sampled value to calculate the required frequency F(t) of the input bridge gate pulses according to (11). The coefficient K_p can be considered as a scaling factor that will be obtained from the Maximum Power Point Tracking (MPPT) algorithm. For any given operating conditions, K_p will be adjusted by the MPPT section to obtain the maximum power available from the photovoltaic cell panels.

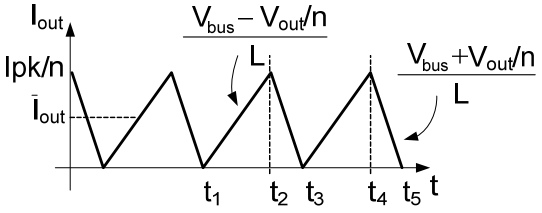

Figure 3. Zoom on I_{out} (Figure 1).

Another option for deriving F(t) is to measure only the rms value of the line voltage (much lower sampling rate) and calculate the V_{line} according to (6). For this case, (11) can be rewritten as follows:

$$F(t) = K_p \frac{V_{bus}^2 - 2(V_{rms}/n)^2 \sin^2(2\pi f_{line} t)}{V_{rms} \sin(2\pi f_{line} t)} \qquad (12)$$

Yet another control option would be to calculate the frequency F(t) without sensing the line voltage at all. This can be accomplished by assuming some predefined (nominal) rms value of the line voltage (V_{nom}):

$$F(t) = K_p \frac{V_{bus}^2 - 2(V_{nom}/n)^2 \sin^2(2\pi f_{line} t)}{V_{nom} \sin(2\pi f_{line} t)} \qquad (13)$$

Although there is no need to measure the line voltage in this case, there would be a need to synchronize the operation to the line frequency by, for example, sensing the zero crossing of the line voltage.

It should be stressed though that none of the above mentioned control methods require the sensing of the output current.

From the practical point of view, the first approach is the most complicated one as it requires line sensing circuitry with rather high sampling rate. In the second case, the sampling rate can be much lower as only the rms value of the line voltage needs to be measured. However, the current injected to the line may be slightly distorted. The third method is the simplest among the suggested control approaches since no line sensing circuitry is needed except for synchronization. On the other hand, the THD of the current generated in this case will increase as the difference between the nominal and actual rms values of the line voltage increases.

By combining (7) and (13), the current generated in the last case is found to be:

$$\bar{I}_{out}(t) = \frac{P_{out}}{V_{nom}^2} \frac{1 - \alpha^2\beta^2 \sin^2(2\pi f_{line} t)}{1 - \beta^2 \sin^2(2\pi f_{line} t)} V_{nom}(t) \qquad (14)$$

where:

$$V_{nom}(t) = V_{nom}\sqrt{2}\sin(2\pi f_{line} t),\ \alpha = \frac{V_{rms}}{V_{nom}},\ \beta = \frac{\sqrt{2}}{n}\frac{V_{nom}}{V_{bus}}.$$

In all three alternatives (11-13) the frequency needs to go to high (and even impractical) values around the zero crossing of the line voltage when its levels, and hence the current levels, are low. One possible way to overcome this practical limitation is to apply pulse width modulation while staying at constant switching frequency. In this mode of operation, two diagonal switches (say Q1 and Q3) are kept "on" for some time interval t_{on}, allowing the inductor's current to increase (Fig. 4), and then switched "off". During "t_{off}" the current keeps flowing in the same direction and hence the body diodes of Q2 and Q4 will conduct until the current through the inductor reaches zero. In the next switching cycle, the sequence is repeated for Q2, Q4 and body diodes of Q1, Q2.

The output current is obtained by rectifying the inductor's current. The average of the output current over the switching cycle is given as:

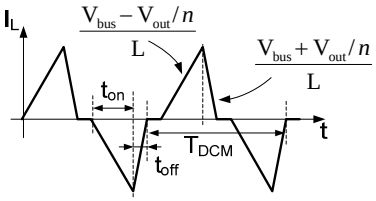

Figure 4. Inductor's current at PWM mode of operation.

$$\bar{I}_{out}(t) = \frac{1}{n}\left[\frac{V_{bus} - V_{out}/n}{L} t_{on}^2 + \frac{V_{bus} + V_{out}/n}{L} t_{off}^2\right] f_{DCM} \qquad (15)$$

where $f_{DCM} = 1/T_{DCM}$

From Fig. 4, the ratio of "t_{on}" to "t_{off}" can be expressed as:

$$\frac{t_{off}}{t_{on}} = \frac{V_{bus} - V_{out}/n}{V_{bus} + V_{out}/n} \qquad (16)$$

Substituting this back to (15) yields:

$$\bar{I}_{out}(t) = \frac{2V_{bus} \cdot t_{on}^2}{nL} \frac{V_{bus} - V_{out}/n}{V_{bus} + V_{out}/n} f_{DCM} \qquad (17)$$

For the output current to follow the line voltage, (17) should be equal to (10). Since $|V_{out}|=|V_{line}(t)|$, "t_{on}" can be expressed as:

$$t_{on} = \sqrt{\frac{V_{line}(t)}{K_p K_{DCM}} \frac{V_{bus} + V_{line}(t)/n}{V_{bus} - V_{line}(t)/n}} \qquad (18)$$

where $K_{DCM} = 8V_{bus}^2 f_{DCM}$.

III. Experimental

The behavior of the proposed OCS inverter was tested experimentally on a 1kW prototype that was build according to the topology shown in Fig. 1 and was powered by a DC voltage source. The transformer ratio "n" was set to 2. The value of the main inductor was 28μH. The output capacitor C_F was 1μF. The switching frequency varied from 60kHz at the maximum of the line voltage up to 200kHz. Near the zero crossings of the line voltage, the PWM of the input bridge was applied to obtain sinusoidal shaped average current while staying at the constant switching frequency of 50kHz.

The circuit was controlled by a microcontroller (dsPIC30F2020, Microchip). Tests were run up to 250W.

Fig. 5 shows the output current measured when the inverter was connected to 110Vrms line. Fig. 6 shows the instantaneous inductors current at both PWM and frequency modulation operational modes.

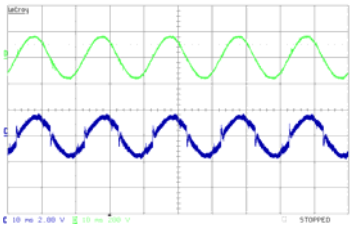

Figure 5. Output behavior of the inverter with no sensing of the output voltage. Vin=115V; Vline=110Vrms; Pout=150W. Upper trace: line current (I_{LINE}) 2A/div; Lower trace: line voltage 200V/div; Horizontal scale: 20ms/div.

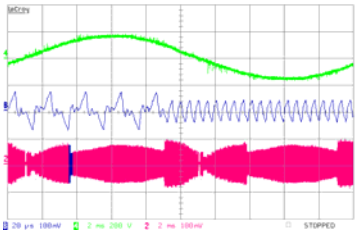

Figure 6. Inductor current over a line period. Lower trace: inductors current 5A/div; Middle trace: zoom-in of the marked zone of the lower trace 5A/div. Upper trace: line voltage 200V/div; Horizontal scale: upper and lower traces - 2ms/div; middle trace – 20μs/div.

The following steps were taken to prevent high charging current of the output capacitor and the injection of spurious currents to the grid when first connecting the inverter to the grid. First, disabling all the drivers of the output bridge (Fig. 7) when the inverter is first plugged into the line. This allows the capacitor to charge to the peak value of the line voltage through the current limiting resistor R and body diodes of Q_5-Q_8 (Fig. 7). Following a predefined delay, the output relay (Fig. 7) is enabled, shorting the resistor R. Finally the output bridge drivers are enabled when the line voltage is at its peak (Fig. 8) to ensure that the capacitor and the line voltages are close to each other and consequently no high current spikes would flow via the output bridge switches.

IV. Discussion and Conclusions

This study presents an OCS inverter that is controlled by varying the switching frequency. All the switches are switched under zero voltage at turn on. The proposed inverter applies high frequency isolation transformer.

It is evident from (7) that the current injected into the line is not independent of the line voltage. It was shown, however, that the influence of the line voltage on the output current can be reduced considerably by proper design. Consequently, the proposed topology behaves as a current source for all practical needs.

Experimental results verify the theoretical predictions that the proposed control method, with no sensing of the line voltage, makes the inverter act as a stable current source. The proposed inverter can be operated in open loop, i.e. with no need to sense the line current and even without sensing the line voltage – except for synchronization. Consequently the outputs of the inverters built according to the proposed topology can be connected in parallel. For the rigid line, the output current of every single inverter will be independent of the adjacent systems. That is, no special interconnection circuits or current sharing control loops are basically required - except for redundancy reasons. This is in contrast to the conventional voltage sourcing inverters where even a small disturbance at the line voltage may lead to current run away and consequently a tight current feedback loop must be applied.

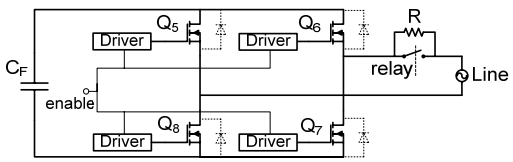

Figure 7. Output bridge and grid connecting circuitry.

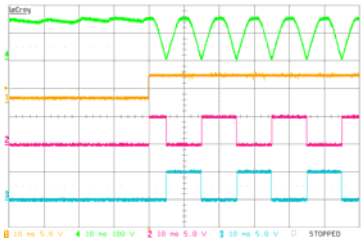

Figure 8. Grid connection sequence. V_{line}=110V; From top to bottom: capacitor's voltage 100V/div; "enable" signal of the output inverter 5V/div; gate signal to one diagonal of the output bridge 5V/div; gate signal to another diagonal of the output bridge 5V/div; Horizontal scale: 10ms/div.

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