Transformer's Capacitance Effect on the Operation of Triangular-Current Shaped Soft-Switched Converters

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Abstract - This paper addresses the effect of the isolating transformer parasitic capacitor in soft switched converter topologies that apply triangular inductor current. When a transformer is included in the circuit, it will not only add (leakage) inductance to the converter but will also add capacitance. This capacitance will cause a partial resonance behavior and therefore may alter the voltage transfer ratio of the converter. The objective of this study was to analyze the effect of this capacitance on the behavior of Triangular Current Shaped (TCS) soft-switched converters.

The isolated TCS converter was analyzed and the theoretical results were verified by simulations and experimentally at a 1kW power level. The analysis show that the transformer's capacitance boosts the voltage gain of the converter, changes the shape of the inductor current and hence modifies the RMS value of the current. It was found though, that by proper design the RMS current (for same power level) may in fact be reduced and consequently, will result in lower conduction losses as compared to the case with no capacitor.

I. INTRODUCTION

In classical soft switched converters, a resonant network is normally applied to achieve soft switching [1]. Another approach for achieving soft switching, that is similar to resonant load converters but without applying a resonant capacitor, was reported in [2-6]. In the latter cases the current waveforms are non sinusoidal but rather triangular. Due to the fact that the resonant capacitor can be omitted, these topologies are especially suitable for high current applications [2, 5].

The Triangular Current Shaped (TCS) converter can be built without [6] or with transformer isolation. If a high input to output voltage ratio is required, as for example in fuel cells applications, or laser drivers, a step up isolation transformer will be normally introduced between the input and output sides of the converter. In some applications, an isolation transformer may be required for safety reasons even in low output voltage applications. When a transformer is included, it will not only add (leakage) inductance to the converter but will also add capacitance. This capacitance will cause a partial resonance behavior and therefore may alter the voltage transfer ratio of the converter. The objective of this study was to analyze the effect of this capacitance on the behavior of isolated TCS converter.

II. THE BASIC TRANSFORMER ISOLATED TCS CONVERTER

As background, we first consider the isolated topology shown in Fig. 1 with no winding capacitance. We assume that the isolated converter (Fig. 1) is fed from an input voltage Vin, runs at a switching frequency f_s, and the output voltage is V_{out}. The current is rectified at the secondary side by means of a voltage doubler. The latter is beneficial when extra gain is needed and may simplify the design of the isolating transformer. To reduce the RMS value of the inductor current, it is advantageous to operate this converter by the phase shifted PWM control scheme. In this operational mode, the circulating current is reduced by locking the primary current within the bridge switches rather than injecting it back to the input [6]. This is achieved by shorting the current via the two upper switches (Q1, Q2 - ON) or the two lower switches (Q3, Q4 - ON) of the input bridge (Fig. 1).

The output voltage of the bridge (V_{MR}-V_{ML}) and the inductor current for this mode of operation are sketched in Fig. 2. It is further assumed that the isolation transformer has a transformer ratio n and the voltage reflected to its primary side (V_{refl}) is lower than the input voltage.

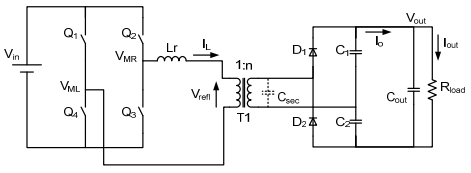

Figure 1. Isolated TCS converter with voltage doubler at the output side.

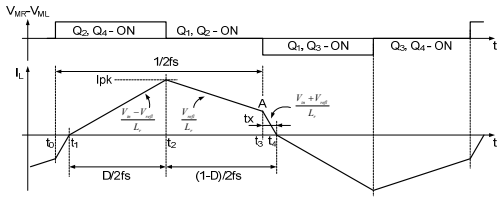

Figure 2. Inductor current of an isolated TCS converter.

Based on the inductor current shape (Fig. 2), three operational stages can be identified:

a: time interval t1- t2

During this time interval, the current through the inductor rises linearly with a slope determined by the difference between the input voltage and the voltage reflected to the primary of the transformer (V_{refl}). This interval ends when transistor Q4 turns off and Q1 turns on (after a small dead time). The peak current of the inductor will thus be calculated as:

$$I_{pk} = \frac{V_{in}}{L_r}\frac{D}{2f_s}(1-k) \qquad (1)$$

where $k = V_{refl}/V_{in}$; $V_{refl} = V_{out}/2n$; L_r - main inductor; f_s - switching frequency; $D = \frac{t_2 - t_1}{2f_s}$.

b: time interval t2-t3

During this interval the voltage applied to the inductor is the voltage reflected to the primary of the isolation transformer (V_{refl}). The current through the inductor decreases with a slope V_{refl}/L_r. This interval ends when transistor Q2 turns off and Q3 turns on.

c: time interval t3-t4

The voltage across the inductor is equal to the sum of the input and the reflected voltages. The inductor current drops to zero.

The switching at point A at t_3 (Fig. 2) may occur at non-zero current and consequently the current during the time interval tx (t_3-t_4) will be fed back to the input, increasing the RMS value of the input current. To prevent the energy return to the input during this time interval (t_3-t_4), the frequency (f_s) and duty cycle (D) can be adjusted such that the residual current is close to zero (tx=0) as shown in Fig. 3. In this case, the switching will be under zero current switching conditions and if some residual current is allowed, it will maintain zero voltage switching at turn on.

From Fig. 3, the voltage applied to the inductor during t_1-t_2 is $V_{in}(1-k)$, and during t_2-t_3 the inductors voltage is $V_{in}k$. Since the average voltage across the inductor must be kept zero, one can write:

$$V_{in}(1-k)\frac{D}{2f_s} = V_{in}k\frac{1-D}{2f_s} \qquad (2)$$

From (2), by canceling out the similar terms and rearranging:

$$k = D \qquad (3)$$

That is, in this operation mode, the duty cycle (D) sets the ratio of the reflected to primary output voltage (V_{refl}) to the input voltage. Considering the transformer ratio and the gain contribution of the voltage doubler at the secondary side of the transformer, the output to the input ratio will be given as follows:

$$\frac{V_{out}}{V_{in}} = 2nD \qquad (4)$$

III. TRANSFORMER ISOLATED TCS CONVERTER ANALYSIS (WITH WINDING CAPACITANCE)

Fig. 4 depicts the shape of the inductor current of the isolated converter when the parasitic winding capacitor is taken into consideration. Based on Fig. 4, four operational stages can be identified:

a: time period t_0-t_1 (resonant phase).

At the beginning of this time interval (Q2 and Q4 are on) the voltage across the capacitor is negative and its absolute value equals to the half the output voltage. During this period the current through the main inductor is sinusoidal due to the resonance between L_r and the equivalent parasitic capacitor at the secondary winding of the transformer (C_{sec}). The inductor current and the capacitor voltage are given as follows:

$$I_{Lr}(t) = V_{in}\frac{1+k}{Z_r}\sin(2\pi \cdot f_r \cdot t) \qquad (5a)$$

$$V_{C\sec}(t) = V_{in}\left[1-(1+k)\cos(2\pi \cdot f_r \cdot t)\right] \qquad (5b)$$

where $k = V_{refl}/V_{in}$; $V_{refl} = V_{out}/2n$; $Z_r = \frac{1}{n}\sqrt{\frac{L_r}{C_{\sec}}}$; $f_r = \frac{1}{2\pi \cdot n\sqrt{L_r \cdot C_{\sec}}}$.

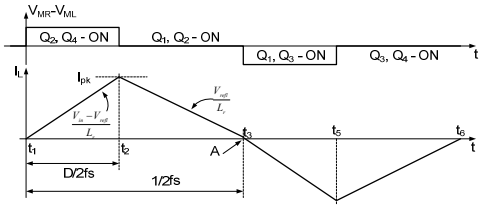

Figure 3. Inductor current of an isolated TCS converter operating under ZCS and ZVS at turn-on.

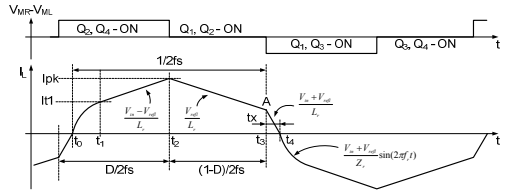

Figure 4. Inductor current of an isolated TCS converter with parasitic capacitance.

This time interval ends when the voltage across the capacitor reaches half of the output voltage (in the voltage doubler configuration). At this instance, the relevant output diode starts to conduct clamping the voltage across the capacitor C_{sec} to $V_{out}/2$.

The time instance t_1 can be calculated by substituting $V_{C\sec}(t_1) = V_{out}/2 = k \cdot n \cdot V_{in}$ into (5b):

$$t_1 = \frac{1}{2\pi f_r} \arccos \frac{1-k}{1+k} \tag{6}$$

Substituting (6) into (5a) the current at the end of this time period will be found as follows:

$$I(t_1) = 2\sqrt{k}\,\frac{V_{in}}{Z_r} \tag{7}$$

b: time interval t_1- t_2

During this time interval, the current through the inductor rises linearly with a slope determined by the difference between the input voltage and the voltage reflected to the primary of the transformer. This interval ends when transistor Q4 turns off and Q1 turns on (after a small dead time). The peak current of the inductor will thus be calculated as:

$$I_{pk} = 2\sqrt{k}\,\frac{V_{in}}{Z_r} + \frac{V_{in}}{Z_r} 2\pi f_r (1-k)(t_2 - t_1) \tag{8}$$

c: time interval t_2-t_3

The output of the input bridge is shorted via Q1, Q2, so the voltage applied to the inductor is equal to the voltage reflected to the primary of the isolation transformer ($V_{refl} = V_{out}/2n$). The current through the inductor decreases with a slope V_{refl}/L_r. This interval ends when transistor Q2 turns off and Q3 turns on. The inductor current at the end of this time interval is found to be:

$$I(t_3) = I_{pk} - \frac{V_{in}}{Z_r} k 2\pi f_r (t_3 - t_2) \tag{9}$$

d: time interval t_3-t_4

The voltage applied to the inductor is equal to the sum of the input and the reflected voltages. The inductor current drops to zero.

The duration of this time interval is found to be:

$$t_x = \frac{I(t_3)}{V_{in}/Z_r} \frac{1}{2\pi f_r (1+k)} \tag{10}$$

As discussed below, this time interval can be adjusted for better performance.

Similarly to the case with no capacitance, to prevent the energy return to the input during the time interval t_3-t_4, and to maintain zero current switching at turn off of Q2 and zero current and voltage switching at turn on of Q3, the frequency (f_s) and duty cycle (D) should be adjusted such that the residual current is close to zero (t_x=0). This is demonstrated in Fig. 5. This operation mode is denoted here as Borderline Conduction Mode (BCM). The duty cycle in BCM is referenced as D_{BL}

In BCM, the current increase during the time interval t_0-t_2 is equal to the drop in the current during t_2-t_3. From (8), expressing the time interval (t_2-t_0) as $D_{BL}/2f_s$ we get:

$$\Delta I_{t0-t2} = I_{pk} = 2\sqrt{k}\,\frac{V_{in}}{Z_r} + \frac{V_{in}}{Z_r} 2\pi f_r (1-k)\left(\frac{D_{BL}}{2f_s} - t_1\right) \tag{11}$$

where: t_1 is given by (6).

Similarly,

$$\Delta I_{t2-t3} = I_{pk} = \frac{V_{in} k}{Z_r} 2\pi f_r \frac{1-D_{BL}}{2f_s} \tag{12}$$

By equating (11) and (12) the duty cycle for the BCM was found to be:

$$D_{BL} = k - \frac{m}{\pi}\left[2\sqrt{k} - (1-k)\arccos\left(\frac{1-k}{1+k}\right)\right] \tag{13}$$

The normalized average output current, delivered to the load in BCM was found from (5a), (6), (7), (11), (12) and (13) to be:

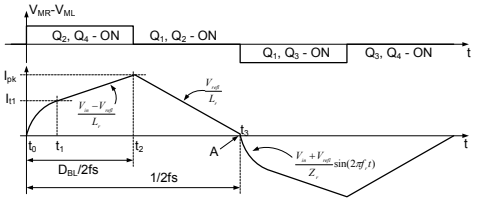

Figure 5. Inductor current of an isolated TCS converter operating in BCM (with parasitic capacitance).

$$I^*_{out\,av} = \frac{k}{2n}\left[\begin{array}{l} \frac{m}{\pi}(1-k)\arccos^2\left(\frac{1-k}{1+k}\right)+ \\ \left(\frac{4m}{\pi}\sqrt{k}+2(1-k)\right)\arccos\left(\frac{1-k}{1+k}\right)+ \\ 4\sqrt{k}+\frac{\pi}{m}(1-k)-\frac{4m}{\pi} \end{array}\right] \quad (14)$$

where: $I^*_{out\,av} = \frac{I_{out\,av}}{V_{refl}/Z_r}$, $I_{out\,av}$ - average current delivered to the load and $m = f_s / f_r$.

The same procedure was used to derive the expression for the normalized rms value of the inductor current:

$$I^*_{rms} = \sqrt{\begin{array}{l} (1+k)^2\frac{m}{2\pi}\left[\arccos\left(\frac{1-k}{1+k}\right)-\frac{2\sqrt{k}(1-k)}{(1+k)^2}\right]+ \\ \left[\frac{\pi^2k^2}{3m^2}(1-D_{BL})^3+\frac{1}{3}\left(D_{BL}-\frac{m}{\pi}\arccos\left(\frac{1-k}{1+k}\right)\right)\times\right. \\ \left.\left(4k+\frac{\pi^2k^2}{m^2}(1-D_{BL})^2+\frac{2k\sqrt{k}\pi}{m}(1-D_{BL})\right)\right] \end{array}} \quad (15)$$

where: $I^*_{rms} = \frac{I_{rms}}{V_{refl}/Z_r}$, I_{rms} – rms value of inductor current.

In this operational mode, the power delivered to the load will be adjusted by controlling both the switching frequency {m} and the duty cycle (D_{BL}). The latter needs to be set according to (13) for each operating conditions in terms of input to output voltage ratio and power level.

For a duty cycles lower then D_{BL} the inductor current will cross the zero before the relevant transistor of the leading lag is switched off. For example, in the half switching cycle described above (Fig. 5), if the inductor current becomes negative prior to the time instance t_3, the body diode of Q4 will start conducting. This will result in hard switching and a current spike due to the reverse recovery of this diode when the complimentary switch Q1 turns on. Consequently, for safe operation, the duty cycle must be always higher than D_{BL} for every switching frequency. This will assure not only near zero current switching but also current lag and hence zero voltage switching at turn on (e.g. of Q1 in above example).

IV. The Effect of the Transformer's Capacitance in BCM Operation

Comparing the duty cycle D_{BL} found for the case when the transformer's capacitance is taken into account (13), to the no capacitance case (3) one finds that for the same voltage conversion ratio ($2nk$), the steady state duty cycles will be different. This difference is due to the second term in (13). Fig. 6 plots the value in the brackets of the second term of (13) for k below unity.

It follows from this plot that the second term of (13) is always positive for the range of interest ($0 < k < 1$). Consequently, the duty cycle D_{BL} in the case with the winding capacitance is lower then the reflected to primary output to input ratio (k). This is unlike the case with no winding capacitor where the ratio k is set by the duty cycle (3). Putting this in other words - for the same duty cycle, the ratio k in the case of the converter with the capacitor will always be higher. It means that the capacitance adds some extra voltage gain to the converter. On the other hand, the reactive current charging the capacitor at the beginning of every cycle (time interval t_0-t_1 in Fig. 4&5) will result in a change of the RMS value of the inductor current. Interestingly, this will not necessarily lead to higher conduction losses. In fact, for some operating conditions, the ratio of the RMS current to the average current (which is proportional to the output power for a fixed reflected voltage) can even be better (lower) than for the case with no capacitance at all. This is demonstrated in Figs. 7-8 where the RMS-to-average current ratio is plotted vs. the output power for different reflected voltages (different k values and hence output voltages). These figures show that when the resonant (parasitic) capacitor is relatively small, the ratio is lower as compared to the case with no capacitance, for a quite wide operating range. These curves were calculated for L=0.55μH, Vin=24V, and for a switching frequency range of 75kHz down to 25kHz. The horizontal line at about 1.55 is the theoretical value ($2/\sqrt{3}$) of the pure triangular case.

V. Simulation and Experimental

The behavior of the isolated TCS soft switched converter was verified by running a full circuit (cycle-by-cycle) simulation and conducting measurements on an experimental converter. Fig 9 shows the cycle-by-cycle simulation model of the converter.

The simulation model comprises of an input bridge implemented by switches S1-S4 and body diodes D1-D4, main inductor L1, isolation transformer (L3, L4), and voltage doubler (D12, D13, C2, C3).

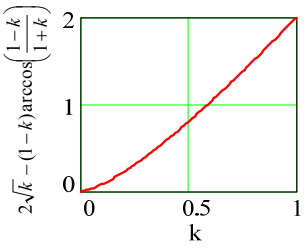

Figure 6. Plot of the value in the brackets of the second term of (13).

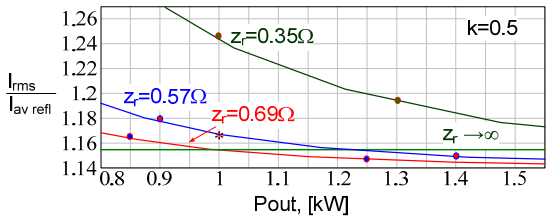

Figure 7. Ratio of input rms current to output average current reflected to the primary for different parasitic capacitors and primary-to-input voltage ratio (k) 0.5. Vin=24V. Solid line: theoretical predictions; Dots: cycle-by-cycle simulation results. Asterisk : Experimental converter

The circuit is fed by a dc voltage source V8. The output voltage is set by the DC voltage source V10 according to a chosen k ratio. The winding capacitance is modeled by capacitor C_{sec}. Simulation results for the ratio I_{rms}/I_{av_refl} at different operating conditions are shown as dots in Fig. 7 and 8.

Fig. 10 shows the experimental results measured on an isolated 1kW TCS converter (Fig. 1) for Vin=24V. The output voltage was about 4kV. The circuit was operated at BCM. The input bridge comprised of IRFP4368 (International Rectifiers, USA) MOSFETs with typical Rds_{on} of 1.46mΩ@25^{0}C. The main inductor was about 0.55µH (leakage of the isolation transformer and stray inductances in the circuit), output capacitors were 0.3µF each, and load was about 15kΩ. The transformer was built on an E65 core and comprised of two primary turns and 338 secondary. The converter was assembled on 4 layers PCB. The outer layers that were used for carrying the power were of 3oz copper. The equivalent parasitic capacitor of the secondary winding was about 60pF. The switching frequency was set to 35kHz and the output power was about 1kW. The efficiency was measured to be 81.7%. The peak inductor current measured experimentally (Fig. 9) was about 170A. The peak inductor current calculated theoretically at the operating conditions stated above is 173A. The current at the end of the capacitor charging interval (I_{t1}) calculated from (7) is 60A. I_{t1} found from the Fig. 9 is about 60A as well.

Fig. 11 depicts the estimated losses distribution for the above described conditions.

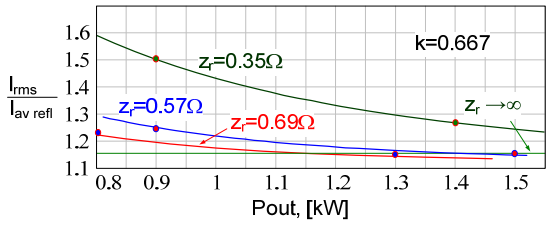

Figure 8. Ratio of input rms current to output average current reflected to the primary for different parasitic capacitors and primary-to-input voltage ratio (k) 0.667. Vin=24V. Solid line: theoretical predictions; Dots: cycle-by-cycle simulation results.

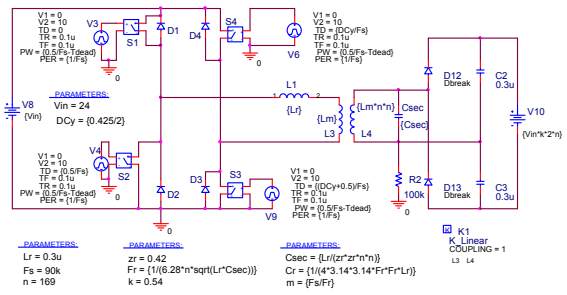

Figure 9. PSPICE cycle-by-cycle simulation model.

The conduction losses estimation is based on a primary rms current of 100A. The switching losses were calculated assuming linear change of the drain current and voltage at turn off, and switching time of 300ns. The transformer cupper losses were measured by first mapping the temperature of the transformer winding for different power dissipation levels. It was accomplished by injecting a DC current into the secondary winding of the transformer. The power was measured by monitoring the current and the voltage of the secondary winding and the surface temperature of the transformer was measured for different injected power levels. The copper losses in the experimental setup were then determined by measuring the surface temperature of the transformer while operating the converter and comparing it to the temperature versus power curve.

The loss estimation chart presented in Fig. 11 suggests that that the conduction losses (MOSFET, wiring and PCB) are dominant. The wiring and PCB losses were estimated by subtracting from the total power loss (180W) the estimated losses of the active and passive devices. The balance, 60W, is assumed to be dissipated by inter-wiring and PCB of the experimental breadboard. It should be noted that with an rms current of 100A, 6mΩ of stray resistance will dissipate the 60W. The PCB losses were relatively high due to the fact that the copper gauge was 3Oz while using only two layers to carry the power.

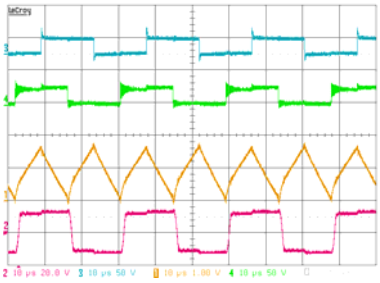

Figure 10. Experimental results.

Vin=24.24V; Iin=51.7A; Vout≈4kV; Iout=254mA; Vrefl=11.9V.

Upper trace: lead lag mid. Point, 50V/div; Second trace from top: lagging lag mid. point 50V/div; Third trace from top: rectified inductors current 100A/div; Lower trace: primary voltage 50V/div; Horizontal scale: 10us/div.

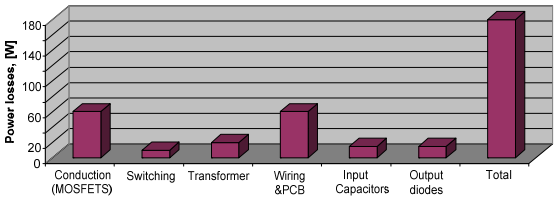

Figure 11. Estimated power losses distribution of experimental breadboard.

A second reason for the high PCB conduction losses is the small package of the MOSFETs (TO247) that has rather small and closely spaced pins. This dictates a layout with sections of narrow traces. Thermal imaging revealed that the temperature of some parts of the PCB were as high as 70^0C when the system was operated under room temperature conditions. Fig. 12 shows the measurement results for the converter when 100pF capacitor was added to the secondary of the isolation transformer. Together with the parasitic winding capacitance the equivalent secondary capacitance was about 160pF. The measurements were conducted for the same output voltage (4kV). The input voltage was somewhat lower as compared to the case with no additional capacitance, as predicted by theoretical analysis. The efficiency was about 80.6%. The peak current in this case was about the same but the current at the end of the resonant phase was higher and the resonant phase lasted longer. According to Fig. 10, the $I_{t1} \approx 100A$ (I_{t1} calculated from (7) is 98A) and $t_1 \approx 2\mu s$ (the value calculated from (6) is $1.9\mu s$). The higher rms value of the inductor current, due to the higher reactive current charging the capacitor, explains the lower efficiency (as compared to the case with no additional capacitor) measured in this experiment.

VI. Discussion and Conclusions

This study presented an isolated TCS converter and investigated the effect of the transformer's parasitic capacitance on its behavior.

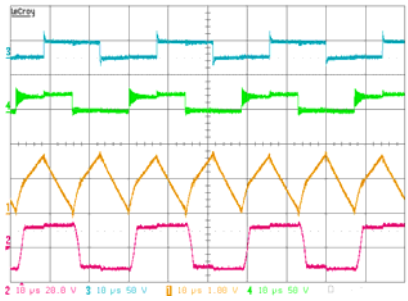

Figure 12. Experimental results. $C_{sec} \approx 160$pF.

Vin=23 V; Iin=55A; Vout≈4kV; Iout=253mA; Vrefl=11.9V.

Upper trace: lead lag mid. point 50V/div; Second trace from top: lagging lag mid. point 50V/div; Third trace from top: Rectified inductors current 100A/div; Lower trace: primary voltage 50V/div; Horizontal scale: 10us/div.

The proposed one stage topology features high voltage gain, current sourcing behavior at the output and ability to operate with high currents at the input. The latter stems from the fact that no series capacitor is applied at the input side. These features makes this topology beneficial for high power, low input, and high output application like, for example a microwave oven fed from a 24V battery or fuel cell converters where high input-to-output gain is needed.

The results of the analysis show that the capacitance of the transformer's winding boosts the voltage gain of the converter and shapes the inductor current, changing thereby its RMS value. It was found though, that this change can lead to higher or lower RMS currents for same power level. This is because the resonant part of the current that is caused by the transformer's capacitance has two opposing effects, as demonstrated in Figs. 13&14. These figures show the inductor and the output current for two different capacitors. On the one hand , the resonant portion of the current adds a reactive current to the primary side since during the resonant part no current is outputted to the secondary (area A in Figs. 13&14). On the other hand, the shape of the current that passes through the transformer to the output, has a lower RMS to average current ratio. This is because the first part of the current (area B in Figs. 13&14) has a trapezoidal shape while in the non resonant case the shape is triangular [6]. In the triangular case, the RMS to average current is $2/\sqrt{3}$ while the ratio calculated for the trapezoidal shape is always lower. When the transformer's capacitance is large (Fig. 14), the reactive current effect is dominant and the overall RMS to average current is higher (Figs. 7-8). However, when the capacitance is small (Fig. 13) the reactive current is relatively low and current is outputted to the load during the majority of the switching cycle. In this case the mitigating effect of the lower RMS value of the trapezoidal shape prevails and the overall conduction losses will be lower. The normalized analysis and curves presented in this paper may help designers to select the optimal operating conditions, such as the optimal reflected voltage, for maximum efficiency.

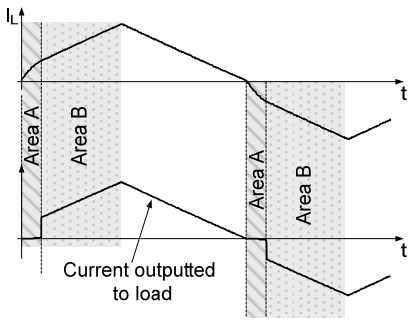

Figure 13. Effect of parasitic capacitance. Small capacitance.

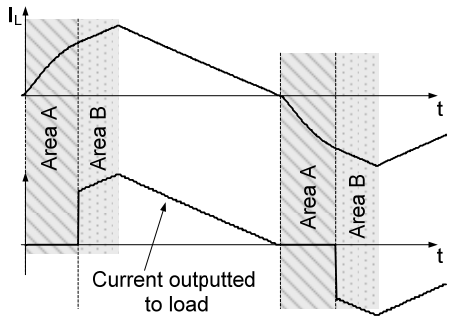

Figure 14. Effect of parasitic capacitance. Large capacitance.

The experimental converter was not designed to operate at the optimal area of operation (the I_{rms}/I_{av_refl} ratio was 1.162 (Fig. 7), which is slightly above $2/\sqrt{3}$ ratio, found when the current is purely triangular). The major reason for this was the requirement to operate at nominal power for quite wide input voltage range (18V-30V). As a result, the reflected voltage had to be kept at relatively low value. This is because according to the analysis developed in this study, for the low input voltage (18V), and the given leakage inductance, the reflected voltage needed to be as low as 12V to allow transferring the nominal power without lowering the switching frequencies down to the audible range. In addition, due to the lack of space a relatively small core for the main transformer had to be chosen. Notwithstanding these deficiencies, the efficiency of the experimental converter was found to be on par with the case of, say, two serially connected stages of lower gain each. This is due to the fact that the converter under study was operated under zero current and zero voltage at turn on, so the switching losses were relatively small. Moreover, it follows from the losses analysis (Fig. 11) that the efficiency can even be improved by utilizing thicker PCB layers (e.g. 4-6oz) and a bigger transformer.

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