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Algebraic Foundation of Self Adjusting Switched Capacitors Converters

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***Abstract* -- An algebraic model that describes the operation of binary Switched-Capacitor Converters (SCC) was developed and generalized to any radix case. The proposed approach reduces the power loss by increasing the number of target voltages. In the binary case, the flying capacitors are automatically kept charged to binary weighted voltages and consequently, the resolution of the possible target voltages is binary. The paper presents the underlining theory of the proposed SCC and two new control methods to regulate the output voltage. It is shown that the theoretical formulation of the new number systems can describe many SCC circuits on the market and can help design new SCC with a larger number of target voltages. The theoretical results were verified for the binary case by simulation and experimentally. Excellent agreement was found between the theory and experimental results. The down side of the proposed SCC schemes is the relatively large number of switches which makes the approach more suitable for low power applications.**

***Index Terms*--Binary arithmetic, binary sequences, DC-DC power conversion, redundant number systems, resolution, switched capacitor, switched mode power supplies.**

I. INTRODUCTION

Switched Capacitor Converters (SCC) apply capacitors as temporary energy storage elements when transferring energy from a power source to a load. The energy transfer is accomplished by charging and discharging the so called "flying capacitors" via switches or diodes (Fig 1).

Unfortunately, SCC suffer from a fundamental power loss deficiency which makes their use in some applications prohibitive.

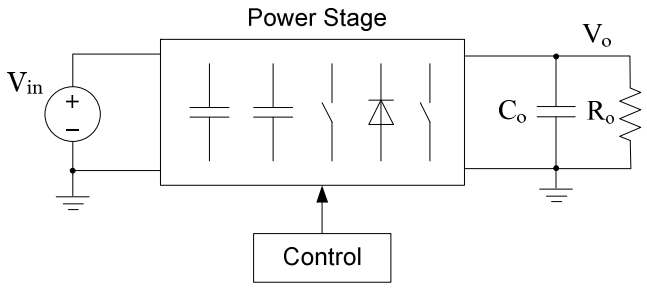


Fig. 1. The switched capacitor converter (SCC) concept.

The power loss is due to the inherent energy dissipation when a capacitor is charged or discharged by a voltage source or another capacitor. This physical phenomenon is analogous to the case of an inductor that is charged or charged by a current source. In both cases, the relevant state variable (current or voltage) will increase to infinity in the theoretical resistance-free case. In the practical case, when resistance is present in the circuit, the charging and discharging current of a capacitor will cause power dissipation. This inherent power loss in the SCC case can be modeled by an equivalent circuit that includes a voltage source (V_{TRG}) and an internal resistance (R_{eq}) as depicted schematically in Fig. 2 [1-9].

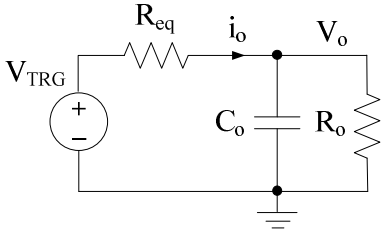


Fig. 2. The SCC equivalent circuit.

The voltage source (V_{TRG}) value is the no-load output voltage of the SCC and is equal to some multiple n of the input voltage (topology dependent) while the internal resistance (R_e) represents the losses due to the current passing through the SCC. In the model representation of Fig. 2, the losses are conveniently described as a function of the load current which simplifies the formulation of the input to output voltage ratio as well as the efficiency:

$$\frac{V_o}{V_{TRG}} = \frac{R_L}{R_L + R_{eq}} \quad (1);\ V_{TRG} = nV_{in} \quad (2);\ \eta = \frac{V_o}{V_{TRG}} \quad (3)$$

where V_{in} is the voltage of the input power source, n is the no-load voltage transfer ratio, R_{eq} is the internal resistance of the SCC, V_o is the output voltage and R_o is the load resistance.

The no-load voltage transfer ratio n of an SCC is topology dependent. That is, it is a function of the number of the flying capacitors and the way they connect to the input and output terminals and among themselves, when charging and discharging.

In general, n will be a positive or negative rational number [3].

The value of the internal resistance for the SCC was earlier derived to be [9]:

$$R_{eq} = \sum_{i=1}^{n} R_{eCi} \tag{4}$$

where each term R_{eCi} is the contribution of i-th flying capacitor defined as:

$$R_{eCi} = \sum_{j=1}^{m} \frac{k_j^2}{2C_i f_s} \cdot \left[\coth\left(\frac{\beta_j}{2}\right) \right] \tag{5}$$

where $\beta_j = t_j/\tau_j$, t_j is the length of the j-th switching duration of capacitor i, τ_j is the time constant during t_j , m is the number of switching durations of capacitor i, while the coefficient k_j is the ratio of capacitor C_i average current during switching duration j to output current.

SCC can be operated in open loop or closed loop configurations. In open loop, n and R_{eq} are fixed. In this case, the output voltage will not be regulated and will depend on V_{in} and the load resistance R_o. In this situation it is advantageous to reduce R_{eq} as much as possible to keep the efficiency high. Regulation can be achieved by either changing n or R_{eq} (or both) [10]. The no load voltage can be changed by reconfiguring on-the-fly the SCC topology and hence altering n. R_{eq} can be changed by adding resistance to the circuit e.g. by placing a linearly controlled MOSFET in the charging/discharging paths. Other possibilities to vary R_{eq} are frequency change, frequency dithering and duty cycle control [9], [11]-[13]. It is clear though, that the highest efficiency will be reached if n is manipulated such that V_{TRG} is made only slightly higher than the desired V_o, leaving a small voltage drop on R_{eq}. It is further clear that the best results can be obtained if the resolution by which n is altered is high and that its values are evenly spaced. Previous attempts to improve the efficiency of SCC by changing n on-the-fly, applied SCC configurations with limited number of target voltages V_{TRG}. Namely, with a coarse resolution of n. Consequently, the efficiency drops significantly when the required n is in between the sparsely spread values of n. For example, the commercial SCC [12] is regulated to an output voltage of 1.8V and can be switched to two conversion ratios n=1/2 and 2/3. When the input voltage is lower than about 3.5V the target voltage ratio is set to n=2/3 and for input voltage above 3.5V it is switched to n=1/2 transfer ratio. Consequently, high efficiency is observed (Fig. 3) when the input voltage is about 2.7V (1.8/(2/3)) and at 3.6V (1.8/(1/2)). In between and outside the two target voltages, the efficiency drops as the difference between the target voltage and 1.8V increases (3).

The objective of this research was to develop the theory that underlines the behavior of multi target SCC systems.

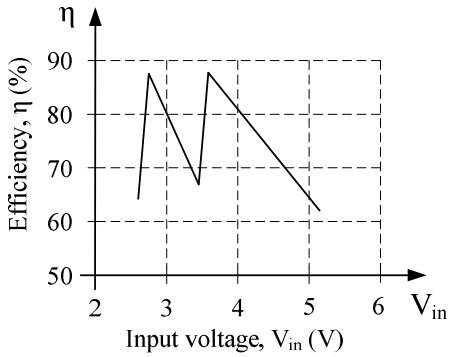


Fig. 3. The output characteristics of a commercial SCC [12] set to an output voltage of 1.8V.

Special attention was paid to SCC topologies of binary resolution. Namely, SCC systems that can be configured to have a no-load input to output voltage ratio that is equal to any binary number for the given number of bits. To this end we defined a new number system and show how these numbers can be translated into a SCC hardware that will follow the algebraic behavior. It this approach, the flying capacitors are automatically kept charged to binary weighted voltages and consequently, the resolution of the target voltages follows a binary number representation and can be made higher by increasing the number of capacitors (bits). The ability to increase the number of target voltages, reduces the spacing between them and consequently increases the efficiency when the input varies over a large voltage range.

The paper presents the underlining theory of the proposed binary SCC and its extension to the general radix case. The theoretical predictions were verified by simulation and experimental results.

II. The Extended Binary Representation

The structures of the proposed binary SCC are based on algebraic expressions that are described by the following definitions and observations.

Any number M_n in the range (0, 1) can be represented in the form:

$$M_n = A_0 + \sum_{j=1}^{n} A_j 2^{-j} \tag{6}$$

where A_0 can be either 0 or 1, A_j takes any of three values -1, 0, 1, and n sets the resolution.

For example, the code {1 0 -1 1} implies:

$$M_3 = 1 + 0 \cdot 2^{-1} - 1 \cdot 2^{-2} + 1 \cdot 2^{-3} = 7/8 \tag{7}$$

Expression (6) defines the Extended Binary (EXB) representation that is a modified version of the Binary Signed-Digit (BSD) representation [14], [15]. Unlike the conventional binary case, a number of different EXB codes can represent a single M_n value. The different codes can be generated by the spawning rule given below.

A rule for spawning the EXB codes: This procedure is iterative and begins with the conventional binary code of M_n to produce several EXB codes that represent same M_n value. Starting from any $A_j = 1$ in the code and adding (in binary arithmetic) "1" to this A_j will result in "0" in the j-th column and "1" as a carry. To maintain the original value of M_n we then add "-1" to the resulting A_j (which is zero after a "1" was added to the original "1"), generating thereby a new EXB code of same value. In short: replace a "1" by "-1" and add a "1" to the column on the left. The procedure is repeated for all $A_j = 1$ in the original code and for all $A_j = 1$ in each spawned EXB code.

The following example demonstrates how four alternative EXB codes are spawned from the binary code of $M_3 = 3/8$. The EXB codes for other fractions M_n, $n = 1\ldots3$ are summarized in Table 1. Example: The conventional binary code of 3/8 is {0 0 1 1}. This will be the starting point. In the left sequence of (8) the "1" of A_3 (the LSB) is replaced by "-1" and the "1" carry is added to A_2. The resulting code is {0 1 0 -1}. This code is later transformed (second sequence from right in (8)) to a new code {1 -1 0 -1}.

$$\begin{array}{cccc}
\overset{\downarrow}{2^0\,2^{-1}\,2^{-2}\,2^{-3}} & \overset{\downarrow}{2^0\,2^{-1}\,2^{-2}\,2^{-3}} & \overset{\downarrow}{2^0\,2^{-1}\,2^{-2}\,2^{-3}} & \overset{\downarrow}{2^0\,2^{-1}\,2^{-2}\,2^{-3}} \\
0\ 0\ 1\ 1 & 0\ 0\ 1\ 1 & 0\ 1\ 0\text{-}1 & 0\ 1\text{-}1\ 1 \\
+\ 0\ 0\ 0\ \mathbf{1} & +\ 0\ 0\ \mathbf{1}\ 0 & +\ 0\ \mathbf{1}\ 0\ 0 & +\ 0\ \mathbf{1}\ 0\ 0 \\
\hline
0\ 1\ 0\ 0 & 0\ 1\ 0\ 1 & 1\ 0\ 0\text{-}1 & 1\ 0\text{-}1\ 1 \\
+\ 0\ 0\ 0\ \mathbf{-1} & +\ 0\ 0\ \mathbf{-1}\ 0 & +\ 0\ \mathbf{-1}\ 0\ 0 & +\ 0\ \mathbf{-1}\ 0\ 0 \\
\hline
0\ 1\ 0\text{-}1 & 0\ 1\text{-}1\ 1 & 1\text{-}1\ 0\text{-}1 & 1\text{-}1\text{-}1\ 1
\end{array} \qquad (8)$$

The four alternative EXB codes, thus generated, represent of course the same fraction $M_3 = 3/8$:

$$\begin{aligned}
&\{0\ \ 1\ \ 0\ \text{-}1\} \rightarrow 0 + 1\cdot2^{-1} + 0\cdot2^{-2} - 1\cdot2^{-3} = 3/8 \\
&\{0\ \ 1\ \text{-}1\ \ 1\} \rightarrow 0 + 1\cdot2^{-1} - 1\cdot2^{-2} - 1\cdot2^{-3} = 3/8 \\
&\{1\ \text{-}1\ \ 0\ \text{-}1\} \rightarrow 1 - 1\cdot2^{-1} + 0\cdot2^{-2} - 1\cdot2^{-3} = 3/8 \\
&\{1\ \text{-}1\ \text{-}1\ \ 1\} \rightarrow 1 - 1\cdot2^{-1} - 1\cdot2^{-2} - 1\cdot2^{-3} = 3/8
\end{aligned} \qquad (9)$$

The above rule for spawning the EXB codes gives rise to two corollaries:

Corollary 1: For a resolution n, the minimum number of EXB codes for a given M_n is $n + 1$.

This is because each $A_j = 1$ in the conventional binary code with resolution n, generates a new EXB code and a carry. Furthermore, since the spawning results in the propagation of a carry, each $A_j = 0$ in the binary code, will turn into a "1", which will also be operated on to spawn a new code.

Corollary 2: For each $A_j = 1$ in the original (binary) and the spawned EXB codes of a given M_n there will be at least one $A_j = -1$ in another EXB code.

This is because the spawning procedure involves the substitution of a "1" by "-1".

III. The Generic Fractional Number Representation

Similar to the binary case given above, we define the generic sequence $N_n(r)$ of radix r in the range (0, 1) as:

TABLE 1
THE EXB CODES OF M_n, $n = 1\ldots3$.

$M_3 = 1/8$				$M_2 = 2/8$				$M_3 = 3/8$				$M_1 = 4/8$			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3
1	-1	-1	-1	1	-1	-1	0	1	-1	-1	1	1	-1	0	0
0	1	-1	-1	0	1	-1	0	0	1	-1	1	0	1	0	0
0	0	1	-1	0	0	1	0	1	-1	0	-1				
0	0	0	1					0	1	0	-1				
								0	0	1	1				

TABLE 1: CONT'D.

$M_3 = 5/8$				$M_2 = 6/8$				$M_3 = 7/8$			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3
1	0	-1	-1	1	-1	1	0	1	0	0	-1
1	-1	1	-1	1	0	-1	0	1	0	-1	1
0	1	1	-1	0	1	1	0	1	-1	1	1
1	-1	0	1					0	1	1	1
0	1	0	1								

$$N_n(r) = A_0 + \sum_{j=1}^{n} A_j r^{-j} \qquad (10)$$

where A_0 is 0 or 1, A_j takes any of the values $1-r,\ldots, -1, 0, 1,\ldots, r-1$, and n is the resolution. For example, the code {1 -2 2} for radix 3 implies:

$$N_2(3) = 1 - 2\cdot3^{-1} + 2\cdot3^{-2} = 5/9 \qquad (11)$$

Expression (10) defines Generic Fractional Numbers (GFN) representation, which is akin to the Generalized Signed-Digit (GSD) representation [16]. The private case of the GFN $N_n(r)$ where all the coefficients A_j are non-negative is identical to the representation of $N_n(r)$ in the conventional number system with the radix r (e.g. decimal). This code is called hereinafter the original code.

A rule for spawning the GFN codes: This procedure is iterative and starts from any $A_j > 0$ in the original code of $N_n(r)$. Adding "$r - 1$" to this A_j results in $A_j < (r - 1)$ and "1" as a carry. To maintain the value of $N_n(r)$ we add "$-(r - 1)$" to the resulting A_j spawning thereby a new GFN code. The procedure is repeated for all $A_j > 0$ in the original code and for all $A_j > 0$ in each spawned GFN code.

In example (12) three alternative GFN codes are spawned from the original code of $N_2(3) = 4/9$. The GFN codes for other fractions $N_n(3)$, $n = 1, 2$ are summarized in Table 2.

$$\begin{array}{ccc}
\overset{\downarrow}{3^0\,3^{-1}\,3^{-2}} & \overset{\downarrow}{3^0\,3^{-1}\,3^{-2}} & \overset{\downarrow}{3^0\,3^{-1}\,3^{-2}} \\
0\ 1\ 1 & 0\ 1\ 1 & 0\ 2\text{-}2 \\
+\ 0\ 0\ \mathbf{2} & +\ 0\ \mathbf{2}\ 0 & +\ 0\ \mathbf{2}\ 0 \\
\hline
0\ 2\ 0 & 1\ 0\ 1 & 1\ 1\text{-}2 \\
+\ 0\ 0\ \mathbf{-2} & +\ 0\ \mathbf{-2}\ 0 & +\ 0\ \mathbf{-2}\ 0 \\
\hline
0\ 2\text{-}2 & 1\text{-}2\ 1 & 1\text{-}1\text{-}2
\end{array} \qquad (12)$$

The three alternative GFN codes thus generated represent of course the same fraction $N_2(3) = 4/9$:

$$\{0\ \ 2\ \text{-}2\} \rightarrow 0 + 2\cdot 3^{-1} - 2\cdot 3^{-2} = 4/9$$
$$\{1\ \text{-}2\ \ 1\} \rightarrow 1 - 2\cdot 3^{-1} + 1\cdot 3^{-2} = 4/9 \qquad (13)$$
$$\{1\ \text{-}1\ \text{-}2\} \rightarrow 1 - 1\cdot 3^{-1} - 2\cdot 3^{-2} = 4/9$$

The spawning rule of the GFN codes brings about again the two following Corollaries:

Corollary 1: For a resolution n, the minimum number of GFN codes for a given $N_n(r)$ is $(n + 1)$.

This is because each of the $A_j > 0$ in the original code with resolution n generates a new GFN code and a carry. Furthermore, since the spawning results in the propagation of a carry, each $A_j = 0$ in the original code will turn into a "1", which will also be operated-on to spawn a new GFN code.

Corollary 2: For each $A_j > 0$ in either the original or the GFN code for a given $N_n(r)$ there will be at least one $A_j < 0$ in another GFN code of this $N_n(r)$.

This is because the spawning procedure involves the subtraction of "$r - 1$" from $A_j > 0$ and since A_j is always smaller than $(r - 1)$ the result will always be $A_j < 0$.

TABLE 2
THE GFN CODES OF $N_n(3)$, $n = 1, 2$

$N_2(3)=1/9$			$N_2(3)=2/9$			$N_1(3)=3/9$			$N_2(3)=4/9$		
A_0	A_1	A_2	A_0	A_1	A_2	A_0	A_1	A_2	A_0	A_1	A_2
1	-2	-2	1	-2	-1	1	-2	0	1	-1	-2
0	1	-2	0	1	-1	0	1	0	0	2	-2
0	0	1	0	0	2				1	-2	1
									0	1	1

TABLE 2: CONT'D.

$N_2(3)=5/9$			$N_1(3)=6/9$			$N_2(3)=7/9$			$N_2(3)=8/9$		
A_0	A_1	A_2	A_0	A_1	A_2	A_0	A_1	A_2	A_0	A_1	A_2
1	-1	-1	1	-1	0	1	0	-2	1	0	-1
0	2	-1	0	2	0	1	-1	1	1	-1	2
1	-2	2				0	2	1	0	2	2
0	1	2									

IV. TRANSLATING THE EXB CODES INTO SCC TOPOLOGIES

This section shows how EXB codes of a given M_n can be translated into sequences of SCC topologies that produce the fractional output to input ratio M_n.

Consider a step-down SCC including a voltage source V_{in}, a set of n flying capacitors C_j and output capacitor C_o, which is paralleled to load R_o. The connection of V_{in} is defined by the coefficient A_0 in each of the EXB codes for a given M_n. Irrespective of the connection of V_{in} the flying capacitors C_j are always connected serially according to the coefficients A_j in the EXB codes. The topological interconnection of V_{in}, C_j and C_o are carried out according to the following rules:

1) If $A_0 = 1$ then V_{in} is connected in a polarity that charges the output.

2) If $A_0 = 0$ then V_{in} is not connected.

3) If $A_j = -1$ then C_j is connected in series to the output in same polarity and to the input if $A_0 = 1$.

4) If $A_j = 0$ then C_j is not connected.

5) If $A_j = 1$ then C_j is connected in series with the output in opposite polarity and to the input if $A_0 = 1$.

These rules are illustrated by considering the EXB codes of $M_3 = 3/8$ (Table 1). Since n=3 we use three flying capacitors C_1, C_2, C_3. We assume in this example that C_1 is charged to $V_{in}/2$, C_2 to $V_{in}/4$, C_3 to $V_{in}/8$ and C_o to $M_n \cdot V_{in}$. Following the above rules, each EXB code for M_3=3/8 leads to a specific connection as depicted in Figure 4 that maintains $V_o = 3/8 \cdot V_{in}$.

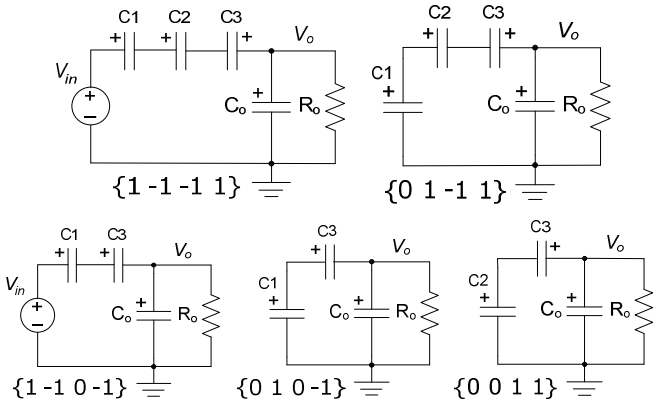


Fig. 4. Capacitors connections that follow the EXB codes of M_3 =3/8.

Since each of the 5 configuration of Fig. 4 is a one-to-one translation of the EXB code corresponding to 3/8, and assuming that the capacitors are charged to the binary fractions of the input voltage ($V_{C1}=V_{in}/2$, $V_{C2}=V_{in}/4$, $V_{C3}=V_{in}/8$ and $V_{Co}= 3/8 \cdot V_{in}$) the output will be kept at $3/8 \cdot V_{in}$, if the system cycles in perpetuity through these configurations. An intuitive explanation for this is that while the SCC switches from one topology to another each capacitor goes through a sequence of charge and discharge. This is assured by Corollary 2 which states that for each "1" in the EXB code there is at least on "-1" in the same position. This means that the theory predicts that in the EXB based SCC all capacitors are going through the sequence of charge and discharge. Moreover, as shown next, the capacitors will always reach the nominal voltages (binary fractions of the input) even from cold start when the voltages across all the capacitors are zero.

One way to prove that the capacitors will always reach the nominal voltages is to consider the fact that each configuration of the SCC for a given EXB code (e.g. Fig. 4) can be considered as an equation (Kirchhoff's Voltage Law (KVL)). By running through all the codes for the given M_n, the SCC is in fact subjecting the capacitors (including the output capacitor) to this set of equations. The SCC realization of EXB codes of a given M_n ratio requires n+1 capacitors (n flying capacitors plus the output capacitor). Consequently the set of equation has n+1 unknowns (the capacitors' voltages) and one would need at least n+1 SCC configurations (equations) to assure solvability. Since Corollary 1 states exactly that (the number of codes for a given M_n is at least

n+1), the EXB based SCC will indeed reach the expected steady state as confirmed by simulation and experimentally. This is illustrated by the following example: the KVL equations for the SCC of Fig. 4 are:

$$\begin{cases} V_{in} - V_{C1} - V_{C2} + V_{C3} = V_{Co} \\ 0 + V_{C1} - V_{C2} + V_{C3} = V_{Co} \\ V_{in} - V_{C1} + 0 - V_{C3} = V_{Co} \\ 0 + V_{C1} + 0 - V_{C3} = V_{Co} \\ 0 + 0 + V_{C2} + V_{C3} = V_{Co} \end{cases} \quad (14)$$

System (14) comprises five equations, while the number of unknowns is equal to 4, so the system has one degree of freedom. It can be solved by eliminating one of the equations yielding, as expected:

$$V_{C1} = 1/2 \cdot V_{in}; V_{C2} = 1/4 \cdot V_{in} \quad (15)$$
$$V_{C3} = 1/8 \cdot V_{in}; V_{Co} = 3/8 \cdot V_{in}$$

Since (15) is unique (the rigorous proof of this is omitted here for the sake of brevity), the capacitors' voltages are self-adjusting, so that there is no need for any control scheme [17] to assure that the capacitors reach the nominal value and hence the output will always self stabilize to the expected voltage.

Considering the fact that the set of equations (14) is solvable it should also be solvable if V_{in} and V_{Co} are switched as shown in (16). This means switching the input and output functions and in fact converting the step down SCC to a step up SCC.

$$\begin{cases} V_{Co} - V_{C1} - V_{C2} + V_{C3} = V_{in} \\ 0 + V_{C1} - V_{C2} + V_{C3} = V_{in} \\ V_{Co} - V_{C1} + 0 - V_{C3} = V_{in} \\ 0 + V_{C1} + 0 - V_{C3} = V_{in} \\ 0 + 0 + V_{C2} + V_{C3} = V_{in} \end{cases} \quad (16)$$

The solution of (16) is:

$$V_{C1} = 4/3 \cdot V_{in}; V_{C2} = 2/3 \cdot V_{in} \quad (17)$$
$$V_{C3} = 1/3 \cdot V_{in}; V_{Co} = 8/3 \cdot V_{in}$$

It is evident that the conversion ratios of the step-up EXB based SCC with the resolution *n* are reciprocal to their step-down counterparts and are defined by a set of fractions with numerator 2^n and denominators 1, …, $2^n - 1$. Note that the highest conversion ratio in this embodiment is equal to 2^n. Although a number of step-up SCC with the conversion ratio 2^n have been proposed earlier [18], [19], [20], there is no published report of SCC with intermediate binary conversion ratios.

V. Translating the GFN codes into SCC topologies

The private case of the EXB based SCC, can be extended to the general GFN fraction $N_n(r)$ case by following the concepts detailed above. However, unlike the case of the EXB, each coefficient A_j of the $N_n(r)$ will be associated with more than one capacitor. The number of capacitors associated with each coefficient will depend on the maximum number in column *j* of the GFN codes for a given $N_n(r)$. In the general case when the SCC is expected to be configured for all the values of $N_n(r)$, each column *j* will be associated with $r - 1$ capacitors. For example, for the $N_2(3)$ case each column will require (for the general case) 2 capacitors ($r - 1 = 3 - 1$) and a total of 4 capacitors (2×2). The translation of the GFN representation to the SCC topologies can be accomplished by the following rules.

1) If $A_0 = 1$ then V_{in} is connected in a polarity that charges the output.

2) If $A_0 = 0$ then V_{in} is not connected.

3) If $A_j = 0$ then all $r - 1$ capacitors C_{jx} of the group *j* are disconnected.

4) If $A_j < -1$ then $|A_j|$ capacitors C_{jx} of group *j* are connected in series with the output in the charge polarity, while the remaining *j* capacitors are connected in parallel to any of the C_{jx} capacitors in same polarity.

5) If $A_j = -1$ then all capacitors C_{jx} of the group *j* are connected in parallel and the group is connected in series with the output in the charge polarity.

6) If $A_j = 1$ then all capacitors C_{jx} of the group *j* are connected in parallel and the group is connected in series with the output in the discharge polarity.

7) If $A_j > 1$ then A_j capacitors C_{jx} of the group *j* are connected in series in same polarity and the group is connected in series with the output in the discharge polarity, while the remaining *j* capacitors are connected in parallel to any of C_{jx} capacitors in same polarity.

As an example to the relationship between GFN codes and SCC topologies we consider the case of $N_1(3) = 1/3$ and $N_1(3) = 2/3$ (one bit, r = 3), given in Fig. 5 and Fig. 6 respectively. The GFN codes for the 1/3 case are {0 1} and {1 -2} which translate into the two configurations of Fig. 5.

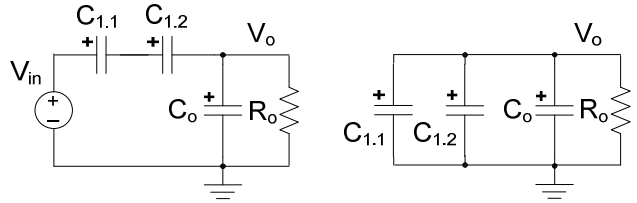


Fig. 5. Capacitors connections that follow the GFN codes of $N_1(3) = 1/3$.

Because the capacitors $C_{1.1}$ and $C_{1.2}$ are connected in parallel, their voltages are identical and are denoted as V_C. It is assumed that in steady state $C_{1.1}$ and $C_{1.2}$ keep the same voltage V_C in the series connection. The KVL equations for this case are:

$$\begin{cases} 1\cdot V_{in} - 2\cdot V_C = V_o \\ 0\cdot V_{in} + 1\cdot V_C = V_o \end{cases} \quad (18)$$

and the solution of (18) is:

$$V_o = V_C = \frac{1}{3}V_{in} \quad (19)$$

Similarly, the case of $N_1(3) = 2/3$ translates into the configurations of Fig. 6.

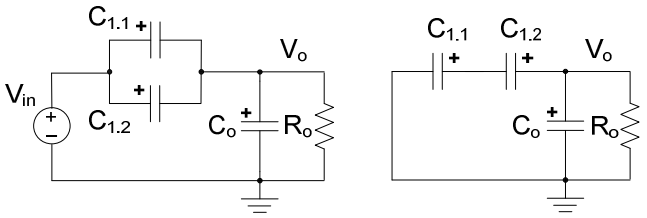


Fig. 6. Capacitors connections that follow the GFN codes of $N_1(3) = 2/3$.

Given m capacitors in the circuit, they can be rearranged by the SCC switches to follow an EXB or a GFN codes or both. For example, using one of the capacitors (or the two in parallel) of the SCC shown in Fig. 6, one can realize the EXB codes of M_1=1/2 ({0 1}, {1 -1}; radix 2). By the number of target voltages can be increased (1/2, 2/3) as implemented in the commercial SCC [12]. Moreover, using the same two capacitors, the transfer ratio 1/3 can also be added (Fig. 5) to farther increase the number of target voltages (1/3, 1/2, 2/3). Of course, this will possibly require more switches, increasing the complexity of the circuit as well as the losses [9].

VI. Output Voltage Regulation

As discussed in the Introduction, output voltage regulation of SCC is normally achieved by changing the equivalent resistance R_{eq} (Fig. 2). We propose here two alternative approaches that are compatible with the structure of the EXB or GFN based SCC. In these SCC it would be desirable to keep the voltages across the capacitors at their nominal values and not change them by partial charge or discharge. One approach to accomplish this is to use dithering that is, switching from one transfer ratio to another. In the regular one ratio mode, the converter will scan over all the codes that correspond to the desired transfer ratio. Fig. 7 depicts as an example the perpetual sequence for $M_3 = 3/8$.

For transfer ratio values which are in between the discrete M_n values one can dither between two neighboring ratios as depicted in Fig. 8.

In the case depicted in Fig. 8 the dither duration is 5 sequences, 4 of 3/8 an one of 4/8. Consequently the average ratio will be 0.4.

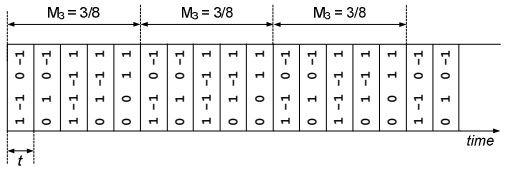


Fig. 7. SCC sequencing for $M_3 = 3/8$.

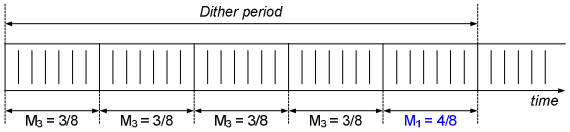


Fig. 8: Dithering between 3/8 and 4/8.

Another method proposed here for output voltage control is to introduce a linear, low dropout (LDO) voltage regulator at the output (Fig. 9). In this case, the LDO will provide the regulation for the LSB while the SCC maintains a low voltage across the LDO. It should be noted that from a theoretical point of view the efficiency is still according to (3) with or without the LDO.

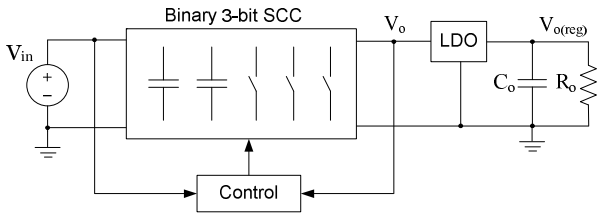


Fig. 9. Block diagram of output voltage regulation by LDO at the output.

VII. Experimental

The experimental setup followed the topology of Fig. 10 and was built around CMOS bidirectional switches MAX4678 with an 'on' resistance of 1.2Ω and a microcontroller PIC18F452, while $C_1 = C_2 = C_3 = 4.7\mu F$. For the step-down case $C_o = 470\mu F$, nominal $R_o = 3.6k\Omega$ and f_s = 100kHz; for the step-up case $C_o = 10\mu F$, nominal $R_o = 3k\Omega$ and $f_s = 12.2kHz$.

Fig. 11 depicts the experimental output voltage during startup from zero voltage across all the capacitors for M_3 = 3/8. The response to a step in the load is presented in Fig. 12. The output ripple for normal operation and when output voltage regulation was carried out by dithering is presented in Fig. 13(a) and Fig. 13(b) respectively. The SCC efficiency versus the load is given in Fig. 14 for $M_3 = 3/8$. The converter was operated also in the step-up mode with $M_3 = 8/3$. The SCC efficiency for this case is given in Fig. 15.

The concept of regulation with a LDO at the output (Fig. 9) was also tested using a LT1121-3.3 (Linear Technology) as the low dropout linear regulator with a fixed 3.3V output voltage. As shown in Fig. 9, the output and input voltages were sampled and the control was programmed to select the minimal conversion ratio which provides an output voltage greater than 3.6V. The LT1121 has a minimum dropout voltage of 0.3V, so at least 3.6V are required at the input.

This implies that the upper limit of the efficiency is limited to 3.3/3.6=0.92 and that is without taking into account the losses of the SCC. In this preliminary - proof of concept - closed loop experiment, the SCC was configured to operate both as a step-up and step-down converter. This was accomplished by introducing extra switches that could flip the input and output terminals. The measured efficiency for the input voltage range of 1.8V to 10V is depicted in Fig. 16.

The calculated values of R_{eq} according to (4, 5) [9] for the 3/8 and 8/3 cases were 9.052Ω and 63.3Ω respectively while the experimentally evaluated values were 7.35 Ω and 64.9Ω.

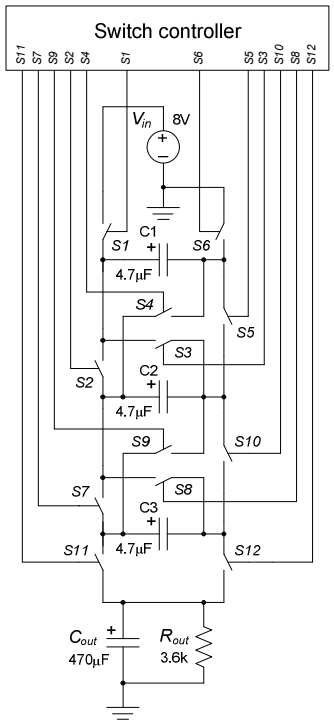


Fig. 10. Interconnection of switches and capacitors of the proposed binary SCC for *n*=3 as used in experimental setup

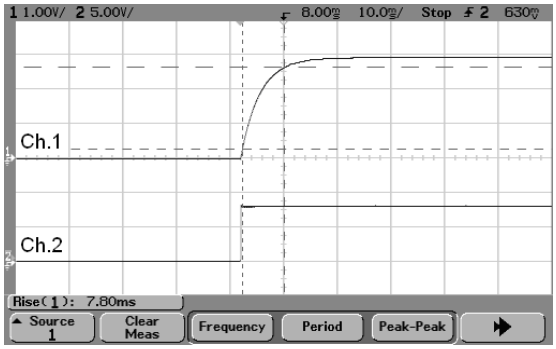


Fig. 11. Output voltage from start up. V_{in} = 8V, M_3 = 3/8, Load resistor R_o = 3.6kΩ. Vertical scale: 1V/div; Horizontal scale: 10ms/div.

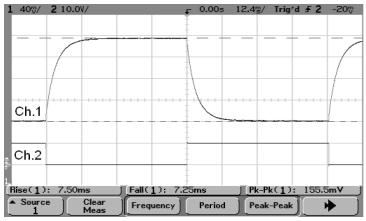
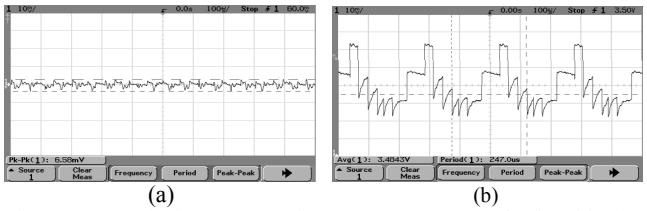


Fig. 12. Response to load (R_o) change from 3.6kΩ to 128 Ω. V_{in} = 8V, M_3 = 3/8. Vertical scale: 40mV/div; Horizontal scale: 12.4ms/div. Ch.1: output voltage, Ch.2: load step control signal. Peak to peak output voltage change is 155.5 mV.



(a) (b)

Fig. 13. Output ripple. V_{in}=8V and R_o = 437 Ω. (a) M_3 = 3/8. (b) Dithering between M_3 = 3/8 and M_1 = 1/2 (in 4:1 ratio). Vertical scale: 10mV/div; Horizontal scale: 100µS/div.

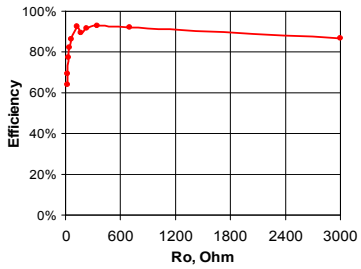


Fig. 14. Efficiency of step-down EXB based SCC, M_3 = 3/8.

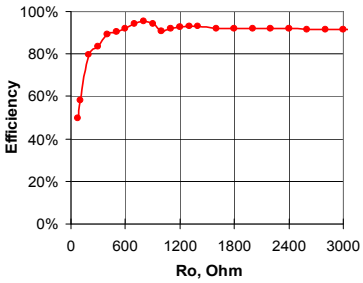


Fig. 15. Efficiency of step-up EXB based SCC, M_3 = 8/3.

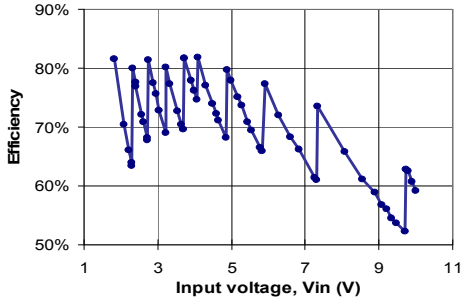


Fig. 16. Efficiency of EXB based SCC operating with an LDO at the output in both step-down and step-up modes. V_o set to 3.3V

VIII. Conclusions and Discussion

An EXB representation is proposed and extended to the general radix case defined as GFN. In the case of the EXB, the radix is 2, while the general GFN can be defined for any radix r. Hence, the case of a GFN of radix 2 { $N_n(2)$ } is in fact the EXB case. Based on the new number systems, a novel procedure is proposed for the design of high resolution multi-target SCC that emulate the EXB and GFN codes. The new theoretically supported concepts were verified by simulation and experiments for static and dynamic responses. The experiments were conducted on a step-down and a step-up SCC with binary resolution. Several control schemes were tested including linear and dithering approaches to provide continuous regulation of the output voltage. Both of the proposed control approaches were found to function properly but the dithering scheme gave rise to a higher output ripple. This could be explained by the fact that in this control method the SCC has to be reconfigured dynamically between two M_n values.

The number systems defined in this study establish the foundation of the class of SCC circuit in which the flying capacitors are self charged to some nominal value. It is shown that these SCC circuits can be considered as hardware computational systems that solve a set of equations defined by the EXB, or in general case, by the GFN representations. It is further shown that for a given number of capacitors, one can generate many target voltages by configuring the flying capacitors interconnections according to different EXB or GFN codes.

The main feature of the proposed SCC scheme is the ability to design SCC with many target voltages of high resolution. This would lead to a higher efficiency in case that the output voltage needs to be regulated while the input voltage varies over a wide range. The downside is the relatively large number of bidirectional switches required for realization.

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