Presented at the Energy Conversion Congress and Expo, ECCE-2009, pp. 1118-1125

A Heuristic Digital Control Method for Optimal Capacitor Charging

Mor Mordechai Peretz, Student Member, IEEE, and Sam Ben-Yaakov, Senior Member, IEEE
Power Electronics Laboratory
Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev
P.O. Box 653, Beer-Sheva 84105, ISRAEL.
Phone: +972-8-646-1561; Fax: +972-8-647-2949;
Emails: morp@ee.bgu.ac.il, sby@ee.bgu.ac.il ; Website: www.ee.bgu.ac.il/~pel

***Abstract* -- A digital control method for optimal capacitor charging was developed and tested by simulations and experimentally. The control algorithm follows the concept of first searching for the optimal charging conditions of the given power stage and then using the collected data in the free running operation. The major advantage of this control approach is that it eliminates the uncertainty due to parameters variations and that it can be applied to any type of capacitor charger configuration by setting the desired charging profile objectives. The method is demonstrated on a piezoelectric transformer based power stage that behaves like a resonant converter. To further increase the accuracy of the control for this resonant converter case, we applied a frequency resolution enhancement algorithm that allows fine tuning of the drive. Excellent agreement was obtained between the analytical derivations, simulations and experimental results.**

I. INTRODUCTION

Pulsed power applications such as pulsed lasers, flash lamps and defibrillators are commonly operated by short, intense, bursts of energy. This operation is normally achieved by rapidly discharging a capacitor at a pulse rate that is required by the load. Once the energy is transferred from the storage capacitor to the pulsed load, the capacitor needs to be recharged fast enough to meet the repetition rate required by the load.

The preferred method to transfer energy to a capacitor would obviously be by a power supply that behaves as a current source. This will ease the control since a voltage source charger will require tight current feedback to avoid current spikes. Another requirement of the design of a capacitor charger is the need to assure safe operation at low output voltages that prevail at the beginning of the charging phase. Furthermore, the requirement for efficient charging rate over the full span of the capacitor voltage, from zero to maximum voltage, also poses a substantial design difficulty considering the large variation of the input to output voltage ratio.

Two general topologies were proposed in the literature for capacitor charging, the flyback converter [1, 2] and the resonant converter [3-6]. Tight and rather sophisticated control is required when applying these topologies as capacitor chargers. Simple constant current charging is inefficient since the power delivered to the discharged capacitor will be very low. On the other hand, constant power charging may be dangerous as it might stress the converter, e.g. very high current at low voltage. The control challenges of a capacitor charger were met in previous studies primarily by analog circuits. For example, limiting the inrush current by sweeping the drive frequency up to a maximum value that is less than the resonant frequency [3].

Another example of a sophisticated capacitor charger control can be found in [7]. In this case the charger is built around a piezoelectric transformer that behaves like a resonant circuit. The control challenge here is to adjust the switching frequency to the resonant frequency which is a function of the (variable) capacitor voltage. Tight frequency control was achieved in this case by an analog control implementations of a phase-locked loop to assure that the system will operate at the series resonant frequency at any output voltage.

A major drawback of the earlier analog control schemes for capacitor chargers is that they require a-priori analytical knowledge of the system, that they assume that the system's parameters are constant and that the control is limited to linear operation. With the proliferation of digital control, the implementation of smart control algorithms and in particular, non-linear maximum power tracking schemes becomes viable.

The objective of this work was to explore a heuristic approach for the design of digital power tracking control of capacitor chargers. In this generic approach, the controller first maps the requirements for efficient charging, taking into account a set of constraints such as a requirement for maximum current, or maximum power but with limits on the stresses of the components. Once the mapping is accomplished off-line, the stored data is used in the actual charging sequences.

II. PROPOSED DIGITAL CONTROL ALGORITHM FOR OPTIMAL CHARGE DELIVERY

In general, maximum charge delivery to the output capacitor is limited by the maximum current that can be outputted from the power charger. However, care must be exercised not to exceed the safe limits of the power elements. For example, when driving a high Q resonant network at the resonant frequency, the high reactive current that circulates thru the system may damage the power switches. In the case of a flyback charger, the coupled inductor may not discharge (reset) from one cycle to another and the inductor current

may built to dangerous levels. In such cases, one would have to apply a set of constraints to assure rapid power transfer to the load while keeping the power charger safe [1].

In this study we defined *optimal charging* as the fastest charging rate that can be obtained while keeping the power charger under safe operating conditions.

Two general control approaches can be applied to achieve maximum power tracking. One is the perturbation based Maximum Power Point Tracking (MPPT) approach that is commonly applied in photovoltaic applications and has many variations [8-10]. The major shortcoming of this method is the need to keep perturbing the system during operation to look for the maximum point. In rapid capacitor charging, this would have to be preformed at a relatively high rate which will significantly increase the required computing power of the digital processor. In addition, the perturbation has to be quite large to invoke a significant change at the output that can properly be measured and processed by the controller. This will cause constant deviations from the optimal point. The second control approach that can be used for capacitor charging is to apply maximum power tracking that is based on the system characteristics. This can be done by either a-priory knowledge of the system behavior under various load conditions [1], or by searching for the optimal charging profile of the load. The search for the optimal charging profile can be carried out off-line prior to the operational charging sequence. The off-line search will take into account the constraints, if any, to assure safe charging. The latter, the search based heuristic approach, was adopted in this study. Fig. 1 shows the conceptual block diagram of the proposed search-and-tune algorithm.

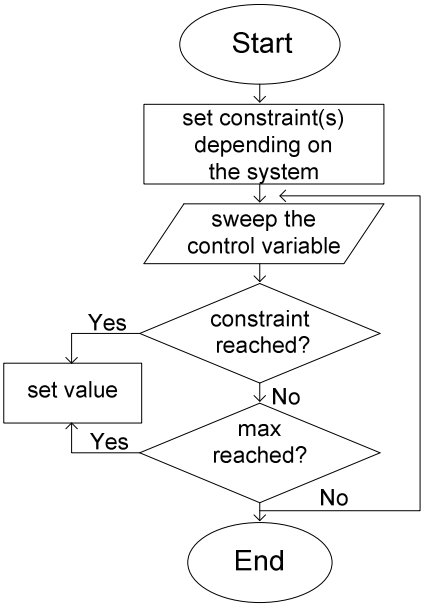

Fig. 1 Conceptual flow chart of proposed search-and-tune algorithm for generating the optimal charging profile.

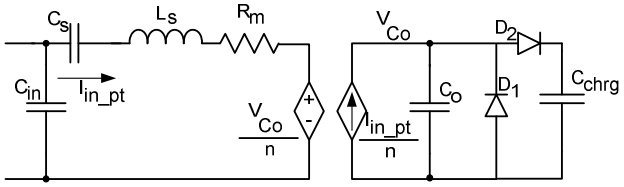

Fig. 2. Equivalent circuit of piezoelectric transformer (PT) connected to a voltage doubler rectifier.

In this work we exemplify the proposed control algorithm on a system that comprises a piezoelectric transformer (PT) that is connected at the output terminals to a voltage doubler rectifier to provide DC charging current (Fig. 2). The PT application highlights a highly challenging control task for a digital controller considering the narrow frequency operation range of the PT and consequently, the very fine frequency resolution that is needed to regulate the PT.

To apply the search for optimal charging in this application, we have set the search objective to be the highest current that can be transferred to the load at any capacitor voltage. This is a realistic target considering the fact that safe operation is theoretically expected [11] and experimentally observed at the maximum output current for any output voltage. This is due to the relatively large internal losses of the experimental PT which always maintains the output current at safe levels. The proposed control algorithm follows four basic steps:

1. Subjecting the resonant converter to sequences of frequency sweeps, where the objective in each sweep is to detect the drive frequency at which an output current peak is observed and to store the value of the frequency and the voltage of the capacitor at the instance of the current peak.
2. Setting up a look-up table of the optimal switching frequency for a given capacitor voltage value based on the optimum points information (f_s vs. V_{out}) found in 1.
3. During normal operation, sampling the output voltage and generating the required drive frequency. To increase the table accuracy for intermediate values, a linear interpolation algorithm was invoked between two neighboring cells of the table points.
4. Repeat steps 1, 2 occasionally to refresh the look-up-table. This compensates temperature drifts and other parameters variations.

It should be noted that as the frequency sweep is applied, the output voltage keeps building up which limits the number of sweeps that can be applied for a given final charging voltage. To overcome this challenge we applied an adaptive frequency range sweep algorithm. This entails frequency sweeps of narrow band around each output voltage.

The flowcharts of the search-and-tune algorithm and the main program routines are given in Figs. 3 and 4, respectively. The proposed search-and-tune routine is applying sweeps of short frequency range and looking for the maximum output current value in each sweep window. Once a maximum is detected the output voltage and the frequency that coincide with the maximum current are placed in the

look up table (LUT). This search-and-tune routine is initiated at startup and from time to time to adjust for parameters drifts (Fig. 4). The LUT thus generated is used to drive the charger during the normal charging sequence (Fig. 4). Depending on the resolution of the LUT, linear interpolation may be applied to calculate drive frequency for an output voltage value which is in between two voltages points registered in the LUT.

The LUT data collection stage and the charging operation are demonstrated in Fig. 5 which depicts the operation of the proposed control method when applied to the experimental unit of Fig. 6. During the scanning process the frequency that produced the maximum current in each frequency window is registered along with the output current. This is a relatively lengthy process (as compared to the normal charging time) since the rate of frequency change must be kept low to enable the system to softly reach the maximum charging current in each sweep. Too fast sweeps may distort the data due to the relative long settling time of high Q systems. Once the LUT is composed, the optimal charging operation can resume (the "free running" portion in Fig. 5)

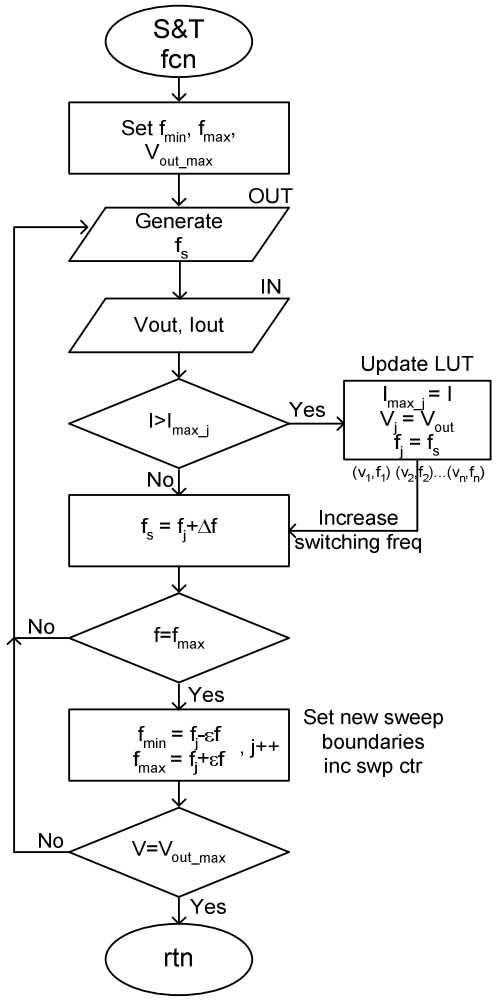

Fig. 3. Detailed flow chart of the search-and-tune routine for generating the optimal charging profile.

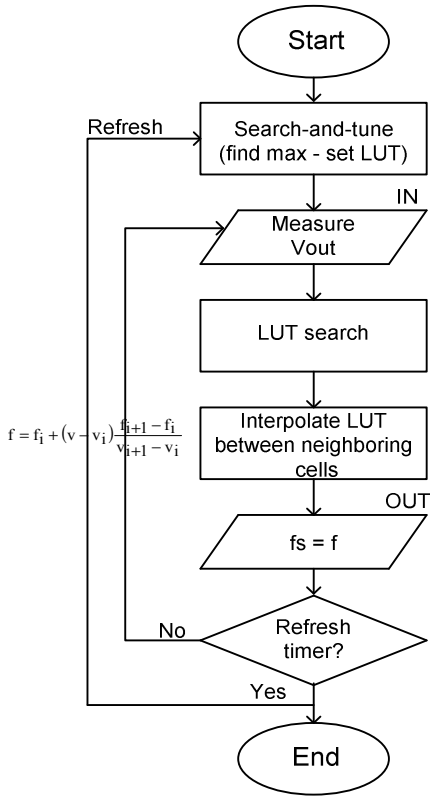

Fig. 4. Detailed flow chart of the main routine of proposed control method.

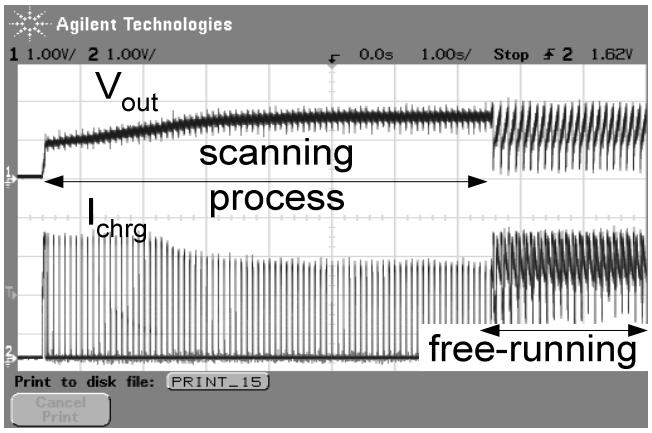

Fig. 5. Experimental results showing the concept of proposed capacitor charger control. Upper trace: output voltage 750V/div. Lower trace: Charging current 3mA/div. Horizontal scale 1s/div.

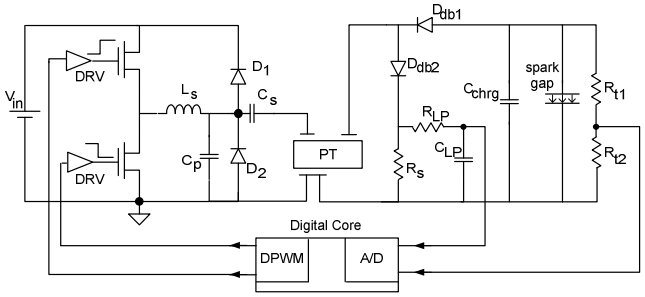

Fig. 6. Experimental setup.

A practical limitation of digital control when applied to resonant converter is the drive frequency resolution that can be achieved from the digital core. The frequency is typically generated by digital PWM (DPWM) module hardware by dividing the clock frequency. This sets a limitation on the frequency resolution that can be synthesized by a given digital controller. That is, practical digital processors are incapable of changing the frequency in fine steps as may be required when controlling a high Q resonant circuit [14]. The basic operation of frequency generation by a DPWM unit consists of a counter that is incremented every time interval that is set by the unit clock, TB_{clk}, (at the rate of the system's clock or its fraction) the counter is reset whenever the count reaches the value (N_{per}) stored in its period compare register. The generated frequency, f_{DPWM}, can be expressed by

$$f_{DPWM} = \frac{1}{N_{per} TB_{clk}} \tag{1}$$

The frequency resolution, f_{res}, is calculated as the difference between two nearest period settings (N_{per}) and (N_{per}+1)

$$f_{res} = \frac{1}{N_{per} TB_{clk}} - \frac{1}{(N_{per}+1) TB_{clk}} \approx \frac{1}{N_{per}^2 TB_{clk}} = TB_{clk} f_{DPWM}^2 \tag{2}$$

This implies that, as the operating frequency increases, the frequency resolution become rougher by the square of the operating frequency.

To overcome the resolution obstacle we applied frequency resolution enhancement algorithm [14] that is based on adaptive fractional-N dithering of the frequency generated by the DPWM modules of the digital platform. This was accomplished by dithering the DPWM period between (N_{per}) and (N_{per}+1). The "dither factor" 'n' is the number of DPWM cycles needed to achieve the desired fractional frequency. Dithering is accomplished by keeping the period constant over (n-1) DPWM cycles (denoted as base period) and then changing the last slot (n) to another period. The resultant (average) frequency obtained by this method can be calculated by

$$f_{DPWM\_dit} = \frac{1}{[(n-1)N_{per} + (N_{per}+1)]/n\, TB_{clk}} = \frac{1}{\left(N_{per} + \frac{1}{n}\right) TB_{clk}} \quad n = 1,2,3... \tag{3}$$

and the frequency resolution

$$f_{res\_dit} = \frac{1}{\left(N_{per} + \frac{1}{n+1}\right) TB_{clk}} - \frac{1}{\left(N_{per} + \frac{1}{n}\right) TB_{clk}} \approx \frac{1}{n(n+1) N_{per}^2 TB_{clk}} = \frac{TB_{clk} f_{DPWM}^2}{n(n+1)} \tag{4}$$

Fig. 7 demonstrates the improvement of frequency resolution by the Frac-N dithering method with 3-bit resolution enhancement, compared to the ordinary operating of the DPWM (as a frequency generator).

III. Analysis of Optimal Capacitor Charging by a PT Based Converter

The proposed heuristic charging control scheme and the LUT experimentally drive frequency obtained in the experiments were verified for the PT charger against values that were derived by a theoretical analysis based on an average model of the PT [11, 12]. The theoretical results thus obtained were then compared to simulation results and finally used to confirm the experimental results.

For maximum charge delivery it is desired that the operation of the PT be at the resonant frequency throughout the charge cycle. However, the output impedance that the converter "sees" is changing as a function of the voltage across the output capacitor [11, 12]. As a result, the switching frequency has to track the resonant frequency of the network which varies during the charging operation. This frequency variation was calculated by an AC equivalent circuit [11, 12] that describes the characteristics of the PT while charging a capacitor (Fig. 2).

Fig. 8 depicts typical waveforms of the voltage doubler rectifier at the output of the PT. The reflected current, I_{in_PT}/n (n is the PT transfer ratio, Fig. 2), is assumed to be a sine wave due to the high Q nature of the PT, this current flows thru the capacitor C_o during the non-conducting phase of the diodes D_1 and D_2, and passes thru the diodes during their conduction interval, θ. This interval can be calculated for a given load conditions to be

$$\theta = 2\mathrm{tg}^{-1}\sqrt{\frac{2\pi}{\omega C_o R_L}} \tag{5}$$

where R_L represents the loading conditions seen by the voltage doubler rectifier.

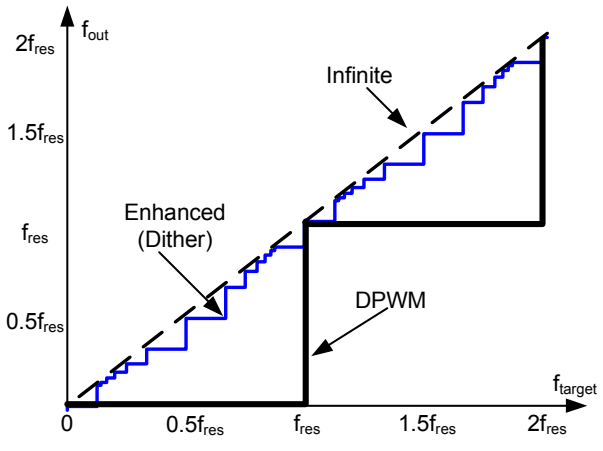

Fig. 7. Output frequency versus desired frequency for original DPWM and 3 bit resolution enhancement.

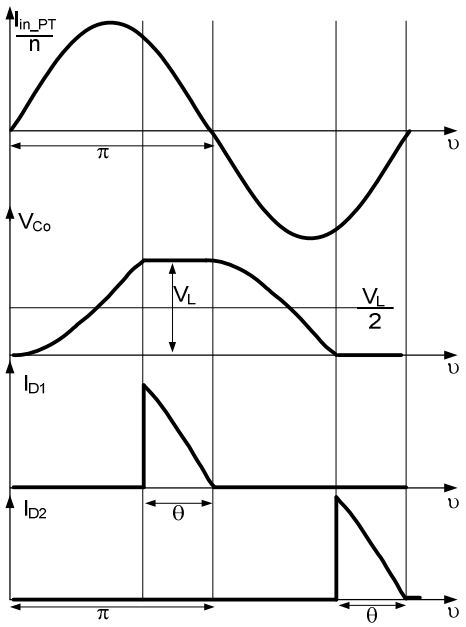

Fig. 8. Typical current and voltage waveforms of the voltage doubler rectifier fed by a piezoelectric transformer (Fig. 2).

The voltage V_{Co} is assumed to be constant during the conduction phase of the diodes (Fig. 8). In contrast, the PT output current has sinusoidal shape due to the high Q of the PT and consequently, (based on the fundamental harmonic approximation) the output power will be

$$P_{out} = \frac{1}{2} V_{Co(1)max} \frac{I_{in\_PTmax}}{n} \cos\varphi_{(1)} \tag{6}$$

where $V_{Co(1)max}$ is the peak of the fundamental harmonic of V_{Co} and $\varphi_{(1)}$ is the displacement angle between the V_{Co} and I_{in_PT}. The values of V_{Co} and $\varphi_{(1)}$ are:

$$V_{Co(1)max} = k_{(1)} (V_{Co})_{ac.pk} \tag{7}$$

$$\varphi_{(1)} = tg^{-1}\left(\frac{a_1}{b_1}\right) \tag{8}$$

where $k_{(1)}$ the voltage waveform coefficient [13]:

$$k_{(1)} = \sqrt{a_{(1)} + b_{(1)}} \tag{9}$$

$$a_{(1)} = -\frac{2}{\pi}\left[\frac{\pi - \theta + \frac{1}{2}\sin(2\theta)}{1+\cos(\theta)}\right] \tag{10}$$

$$b_{(1)} = \frac{2}{\pi}[1 - \cos(\theta)] \tag{11}$$

For a given running frequency, ω, the loaded voltage doubler configuration in Fig. 2 can be described by the RC equivalent of Fig. 9a [11-13], where the components, R_{eq} and C_{eq} (Fig. 9a) represent the impedance seen from the output terminals of the PT towards the load.

$$R_{eq} = \frac{k_{(1)}^2 R_L}{8} \frac{1}{n^2} \tag{12}$$

$$C_{eq} = \frac{tg|\varphi_{(1)}|}{\omega R_{eq}} n^2 \tag{13}$$

To simplify the analysis, the resonant network plus the load is replaced by an equivalent series network of Fig. 9b [11, 13], where R_{eq}' and C_{eq}' are the series equivalent output components, reflected to the primary side of the PT.

$$R_{eq}' = R_{eq} \frac{1}{1 + (\omega C_{eq} R_{eq})^2} \tag{14}$$

$$C_{eq}' = C_{eq} \frac{1 + (\omega C_{eq} R_{eq})^2}{(\omega C_{eq} R_{eq})^2} \tag{15}$$

The resonant frequency of the network of Fig. 9b will be

$$f_{res} = 1 \Big/ \sqrt{2\pi L_s \frac{C'_{eq} C_s}{C'_{eq} + C_s}} \tag{16}$$

where L_s and C_s are the series inductance and capacitance components of the PT model of Fig. 2.

The output voltage across the energy storage capacitor at resonance can be expressed as

$$V_{out} = 2nV_{in} \Big/ k_{(1)} \left(\cos\varphi_{(1)} + \frac{n^2 R_m}{R_{eq} \cos\varphi_{(1)}} \right) \tag{17}$$

where V_{in} is the amplitude of the input voltage to the PT and R_m is the PT's resistive element..

Applying the above equation one can calculate the resonant frequency of the loaded PT as a function of the output voltage. This can be accomplished by selecting a load resistor R_L, calculating R_{eq} and C_{eq}, and then calculating the resonant frequency and the (rectified) output voltage at the resonant frequency. Repeating this procedure for R_L values from zero to infinity, one can obtain the desired relationship between the resonant frequency and the output voltage. In these calculations, one needs to know the resonant frequency to execute (14) and (15) but this frequency is calculated only at a later stage. The problem can be overcome by iteration but since the frequency range is narrow, (14) and (15) can be calculated to sufficient accuracy by assuming a constant operating frequency.

This conjecture was verified by calculating the degree of improvement that is obtained after one iteration (Fig. 10). This examination shows that the improvement that can be obtained in one iteration is only 0.5%, consequently, the approximated approach (using constant frequency in (14, 15)) was adopted in this study.

Fig. 11 shows the analytically derived resonant frequency as a function of the output voltage, compared to cycle-by-cycle SPICE simulation of the circuit of Fig. 2. Also shown are the results of the experimental measurements. All are in good agreement.

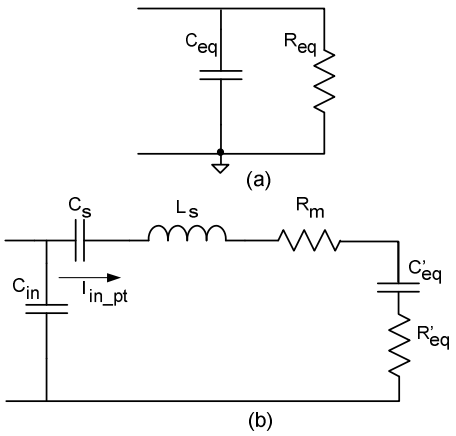

Fig. 9. (a) Equivalent RC circuit of the voltage doubler of Fig. 2 at a given frequency ω. (b) Series equivalent circuit of a PT connected to a voltage doubler.

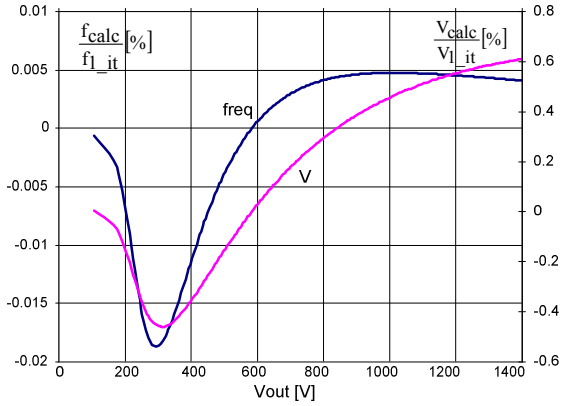

Fig. 10. Calculation improvement after one iteration for resonant frequency (16) and for output voltage (17).

The results of Fig. 11 show that the resonant frequency increases as the output voltage V_{out} builds up. This is due to the fact that when the output voltage increases the total capacitance of the network is reduced, requiring an up shift in the resonant frequency and hence in the drive frequency required to meet optimal charging conditions.

Fig. 12 depicts the optimal charging current profile that can be achieved when the drive frequency is matched to the resonant frequency. This charging profile was used to simulate the output voltage buildup as the capacitor charges. To this end, the charging scheme of Fig. 12 was curve-fitted and the resulting equation was used to define in SPICE environment a voltage dependent current source that was then connected to a capacitor (Fig. 13). The resulting charge profile (Fig. 14) shows an initial short rapid charge and then the voltage keeps building up almost linearly due to the approximate constant current. Given the capacitance value of C_{chrg}=330nF, the expected output power for the experimental PT is evaluated to be

$$P = \frac{C_{chrg}\, V_{chrg}^{2}}{2\, T_{chrg}} = \frac{350n \cdot 1500^{2}}{2 \cdot 0.13} = 3.03W \qquad (18)$$

where V_{chrg} is the final charging voltage, and T_{chrg} is the duration of the charging process from 0 to the desired V_{chrg}.

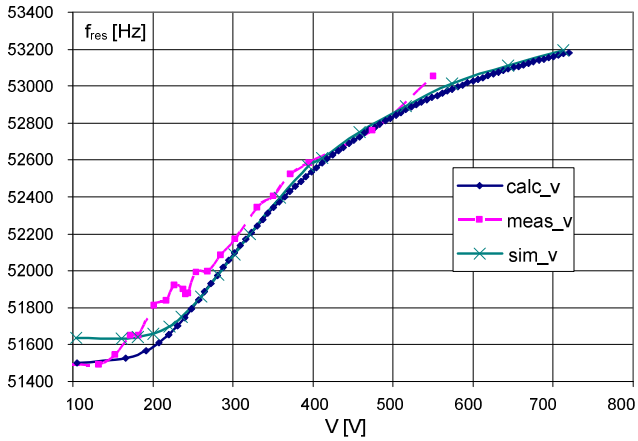

Fig. 11. Calculated, simulated and measured resonant frequency variation as a function of the output voltage.

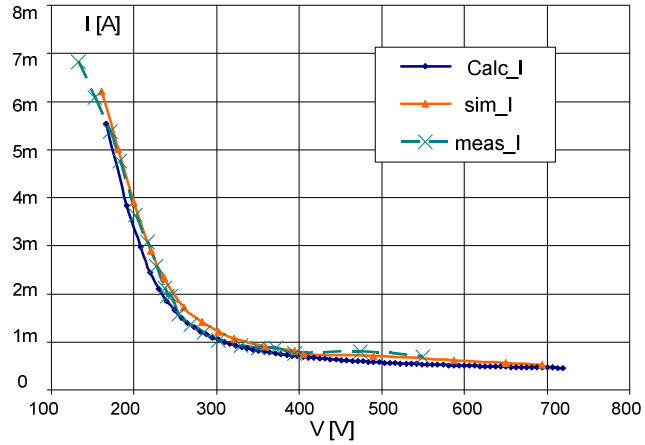

Fig. 12. Calculated, simulated and measured maximum charging current as a function of the output voltage.

IV. Experimental Results

The experimental setup is depicted in Fig. 6. It comprises PT (ELECERAM ELM-610) that was fed by a half-bridge converter, the output terminals of the PT were connected to a voltage doubler rectifier that charges the output capacitor (330nF). The input voltage was 15V and the target output voltage was 1500VDC, a spark gap was connected to the capacitor for rapidly discharge the output capacitor to demonstrate practical operation of the system. The control algorithm was implemented on a TMS320F2808 DSP. The basic frequency resolution was configured to be 1KHz to demonstrate a common microcontroller operation with modest frequency resolution operation. Fig. 15 shows the charging process by the proposed control algorithm with the basic frequency resolution of 1KHz. Fig. 16 depicts the system operation with 3bits frequency resolution enhancement on the basic 1KHz resolution case. The output power of the experimental result was 3W which matches the prediction of (18). Excellent agreement was obtained between the experimental charging process of Fig. 16 and the simulated result of Fig. 14.

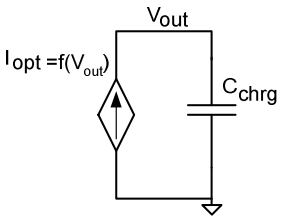

Fig. 13. Behavioral current-source model used to simulate the optimal charging process of the output capacitor.

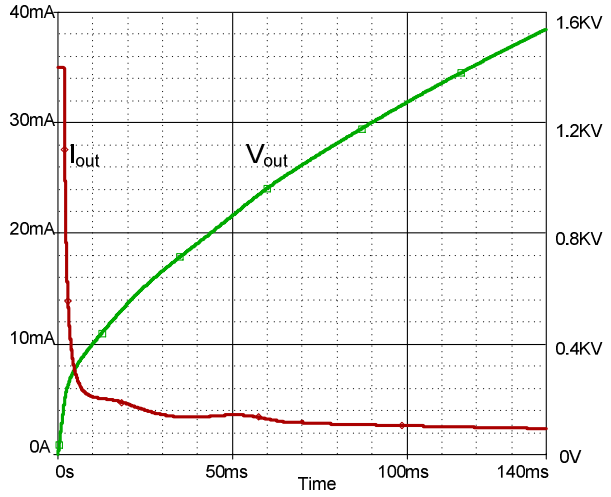

Fig. 14. Simulation results of one charging cycle obtained by the circuit of Fig. 13 – Capacitor charging current and voltage versus time.

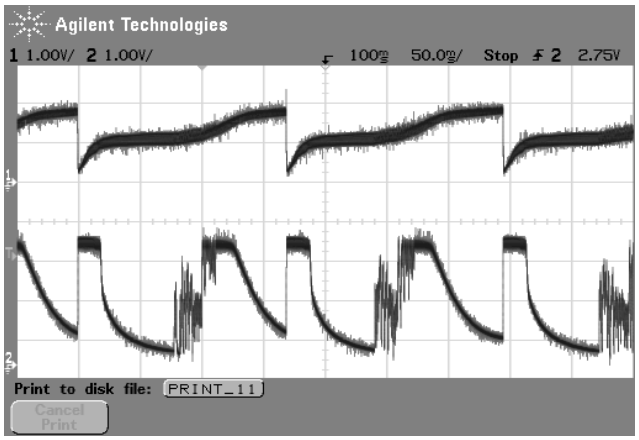

Fig. 15. Experimental results of free running operation with a frequency resolution of 1kHz. Upper trace: output voltage (750V/div). Lower trace: Charging current (3mA/div). Horizontal scale 50mS/div.

V. DISCUSSION AND CONCLUSIONS

The proposed digital control algorithm is based on the concept of maintaining the operation of the converter at optimal charge delivery conditions that are permitted for safe operation, over the entire output voltage span. This concept was exemplified on a digitally controlled PT based converter. The system was first subjected to multiple frequency sweeps and the collected data was used to construct the optimal charging profile. The resulting look-up table was then used in the free running operation. An adaptive frequency range scanning process was implemented to maximize the number of frequency sweeps that can be preformed until the target output voltage is reached. A frequency resolution enhancement procedure that is based on adaptive fractional-N dithering was applied to increase the frequency resolution of the drive generated by the digital platform.

The analysis revealed that the load impedance that the PT based converter "sees" changes as the output voltage builds up. Consequently, the resonant frequency of the converter, at which maximum output current is reached, varies as the capacitor charges. The optimal charging profile overcomes this obstacle by mapping beforehand this frequency change.

The purpose of the theoretical analysis carried out in this study is to provide an insight into the charging process and to verify the experimental results. It should be noted, though, that the results of the analytical derivations can not be used to implement a charging control scheme in practical applications. The major reason for that is that it requires accurate information of the circuit model (e.g. the PT equivalent parameters) which may significantly vary as a function of the operating conditions, temperature, aging and from one unit to another. The proposed scheme overcomes these inaccuracies by collecting the required data in-situ for optimal charging control.

The proposed control approach can be extended to any capacitor charging power stage configuration by applying the relevant constraints of the optimal charging profile during the search phase as shown in the conceptual block diagram of Fig. 1.

ACKNOWLEDGMENT

This research was supported by THE ISRAEL SCIENCE FOUNDATION (grant No. 476/08) and by the Paul Ivanier Center for Robotics and Production management.

Mor M. Peretz is supported by the Adams Fellowship Program of the Israel Academy of Sciences and Humanities.

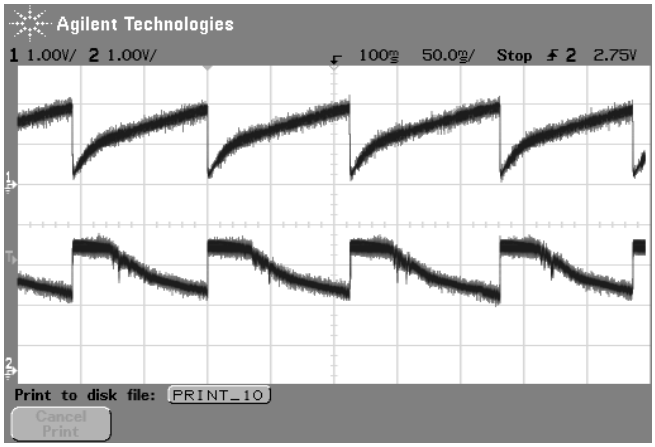

Fig. 16. Experimental results of free running operation with 3bits frequency resolution enhancement on the basic 1kHz resolution. Upper trace: output voltage (750V/div). Lower trace: Charging current (3mA/div). Horizontal scale 50mS/div.

REFERENCES

[1] N. O. Sokal and R. Redl, "Control algorithms and circuit designs for optimally flyback-charging an energy storage capacitor (e.g., for a flash lamp)," *IEEE Trans. Power Electronics,* vol. 12, 885–894, Sept. 1997.

[2] R. L. Newsom, W. C. Dillard, and R. M. Nelms, "Digital Power-Factor Correction for a Capacitor-Charging Power Supply", *IEEE Trans.* on Industrial Electronics, vol. 49, no. 5, 1146-1153, Oct. 2002.

[3] R. M. Nelms, B. E. Strickland, and M. Garbi, "High Voltage Capacitor Charging Power Supplies for Repetitive Rate Loads", *1990 IEEE Industry Applications Society Annual Meeting*, 1281-1285, May 1990.

[4] B. C. Pollard, and R. M. Nelms, "Using the series-parallel resonant converter in capacitor charging applications", *IEEE Applied Power Electronics Conference, APEC-92*, 245-252, Boston, MA, 1992.

[5] H. Zhong, Z. Xu, X. Zou, Y. Zou, L. Yang, and Z. Chao, "Current characteristic of high voltage capacitor charging power supply using a series resonant topology", *29th Annual Conference of the IEEE, IECON '03,* vol. 1, 373-377, Nov. 2003.

[6] H. Pollock, "Constant frequency, constant current load-resonant capacitor charging power supply", *IEE Proceedings - Electric Power Applications*, vol. 146, no. 2, 187-192, March, 1999.

[7] S. Ben-Yaakov, and S. Lineykin, "Maximum power tracking of piezoelectric transformer HV converters under load variations", *IEEE Trans. on Power Electronics*, vol. 21, no. 1, 73-78, 2006.

[8] M. Sokolov, and D. Shmilovitz, "Photovoltaic Maximum Power Point Tracking based on an Adjustable Matched Virtual Load", *IEEE Applied Power Electronics Conference, APEC-2007,* 1480 – 1484, Anaheim, Ca, 2007.

[9] Chihchiang Hua, Jongrong Lin, and Chihming Shen, "Implementation of a DSP-controlled photovoltaic system with peak power tracking", *IEEE Transactions on Industrial Electronics,* vol. 45, no. 1, 99 – 107, Feb. 1998.

[10] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system" *IEEE Trans. Power Electronics,* vol 16, no. 1, 46 – 54, Jan. 2001.

[11] G. Ivensky, I. Zafrany, and S. Ben-Yaakov, "Generic operational characteristics of piezoelectric transformers," *IEEE Trans. Power Electronics,* vol. 17, no. 6, pp. 1049–1057, Nov. 2002.

[12] G. Ivensky, M. Shvartsas, and S. Ben-Yaakov, "Analysis and modeling of a piezoelectric transformer in high output voltage applications," *IEEE Trans. Power Electronics*, vol. 19, no. 2, pp. 542–549, Mar. 2004.

[13] G. Ivensky, A. Kats, and S. Ben-Yaakov, "A RC-model of parallel and series-parallel resonant dc–dc converters with capacitive output filter," *IEEE Trans. Power Electronics*, vol. 14, 515–521, May 1999.

[14] M. M. Peretz and S. Ben-Yaakov,"Digital control of resonant converters: enhancing frequency resolution by dithering", *IEEE Applied Power Electronics Conference, APEC-2009*, Washington, DC, 2009.