# Digital Control of Resonant Converters: Frequency Limit Cycles Conditions

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*Abstract*- **The conditions for limit cycle oscillations in digitally controlled resonant converters were explored theoretically and tested by simulations and experiments. The analytical analysis reveals that, similar to the case of digital PWM control, limit cycles of such systems will occur when the LSB of the control is changing the output by a value that is larger than the resolution of the ADC. However, unlike the case of PWM, limit cycle oscillations is dependent on the operating point since both the power stage gain and the resolution of the digitally generated drive frequency, are not constant over the operational frequency range. Consequently, at high gains (close to resonant) the required frequency resolution may not be supported by the digital core. A time-domain simulation model, that was developed and verified experimentally, enables the steady state analysis of digitally controlled resonant converters including the limit cycles phenomenon as well as the closed loop response.**

**The proposed static analysis and dynamic modeling were verified experimentally on a series-resonant parallel-loaded converter that was operated in closed current loop. The digital control algorithm was implemented on a TMS320F2808 DSP core. Very good agreement was found between the analytical derivations, simulations and the experimental results.**

## I. INTRODUCTION

One of the major culprits of digitally controlled switch-mode converters operating in closed loop is the possible build up of limit cycles. That is, oscillations of the regulated output under steady-state operation [1-3] which results from the presence of quantizers (of the sampling and control units) in the control loop. In digital PWM control, limit cycles may appear when the LSB of the DPWM is changing the output by a value that is larger than the resolution of the ADC.

The limit cycles problem is traditionally overcome by either reducing the ADC resolution (resulting in lower regulation accuracy) or by increasing the DPWM resolution. The latter can be accomplished by reducing the switching frequency, by dithering [4], or by hardware acceleration [5].

Analogous to the case of limit cycles in digital PWM control, one might expect a similar situation when applying digital frequency control to resonant converters (Fig. 1). The main differences between the PWM and the resonant converter cases are that (a) unlike the PWM control case, where the duty ratio resolution is constant, in resonant converters the frequency resolution depends on the running frequency of the converter, and more importantly (b) that the power stage gain is not constant since it varies as a function of the frequency. These attributes of the digital control make it difficult to foresee the appearance of limit cycle oscillations in such systems. Hitherto, there is no reported treatment in the literature for limit cycles existence in frequency controlled systems.

This paper derives the conditions for limit cycle oscillations in digitally controlled resonant converters, and presents a time-domain model, that takes into account the quantization effects, to explore the static and dynamic behavior of such systems.

The results of this investigation will enable designers to foresee the conditions in which limit cycle oscillations may exist in frequency controlled converters. This could be beneficial in the selection of the frequency resolution requirements from the digital hardware and can lead to the development of smarter control techniques for such systems.

## II. STATIC ANALYSIS OF LIMIT CYCLES

The key criterion for determining the existence of limit cycle oscillations in digitally controlled switching converters relies on the comparison between the LSB values (i.e. resolution) of the ADC and the output signal variation due to a LSB change of the control [1, 6]. That is, operation with no-limit-cycles will be assured when the variation of the output due to LSB change of the control, $\Delta_{Sout}$, is smaller than the resolution of the ADC $\Delta_{ADC}$:

$$\Delta_{S_{out}} < \Delta_{ADC} = \frac{V_{ADC}}{2^{N_{ADC}}} \quad (1)$$

where $V_{ADC}$ and $N_{ADC}$ are the ADC reference voltage and number of bits of the ADC, respectively.

In the present static analysis of digitally controlled resonant converters (a typical block diagram is shown in Fig. 1) we assume that the system operates under steady state conditions. It is also assumed that the digital compensator (control law) adds no quantization error to the control loop (due to numerical truncation). Hence, two quantizers can be identified in the system of Fig. 1: the ADC and the digital to frequency converter.

In this work we demonstrate the proposed analysis approach on a digitally controlled series-resonant parallel-loaded converter (Fig. 2), where the object of the control is to regulate

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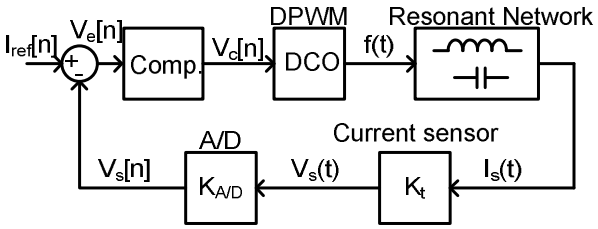


Figure1. Block diagram of a digitally controlled resonant converter

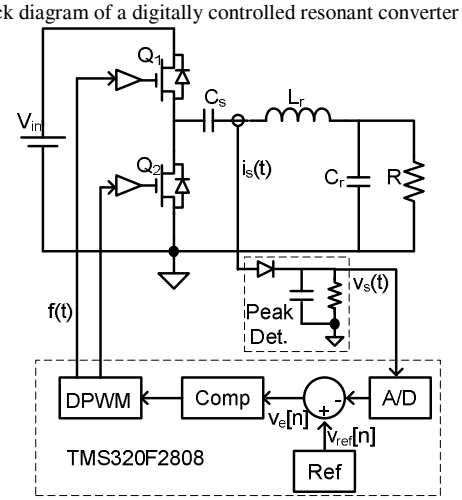


Figure 2. The experimental digitally controlled series-resonant parallel-loaded converter.

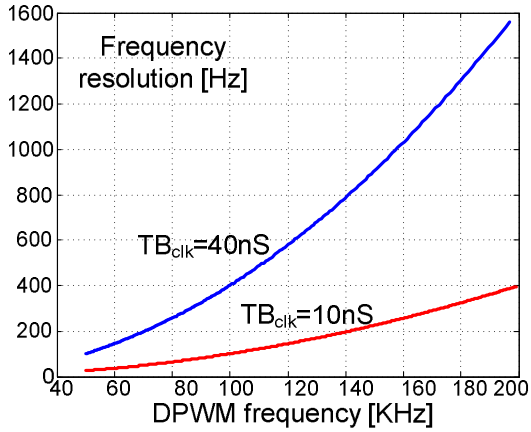


Figure 3. Frequency resolution as a function of the running frequency of typical DPWM unit for two cases of clock frequency.

the resonant current. To this end, the current is first sensed (converted to voltage), rectified and then fed to the digital controller for compensation.

Digital generation of frequency is normally carried out by timers that are programmed to reset at a desired value while maintaining a fixed 50% duty ratio. This is conventionally realized by a DPWM which is operated as digitally controlled oscillator (DCO). The generated frequency can be expressed by

$$f_{DPWM} = \frac{1}{N_{per} TB} \qquad (2)$$

where $N_{per}$ is an integer and TB is the time base of the unit clock.

The frequency resolution can be calculated as the LSB change in $N_{per}$

$$\Delta f_{DPWM} = \frac{1}{N_{per} TB} - \frac{1}{(N_{per}-1)TB} \approx \frac{1}{N_{per}{}^2 TB} = TB f_{DPWM}{}^2 \qquad (3)$$

Considering (3), one finds that the frequency steps of the DPWM are limited by the system clock frequency and are increased by the square factor of the operating frequency (Fig. 3). This implies that a system could be free of limit cycle oscillations at one drive frequency but may exhibit oscillations when operated at higher frequency due to poor resolution.

The next step is to determine the gain of the resonant network as a function of frequency. The normalized impedance of the resonant tank of Fig. 2 and the resonant current [7] are given by:

$$|Z(j\Omega)| = \left|\frac{Z_P(j\Omega)}{Z_r}\right| = \sqrt{Q^2 + \left(\Omega - \frac{1}{\Omega^2}\right)^2} \qquad (4)$$

$$|i_S(j\Omega)| = \left|\frac{V_{in}}{Z(j\Omega)}\right| = V_{in} \Big/ \sqrt{Q^2 + \left(\Omega - \frac{1}{\Omega^2}\right)^2} \qquad (5)$$

where Q is the network's quality factor, $\Omega=f/f_r$ is the deviation of running frequency from the resonant frequency and $V_{in}$ is the normalized input voltage.

Fig. 4 shows the well known frequency response of the resonant current of (5). The small signal frequency to current gain of the power stage can be calculated by taking the derivative of (5)

$$G_{if}(\Omega) = \frac{di_S}{df} = \left|\frac{V_{in}}{Z(j\Omega)}\right| = -2V_{in}\left(\Omega - \frac{1}{\Omega}\right)\left(1 + \frac{1}{\Omega^2}\right) \Big/ \left[Q^2 + \left(\Omega - \frac{1}{\Omega^2}\right)^2\right]^{\frac{3}{2}} \qquad (6)$$

The result of (6) is depicted in Fig. 5 which shows the local gradient of the resonant current gain as a function of the operating frequency of the converter. It is observed that the system is less sensitive to frequency variations near the resonance peak and at frequencies that are far from $\Omega=1$. This implies that at these ranges of operation, the conditions for no-limit-cycle of (1) can be satisfied with coarser frequency steps than it would require when operating at $1.2\Omega$ where the slope of the function is highest.

Multiplying (6) by (3) and taking into account the input voltage value and the current sensing gain ($k_t$), the resonant current (output signal) gain to frequency variations of the DPWM can be expressed as

$$\Delta i_S = G_{if}(\Omega)\Delta f_{DPWM}(\Omega) V_{in} k_t \qquad (7)$$

The criterion for no-limit-cycles operation for this system can now be established by rewriting (1)

$$\Delta i_S < \Delta_{A/D} \quad \Rightarrow \quad G_{if}(\Omega)\Delta f_{DPWM}(\Omega) V_{in} k_t < \frac{V_{ADC}}{2^{N_{ADC}}} \qquad (8)$$

Fig. 6 maps the areas in which limit cycle oscillations exist for the system of Fig. 2. The curves of Fig. 6 demonstrates two operation cases, one with constant frequency steps (dashed line) and the other (solid line) with frequency resolution of an actual

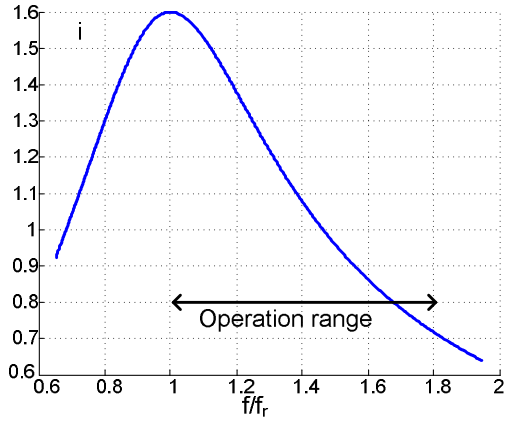


Figure 4. Normalized frequency response of the power stage of Fig. 2.

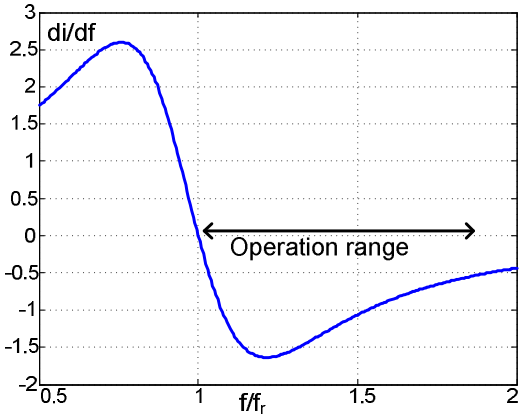


Figure 5. Normalized frequency sensitivity of the resonant current.

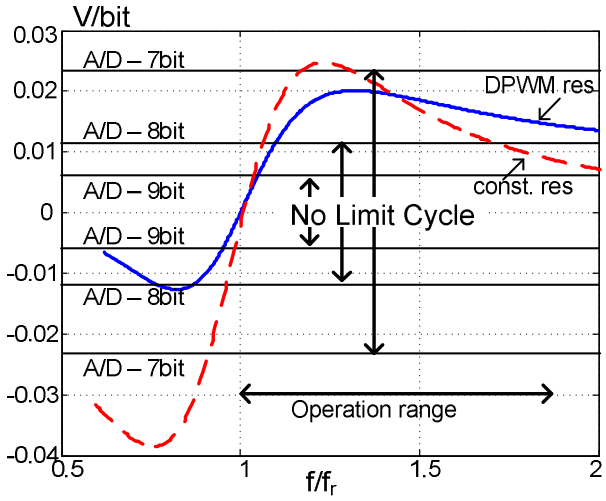


Figure 6. System frequency sensitivity. Map of no-limit-cycle operation conditions for the system of Fig. 2

DCO realized by a DPWM unit. The validity of (8) was tested by a dynamic model of a digitally controlled resonant converter that is developed in the next section.

## III. Dynamic Model

The functional block diagram of the system (Fig. 1) was the basis for the dynamic model construction. The concept of the modeling methodology was to distinguish between dynamic sub units that can be treated as linear transfer functions (TF) and static non-linear units where the input to output ration is non-constant [8]. In the following we present the details of the time-domain simulation model developed (Fig. 7).

### A. *Resonant power stage:*

As was shown in the previous section, the value of the resonant current of the converter depends on the operating frequency (Fig. 4). The resonant tank is considered to respond instantaneously to changes of the frequency when compared to the control loop bandwidth and thus its effect on the system's dynamics can be neglected. Therefore, the functional relationship of this block can be described by the frequency to current TF of (5) which is realized in the simulink model (Fig. 7) as a frequency dependent gain by the 'MATLAB fcn' block.

### B. *Digital control law:*

This block generates the control command c[n] to the DCO as a function of the error, e[n] of a reference value and the measured output. In this work a discrete-time PI control law [9] was applied, that is

$$c[n] = c[n-1] + ae[n] + be[n-1] \tag{9}$$

where 'a' and 'b' are the compensator's coefficients.

It should be noted that the response time of the control law is in the range of system response, therefore this block will be described as a discrete-time linear TF with inherent sampling rate from the ADC.

### C. *Current sensor:*

To regulate the amplitude of the resonant current, a peak detector was applied (Fig. 2). The low-pass action of the detector adds some phase lag to the control loop. This block is modeled as a continuous-time TF of the form

$$\frac{v_S}{i_S}(s) = \frac{k_t}{RCs+1} \tag{10}$$

where R and C are the low-pass filter components.

### D. *Digitally controlled oscillator (quantizer):*

The purpose of this block is to convert the digital value produced by the control to a frequency signal. The behavior of this block is modeled by a gain block that includes quantization action [6]. In this work we realized the frequency gain and resolution by the static relationship obtained in (2) and (3). The frequency limiter (Fig. 7) was added to ensure the proper operation range of the system as was carried out in the experimental unit (e.g. above the resonant frequency).

### E. *Analog to digital converter (quantizer):*

This block converts the continuous-time output to a digital value. It can be conventionally modeled by a gain plus quantization action. The sampling delay was taken into account by a discrete-time unit delay which was also used to specify the sampling rate of the digital section.

Following the above approach, a time-domain simulink model was constructed (Fig. 7). Figs 8 to 10 show some results that validate the proposed modeling approach and the static

analysis. Simulations were run for different ADC resolutions and current reference settings showing both the dynamic behavior of the system and the operation in steady state. The simulation results were found to be in excellent agreement to the limit cycles condition derivations of (8) and Fig. 6.

An interesting insight into the system's operation that supports the static analysis can be gained by the simulation results of the model. Taking Fig. 10 as a reference, it can be observed that limit cycles exists when the ADC is set to a resolution of 8bits and the system attempts to regulate a current value of 1.2 (arbitrary units). This is due to the high gain at 1.3Ω operating frequency (Fig. 4) that is required to achieve this output level. Indeed from the results of the static analysis (Fig. 6), the condition of (8) for no-limit-cycles is indeed not satisfied. However, when a lower current value is called for (which will require higher operation frequency of about 1.7Ω), the criterion set in (8) is satisfied and the oscillations ceased.

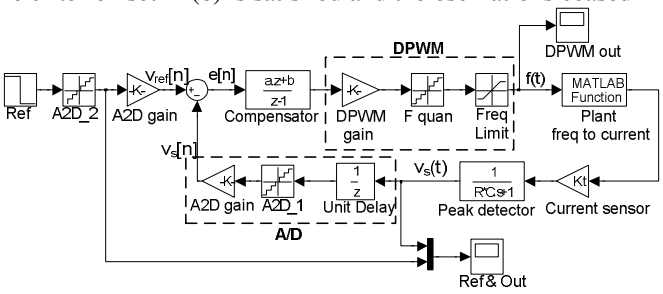


Figure 7. Behavioral simulink model

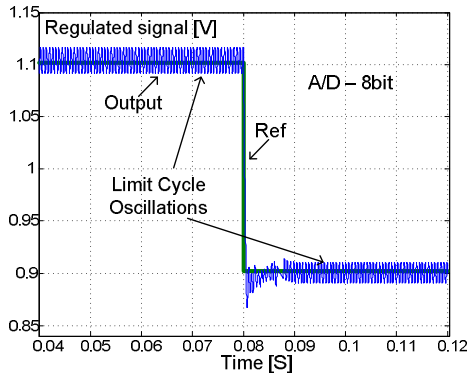


Figure 8. Simulation results of the model of Fig. 7 for a step of current amplitude from 1.1 to 0.9 (arbitrary units), ADC level of 8bit. Limit cycle oscillations.

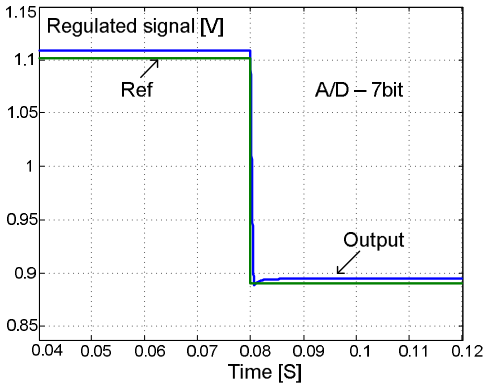


Figure 9. Simulation results of the model of Fig. 7 for a step of current amplitude from 1.1 to 0.9 (arbitrary units), ADC level of 7bit. Free of limit cycle oscillations.

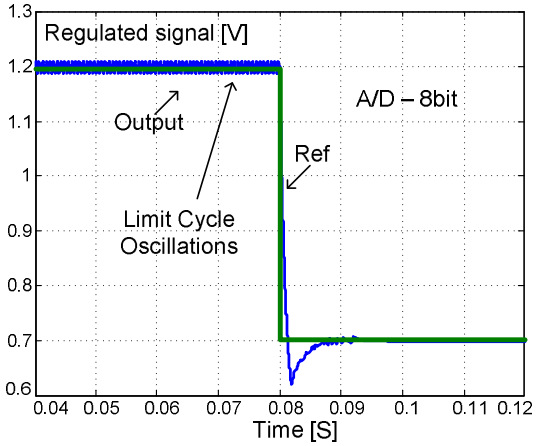


Figure 10. Simulation results of the model of Fig. 7 for a step of current amplitude from 1.2 and 0.7 = ADC level of 8bit. Limit cycle oscillation at 1.2 and no oscillations at 0.7.

## IV. Experimental Verification

To verify the analytical derivations and the simulation model, the resonant converter of Fig. 2 was built and tested experimentally. The digital control algorithm was implemented on a TMS320F2808 (TI) DSP core.

Throughout all the experiments the compensation control law and sampling rate were kept without change, while changing the ADC levels and attempting to regulate different current values. The frequency operation range was limited to operation above the resonant frequency (80KHz≡1Ω to 145KHz≡1.8Ω) to assure ZVS operation of the power switches. The frequency resolution of the frequency generator (DPWM unit) was set to maximum by the digital hardware which was between 11bit at lower frequencies (around the resonant frequency) and 9bit at higher frequencies.

Figs. 11 and 12 verify the proposed criterion and analytical results of limit cycles conditions in such systems. The figures show the rectified output signal (ADC input) when attempting to regulate the resonant current amplitude to 0.15A by the system with 9bit ADC (Fig. 11) and 7bit ADC (Fig. 12).

A further verification of the proposed criterion (eq. 8, Fig. 6) was obtained by mapping the limit-cycles occurrences in the experimental circuit. The results, which are summarized in Table I, were found to be in very good agreement with the analytical prediction (Fig. 6 solid line).

## V. Discussion and Conclusions

In this work the conditions for no-limit-cycles operation of digitally controlled resonant converters were explored. It was found that the limit cycles criterion of PWM operation is insufficient in this case since both the frequency resolution and the power stage frequency to current gain are strongly dependent on the system's operating frequency at any given instance. This stems from the facts that the frequency resolution is decreasing by a square factor of the frequency increase and that the small signal power stage gain changes as a function of the operation frequency. A new criterion for limit-cycles conditions was derived for such systems based on

TABLE I
EXPERIMENTAL LIMIT-CYCLES MAP OF THE SYSTEM OF FIG.2. THE RESULTS CORRESPOND TO THE SOLID LINE OF FIG. 6.

| Current [A] | frequency | 10bit | 9bit | 8bit | 7bit | 6bit |
|---|---|---|---|---|---|---|
| 0.175 | 90k (1.15) | LC | LC | LC | LC | No LC |
| 0.15 | 100k (1.3) | LC | LC | LC | No LC | No LC |
| 0.138 | 110k (1.4) | LC | LC | LC | No LC | No LC |
| 0.11 | 120k (1.55) | LC | LC | LC | No LC | No LC |
| 0.0875 | 135k (1.8) | LC | LC | No LC | No LC | No LC |

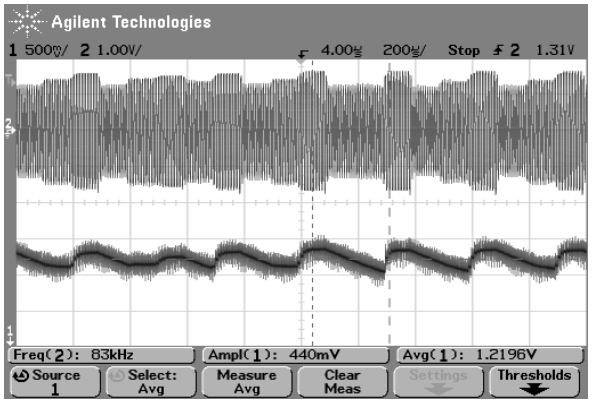


Figure 11. Experimental results of the converter of Fig. 2. For current amplitude at 0.15A with 9bits ADC, limit cycles. Upper trace: resonant current 0.2A/div, lower trace: peak detector output 0.5V/div. Horizontal scale 200µS/div.

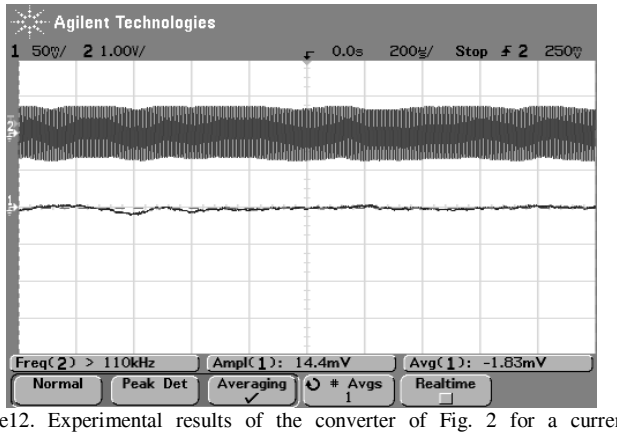


Figure12. Experimental results of the converter of Fig. 2 for a current amplitude of 0.15A with 7bits ADC. Stable steady state operation. Upper trace: resonant current 0.2A/div, lower trace: peak detector output 50mV/div. Horizontal scale 200µS/div.

static analysis at steady state. The analytical model is capable to foresee the existence of limit cycles for all the operation range of the system. Simulation and experimental measurements validated the accuracy of the model. The dynamic behavioral simulation model of the system that was developed enables one to view the transient operation of the system as well as the operation in steady state (including limit cycling phenomenon).

It was found in this study that the conditions for limit cycles of these systems are largely dependent on the power stage characteristics and in particular, the resonant system's quality factor. This is observed in Fig. 5 that shows that the frequency locations of the sensitivity peaks are around the resonant frequency and by examining (6) which implies that these peaks are a function of Q and that they are getting closer to the network's resonant frequency.

The implication of this insight on the closed-loop operation of such systems is that regulation of high Q resonant tank in frequency regions that are relatively far from the resonant frequency requires modest frequency resolution to avoid limit cycles. However, when attempting to regulate the same system around resonance, the requirements of resolution will be much higher.

One of the major obstacles in the design of digitally controlled resonant converters is the limited frequency resolutions capabilities that can be attained by simple microcontrollers. This limitation may affect the control accuracy and make the system more prone to limit cycle oscillations. One solution to this problem is to increase the resolution by frequency dithering as proposed in [4].

The no-limit-cycles criterion that was derived points out not only to the importance of high resolution frequency generation but also to the significance of the operating point which determines the local gain.

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