DESIGN and APPLICATIONS OF A UNIVERSAL POWER MANAGEMENT MIXED-SIGNAL SoC CONTROLLER (UPMC) PLATFORM

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I.   INTRODUCTION

This paper presents engineering application examples of a Universal Power Management mixed-signal SoC Controller (UPMC) for digital control and management. The UPMC controller platform was designed with the vision of allowing the complete migration path from analog to digital control in applications in which the advantages of the digital technology prevail. To this end, the UPMC includes in the design the blocks that are crucial for the implementation of universal digital power control and management systems. The UPMC is suitable for a broad range of applications common to the power conversion industry, including: Power Supplies for Telecom, Computers and Peripherals, Consumer Electronics, Merchant switch-mode power systems (SMPS) and charges, Lighting, Motor Control, Building & Home Automation, Automotive, etc. The first part of the paper describes the design concept of the UPMC and the tools for parameter configuration and storage while the second part describes 4 UPMC applications: a networked electronic ballast for lighting including a digital PFC (Power Factor Correction) control function, a single chip for power control and management of a mobile PC, full control and management of a Line Interactive Uninterruptible Power Supply (UPS) and a multiphase DC/DC converter.

Traditionally, digital control of SMPS was accomplished by applying a general purpose Digital Signal Processor (DSP). Attempts were made to use DSPs to carry out the digital control algorithm, housekeeping, supervisory tasks and communication. Apart from some limited applications, this approach is unsuitable in most industrial instances due to its many drawbacks and limitations. These include: the single arithmetic unit that limits the speed of computation resulting in a limited control bandwidth, excessive delays in a multi converter case, limited capabilities to generate non-sequential pulse as might be needed in non linear control, limited capabilities to achieve high resolution of the output driving signal and its degrading as the number of control channels increases, as well as other shortcomings.

Another approach to modern digital power management is a closed, dedicated controller for a specific application such as Voltage Regulator Module (VRM). The drawback of this approach is the fact that it is limited to the specific application for which it was developed. Hence, application of the unit to solve other power management problems is impossible since a new Application Specific Integrated Circuit (ASIC) design cycle needs to be initiated for every case.

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The UPMC (Fig. 1) developed by Systel Development & Industries Ltd., and already implemented in silicon, was conceived to overcome the limitations of the general purpose DSP approach on the one hand and the limitations of the specialized ASIC solutions on the other.

II.   THE UPMC [1].

In general, the Universal Power Management SoC Controller (UPMC) is the set of programmed and reconfigured hardware modules that specializes in control of the front-end multi-channel switch-mode power systems (SMPS) and their outside world communication.

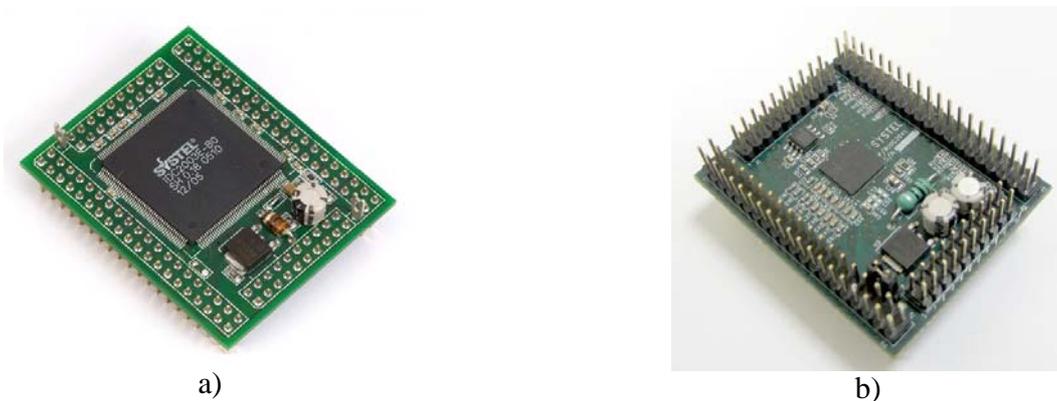a)   b)

Fig.1 The UPMC (a) IDC2003E engineering device and (b) the commercial IDC2040 device mounted on a daughter board for test purposes.

The UPMC modules are functional-packed into three main units: control unit, interface unit and central processing unit (CPU) (Fig.2). The UPMC has 24 analog inputs that provide the multi-channel sampled-data feedback and 58 general purpose (10 Schmidt-triggered) configurable digital inputs/outputs (I/Os). The UPMC core is powered by 1.8V and 3.3V power supplies.

Control unit
The control unit architecture serves as a universal platform to design a single or multi loop control circuit. A key feature is that each control loop accomplishes the task of the highly tailored controller independent of the others, and works in parallel at a device clock rate up to 200MHz. The present silicon implementation of the UPMC named IDC2000 (Integrated Digital Control) includes a device family of up to 11 independent control loops and pulse sequence generators implemented in hardware. This feature overcomes the bottleneck of a single processor that may limit the computing power required for the closed loop control algorithms (for one or more channels) and produces performance figures that are tens of times better than those of the equivalent state-of-the art DSPs.

Another important feature of the UPMC is the ability of each loop to serve the dual control function. First, it achieves design objectives for load and line regulation and dynamic response in closed-loop control mode. Second, it modifies parameters of control loop on-the-fly during the

design stage or during normal operation, to change the working regime while power circuit is operating.

Each control loop can realize various methods of non-linear and linear closed-loop control. The choice of control methods (voltage mode, average and peak current modes) as well as scheme of control (single or multi-loop) is driven solely by the problem to be solved.

The UPMC includes an analog front-end (AFE) and digital Custom Logic modules. Their interconnection can be flexible and modified to suit control method and scheme of control circuit. In general, the control loop is powered through the common AFE Module followed by individual Digital Filter blocks (Proportional-Integral-Differential-Feed-Forward [PIDF] Module) and individual Pulse Sequence Generator blocks (PSG Module) (Fig.2).
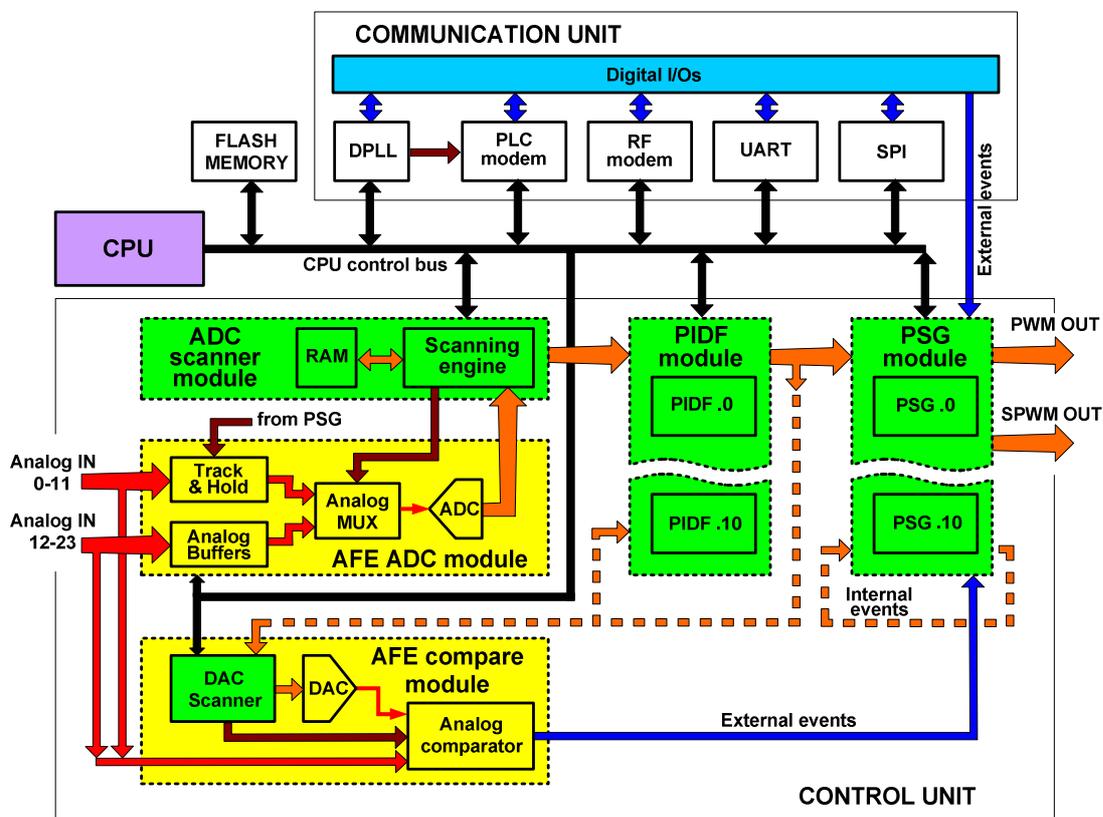

Fig. 2 UPMC High-Level Block Diagram of the IDC2080 (the larger version of the IDC2000 family)

Analog Front-End Module
The main functions of the AFE module are to execute analog-to-digital conversion of analog feedbacks and digital-to-analog conversion of reference signals. For these purposes the AFE module comprises two sub-modules: Analog to Digital Converters (ADC) Module and Analog Compare Module.

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The ADC Module uses ADC cell fed through analog multiplexer (MUX) to digitize analog feedback and analog parameters arriving from analog inputs. Control of ADC Module and storage of converted data is performed by ADC Scanner module. It is a memory-based unit that uses an over-sampling method, thus the required signals are stored in a RAM and are ready to be used by each and every PIDF channel and/or also by CPU. ADC Scanner module is used to scan the ADC analog inputs, by using flexible scanning sequences, and is configured by CPU. Track & Hold devices in ADC Module are used for time related sampling and enable analog measurements at a precise timing referring to PSG switching signals.

The Analog Compare Module (ACM) is meant for magnitude comparison between analog input and reference signals. It includes the analog comparator used to generate analog external events for control of PSG module. This module can be used for the control of the inner loop of "current mode control" power supplies. The programmable analog voltage references are provided by the CPU or alternatively by the PIDF optionally combining with digital saw tooth from PSG via (Digital to Analog Converters (DAC). Selection of the source of the reference is served by programmable DAC Scanner.

PIDF Module
The heart of UPMC are integrated Digital Filters (PIDF Module). It includes 11 hardware implemented programmable control loop PIDF controllers that relieve the central processor from heavy computational task of the control algorithm. Each PIDF controller is a control unit that performs the numeric calculations required to close a digital control loop. The calculations normally use variables such as a reference signal (generally invoked by a CPU) and various feedback signals fed from the controlled circuit of the application (external feedback signals) through the AFE module. The output of PIDF module is data sent to PSG module. Each PIDF controller has all of the proportional, integral, differential gain, and feed forward elements (feed forward to anticipate the affects of sudden input changes). The PIDF is also capable of performing linear interpolations of CPU written reference points in order to generate various types of controlled waveforms. PIDF module is configured by means of the CPU.

Pulse Sequence Generator
The PSG module is an event driven engine generating configurable pulse sequence drive signals for a switching mode machine (power supply, motor driver, UPS, ballast, etc.). Each transition in the pulse sequence signal is dictated by an "external event" or an "internal event". The external event source is outside the IDC and is received typically from a power section. Examples of external events are: voltage zero cross, current zero cross, current threshold cross in current mode control, etc. Internal events are generated inside the IDC and define the duration time of intervals in a pulse sequence signal.

An internal event dictates the end of the time intervals (or pulse sequence segments) that have constant value or calculated value. For example, the PIDF module dictates the interval that has a calculated value (can also be called "loop controlled" value). The pulse sequence configuration is established by means of the CPU at wake up as with the other modules. The configuration establishes the interval that has a constant value (the value can be changed on-the-fly) using configurable state machine. The internal event is generated by digital comparison of timer value

to digital data derived from a digital comparator or by timer overflow. The interval value (duration time) is equal to the division of the digital data by the timer configurable clock frequency.

The programmability of the PSG module structure enables control of the timer operation in relation to the requested pulse sequence group. Each pulse sequence signal generated includes one or more look up tables (LUTs) for its configuration. Each row (address) of a LUT defines one state of the configurable state machine and generates one interval of the pulse sequence signal. Consecutive intervals are generated by consecutive rows (addresses). Therefore, the number of the intervals is equal to the number of the states. The maximum possible number of states in a pulse sequence signal is 16.

CPU

The present version of UPMC comprises on-board CPU module that performs the supervision and general management of low frequency tasks. It functions mainly as the system manager, rather than control loop controller: it coordinates, monitors, protects and assists in complicated numerical calculations. The CPU delivers the configuration parameters to the UPMC modules during the initialization process.   In addition, it delivers parameters for on-the-fly modification of the control unit configuration, setting of reference levels for the control loops, managing PSG module. The CPU also controls interface with the flash memory and various digital I/O ports and is involved in the communication management mechanism.

Communication unit

The UPMC on-board communication unit is intended for support of the remote and/or centralized management of the various power equipments through shared communication network. To support a wide range of modern communication technologies the UPMC includes for power management purposes the following embedded communication modules: Power Line Carrier (PLC), RF, UART. Support of other communication standards (like DALI) is achieved by software.

To enable jitter-free synchronization of various processes to the utilities "Power Line" the UPMC includes the Digital Phase Locked Loop (DPLL) module. It serves mainly as a packet synchronization means for the PLC communication but can be used for other applications (UPS, etc.).

A trade off between performance, power consumption and cost lead to the capabilities summarized in Table I below.

Function	IDC2080	Function	IDC2080
PSG Clock Frequency	200MHz	PSG (pulse sequence generator)	Configurable On-the-Fly
PSG Switching Signal Resolution	5 nS	PSG Pulse Sequence	Responding to external and/or internal events
Average PSG Signal Resolution by Dithering	0.17nS	Number of PSG's outputs	22 (11 complementary outputs or software controlled)

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PSG Pulse Duration – Max # of bits	12	PSG/Modulation Control Method	Flexible Sequence – PWM, FM, or any combination
Minimum Pulse Width	26.5nS	Number of Analog Inputs	24+3 internal (for temp. and VDD measurement)
Maximum Pulse Width	22.2mS	Digital I/O	58 (10 schmidt-trigger inputs)
Minimum Control Calculation Updating Time	170nS	Analog Input Resolution	10 Bit
Control Functions	By PIDF logic engines	Analog Input Sample – Effective Rate	Up to 12MHz flexible sharing its time resources between inputs by priorities
Minimum Total Control Latency	900nS		
External Event Minimum Latency	150nS (current mode)	PSG Frequency	1500kHz/12 Bit 3000kHz/11 Bit 5000kHz/10 Bit (Using dithering)
PSG- # of states per cycle	Configurable, up to 16 states		
Wake Up Time	80mS	Analog Compare Module	24 channels

Table I Basic capabilities of the IDC 2080

Example of a Parameter Design Tool in Lighting Applications – PDK-3-L
To help OEM designers harness the universality and immense flexibility of the UPMC to a specific application, obviously there was a need to develop design tools that will enable the OEM user to configure the architecture of the UPMC. To this end Systel developed the Parameters Development Kit (PDK) and in particular for the fluorescent lamp applications the specific (PDK-3-L) version that is dedicated to serve multi-channel ballast applications, that comprises the PFC stage and up to 8 independent channels of the half-bridges fed resonant circuits.

The PDK is a user-friendly Graphical User Interface (GUI) design tool that allows the designer to configure the UPMC in accordance with selected power topology, control algorithm, type of lamps and desired communication interface. The following is a list of functions carried out by the PDK:

- selection of the UPMC configuration parameters set that defines interconnection between different custom logic blocks and the control algorithms
- design of PIDF digital filters parameters for control of PFC stage and power stage in different operation modes (preheating, ignition, dimming, turn-off)
- development of power stage parameters for dimming mode (switching frequency, maximum and minimum light output)
- create or choose lamp operation curves (light vs. current) from library

- support the manual mode for on-the-fly adjustment of configuration parameters
- configuration of PLC module for communication interface
- new application having the same power topology, control algorithms and similar power level of an existing design (project) - the designer needs to only modify the original set of parameters

Figure 3 below are screen shots of the PDK design tool showing some of the functions at the designer's disposal.
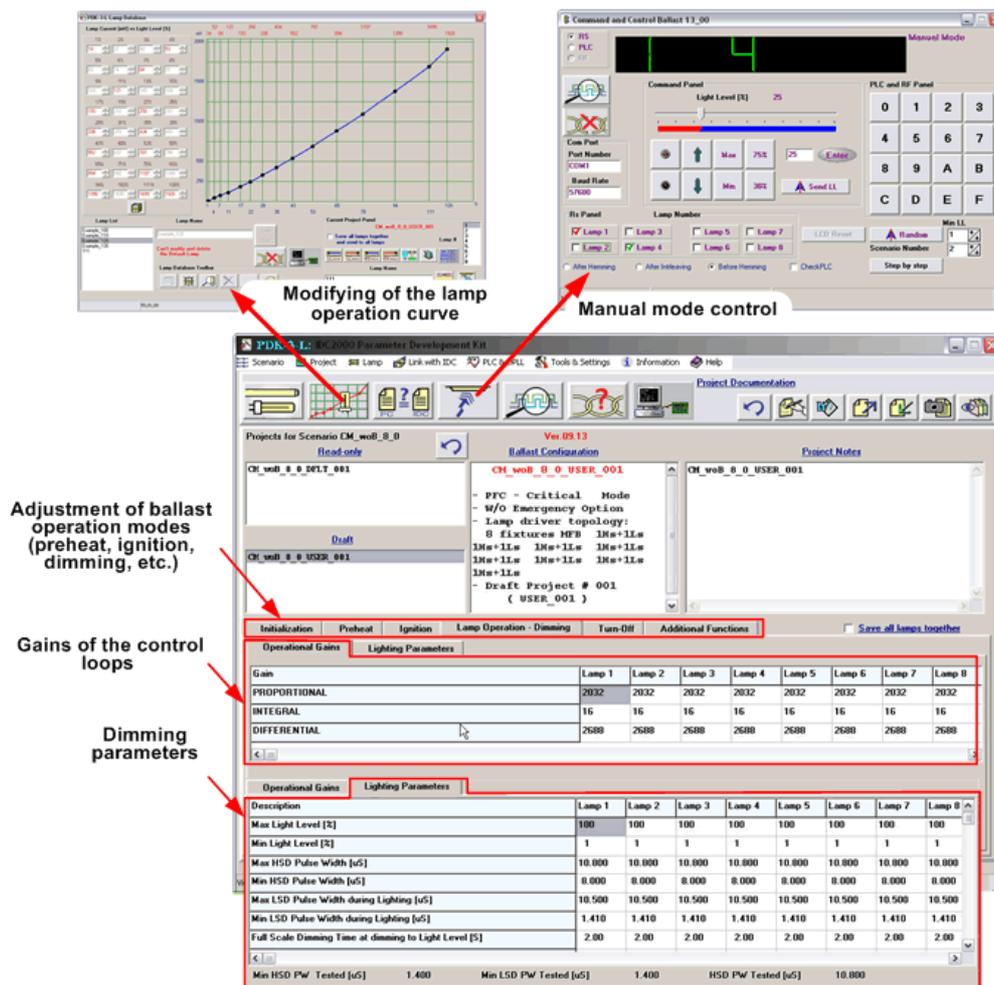

Fig.3 The set of main PDK-3-L screens that support basic configuration functions

In summary, tuning of the end product characteristics can be accomplished without a change of capacitors, resistors and/or magnetics and without code programming the desired specifications during the development stage of the end product. The PDK allows design of a large variety of dimmable and regular electronic ballast models with any type of standard fluorescent lamps.

III. Lighting Application [2]

The first application example of the UPMC to be discussed is a networked electronic ballast system. In this example, the IDC2000 is used as a central control unit of a Multi-Channel Ballast for two main power topologies configurations. One based on Independent Half Bridges (Fig.4), a second, based on Common High Side - Multi Low Side Half-Bridge (Fig.5).

The abilities of the **Multi-Independent topology** (Fig.4) include: (a) individual remote access to lamp/s or fixtures, (b) individual drive and protection of each half-bridge and lamp/s, (c) lamp/s connected to each channel to be separately dimmed to different levels, shutdown or switched on and (d) connection of different lamp types and power to each channel

The abilities of the **Common High Side topology** (Fig.5) include: (a) Uniform and equal dimming of all the lamp/s or fixtures, (b) Separate protection of each half-bridge, lamp/s, (c) Individual remote control access monitoring of each lamp/s and (d) Individual remote shut down or switch on of each lamp/s
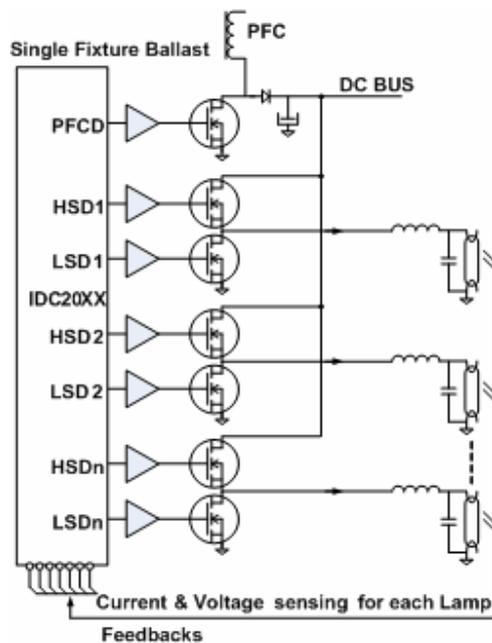

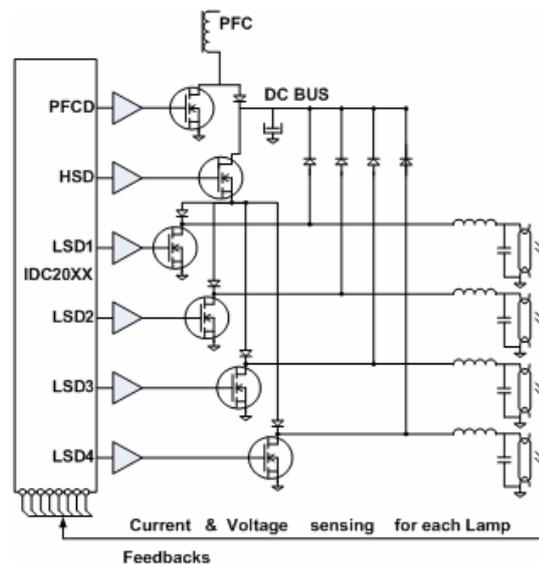Fig. 4 Multi-Channel Ballast based on Multi-Independent Half Bridges

Fig. 5 Multi-Channel Ballast based on Common High Side - Multi Low Side Half-Bridge

Test results of a 200W reference ballast (Fig.6) based on the Independent half Bridges configuration are shown in Figures 7 and 8 which present the voltage and current traces of the lamp during all a complete programmable start-up process when lighting the lamp to high light level and to a very low light level (0.5%) respectively. The UPMC allows the designer to comprehensively modify and tune the programmable start-up process according to his own solutions to meet standards and market requirements.

The PFC stage of the aforesaid multi-channel 200W ballast utilizes a Step-Up Boost Converter operating at critical mode and changing to a discontinuous mode at no load. This converter is controlled by digital PFC control algorithm [3] implemented by the same UPMC. Achieved performances for different loads are presented in Figure 9. The measured THD of input current at 100% and 25% of load is 2% and 2.4% respectively. These results were obtained with a line voltage having 1.5% THD.
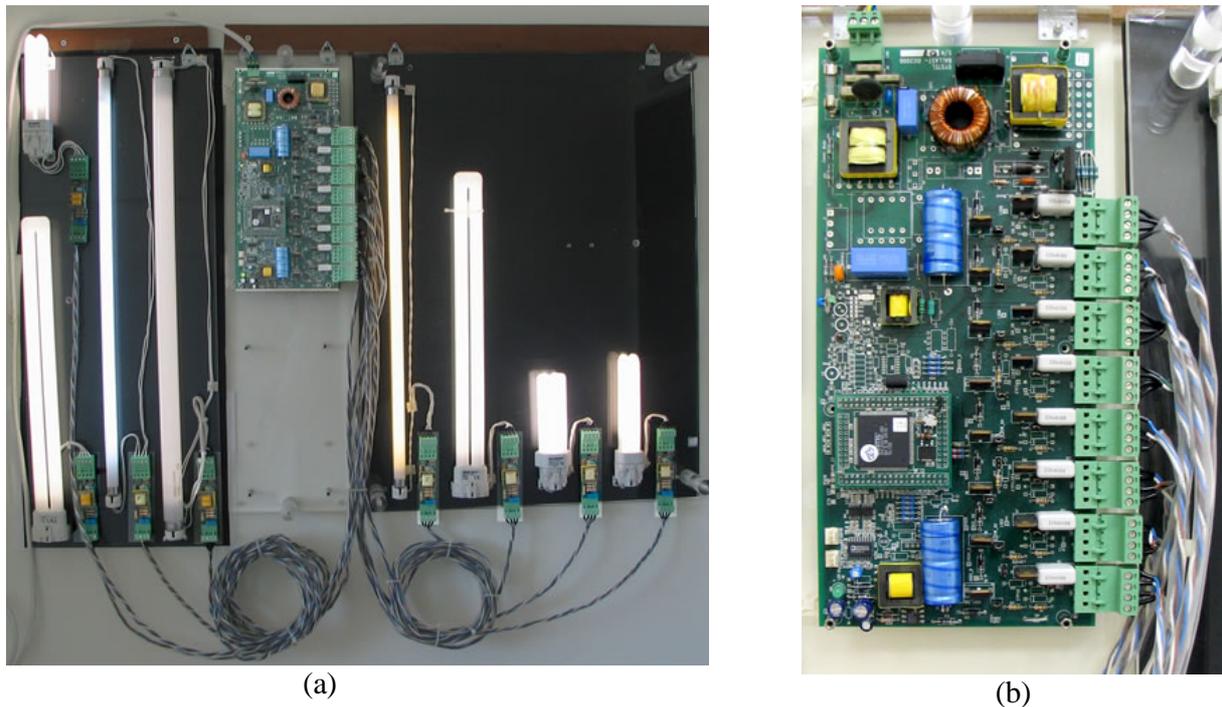

(a)

(b)

Fig. 6 Systel's Lighting Evaluation Kit. (a) An 8-channel ballast reference design board, powered by the IDC2003E Engineering device, driving 8 different types of lamps both in power and shape. Each channel drives lamps at different dimming levels. (b) Detailed picture of the reference design board based on multi-independent half bridges configuration.
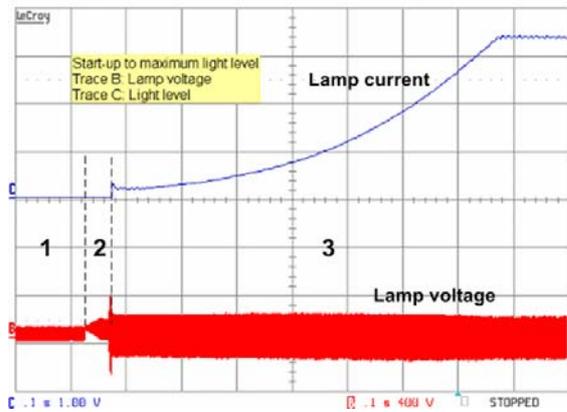
Fig.7 Preprogrammed start-up of fluorescent lamp: preheat (section 1), current trace depicts no light and voltage trace depicts low lamp voltage; ignition (section 2) of the lamp to ignition light level; gradual increase (section 3) of the light (current trace) from ignition level to the maximum. Horizontal scale 100mSec/div.
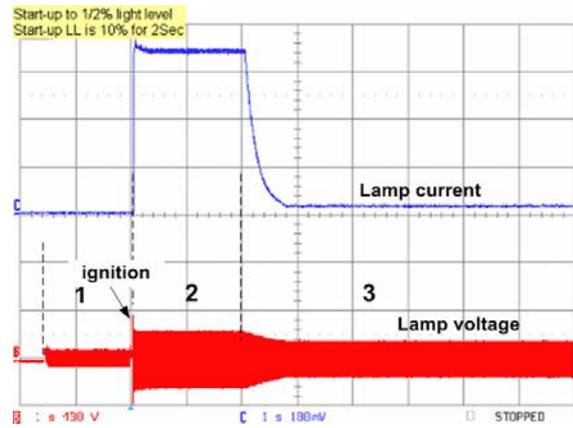
Fig. 8 Start-up of the fluorescent lamp to very low light level (0.5% of the maximum). The algorithm includes preheat (section 1), ignition to pre-configured "Ignition light level" (10% of the maximum) and holding this light level for pre-configured (2 Sec) "ignition LL time"(section 2), dimming to required light level (section 3). Horizontal scale 1 Sec/div.

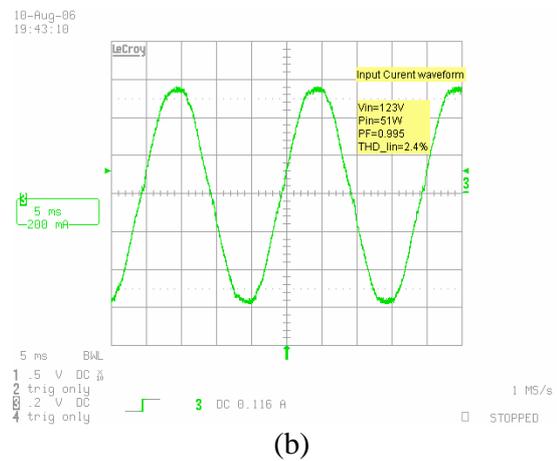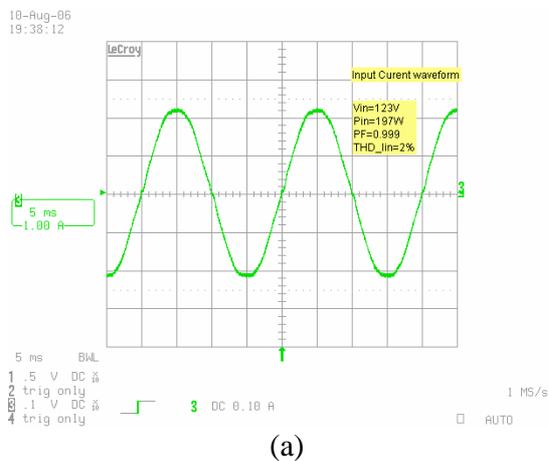(a)   (b)

Fig. 9 The line current of a power factor corrected 200W multi-channel ballast for fluorescent lamps powered with a single UPMC: (a) at full 100% light level (b) at 5% - 10% light level

IV. The PC Application

The following figure depicts an application of the UPMC controller envisioned for a mobile computer. This is an integral concept which supplies within a single chip solution all the voltage regulation channels, the analog and digital I/Os and the requested communication interfaces.

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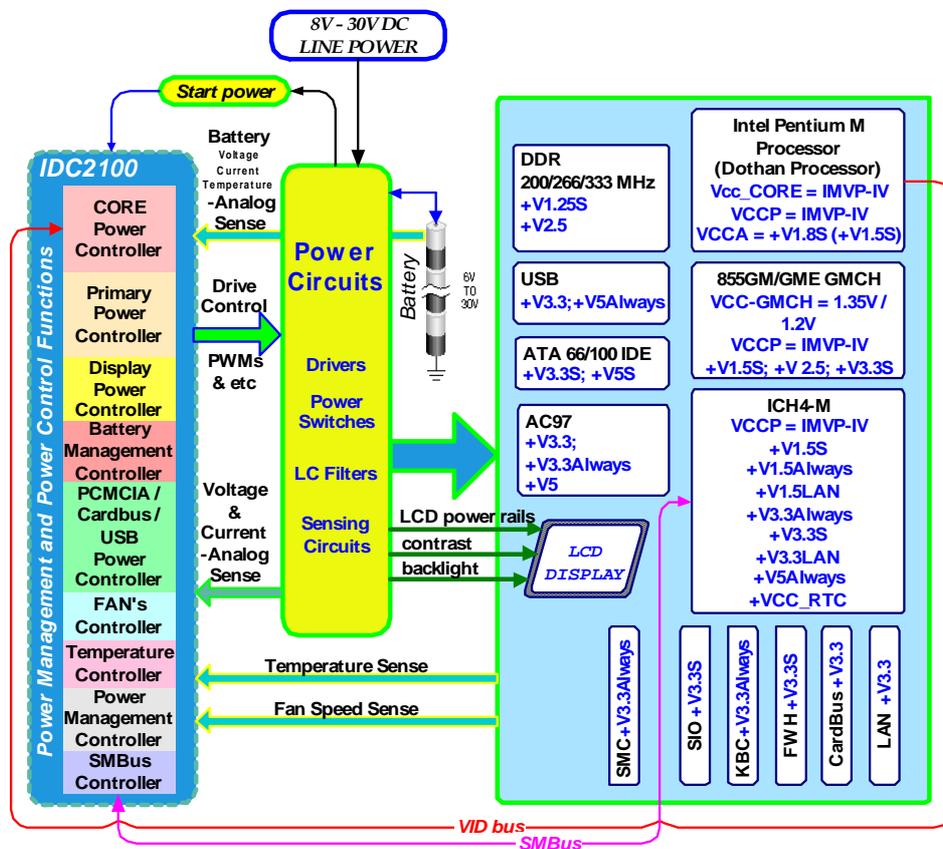by Eytan Rabinovitz, Arie Lev and Sam Ben-Yaakov

Fig. 10 IDC2100 Integration Concept for Power Management and Control in Mobile Systems

In particular, the controller in this application has capability to support a multiphase synchronized buck converter to drive the CPU. In this respect, Figure 12 shows a block diagram of this converter for a particular case of a four phase application driven by the UPMC.

V. Enhancing a Line Interactive Uninterruptible Power Supply with the UPMC

The following block diagram (Fig.11) shows a line interactive UPS powered by a controller of the IDC2000 family devices providing a high-speed, cost effective solution.

This solution provides superior performances showing high dynamic response and stable sine wave with low THD. A unique fast transition from mains to batteries is achieved by means of the DPLL module comprised in the UPMC. This DPLL, in combination with the high resolution control provided by the UPMC, allows a precise mains voltage measurement and an excellent phase lock to mains with a 10µSec time window for zero cross detection. This, together with an output sine wave always being synchronized to mains, allows a smooth transition from battery to mains and vice versa without any harmful overshoots or undershoots at any load type and conditions.
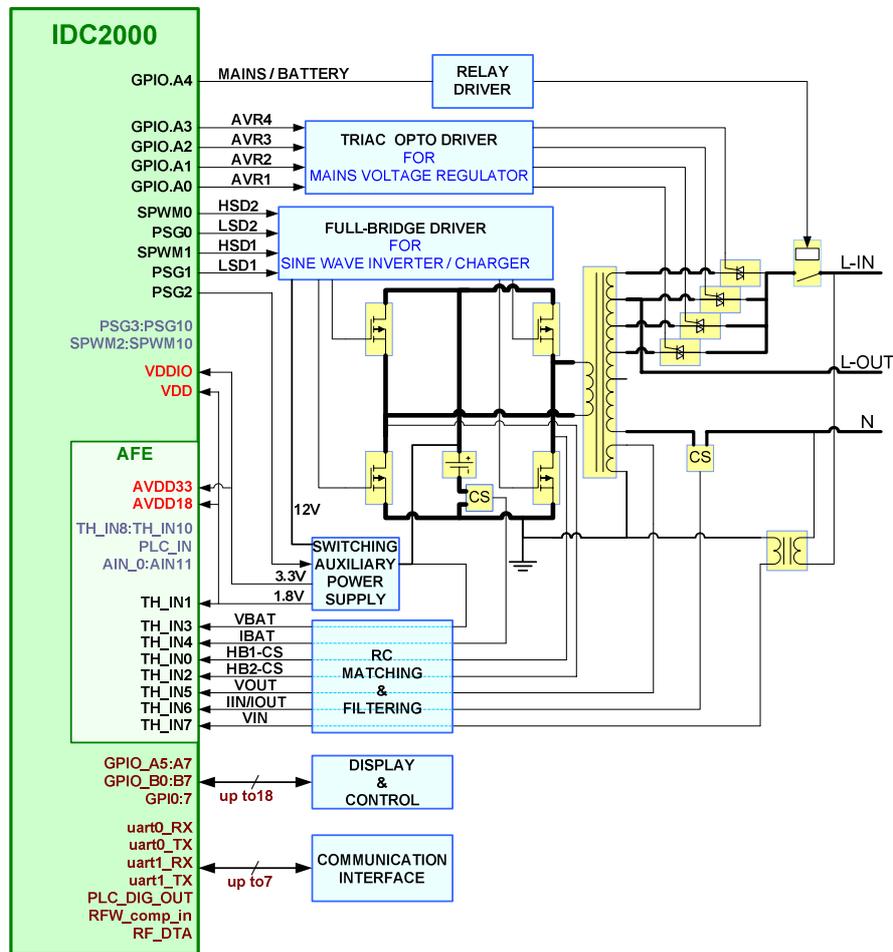
Fig. 11 The line interactive power supply with low THD sine wave and fast AVR response

To mention one of the many other advantages provided by the UPMC - the power switches in this application are precisely protected pulse by pulse current limit thus allowing longer Mean Time Between Failure (MTBF).

The digital capabilities of this controller allow achieving component count and cost optimization in the power circuit design. In addition, further component cost reduction is achieved by using an IDC20XX controller that comprises all the power and management control functions and interfaces in a single chip. Additional advantage is high flexibility in future changes and upgrades which will only necessitate configuration and parameters modification with the existing unit.

VI. DC-DC Converter Application

Another application that demonstrates the power of the UPMC is a multiphase buck converter operating at switching frequency of 6MHz per phase at the load step-up transient of 100A and a slope current of 1000A/µsec. The multiphase converter (Fig. 12) includes 4 HB legs driven and

controlled by the IDC2100 which is a future upgrade version in the UPMC road map aimed for ultra-fast switching mode power supplies.
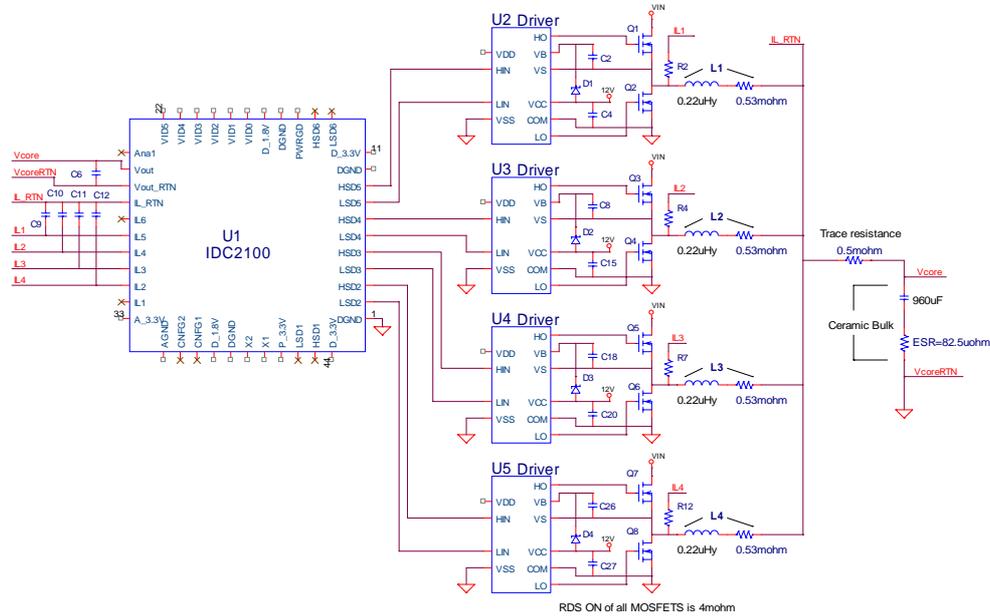

Fig. 12 Four phase synchronized buck converter used for the simulation study

An approximate parameters simulation study was performed to compare the expected performance of the 4 phase converter in Fig.12 in respect to a 6 phase converter alternative, amongst others to show the capabilities of the envisioned solutions. The 4 phase alternative operates at 200KHz and the 6 phase at 800KHz. In the IDC implementation the switching frequency rises to about 6MHz during the transients to achieve the targeted results.

System Specifications:	Alternative 1	Alternative 2
Number of phases	6	4
Steady State Switching Frequency	800Khz	200Khz
Input Voltage	8V to 20V	8V to 20V
Load Current Change	10A-110A	10A-110A
Icc Slope	1000 A/uS	1000 A/uS
Output Voltage (VCC)	1.4V	1.425V
VCC Slope	0.91 mV/A	0.91 mV/A
Power Circuit Electrical Parameters:		
Low Side Switch RdsOn	4mΩ	4mΩ
High Side Switch RdsOn	4mΩ	4mΩ
Low Side Diode – Forward Voltage	2V	2V
Phase Inductor Inductance	110nHy	220nHY
Phase Inductor ESR	0.53mΩ	0.53mΩ
Bulk Capacitor – Total ESL	0.4nHy	0.4nHy
Trace equiv. Resistance	0.5mΩ	0.5mΩ

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Ceramic Capacitors Capacitance	380uF	660uF
CPU Ceramic Capacitors ESR	0.22mΩ	0.15MΩ
Control Parameters Specifications:		
Power Stage Delay Time	50nS	50nS
Total Delay Time	164nS	164nS
Load Step Down – Analog Detect Time	<80nS	<80nS
Load Step Down – Response Time	<30nS	<30nS
Total Step Down Response Time	<160nS	<160nS
Notes: Total Stage Delay Time: delay in FETs and drivers Total Delay Time: Including delay in controller processing		
Results:		
Load Step Down Max. Over Deviation	<4mV	<11mV
Step-Down Sense Response Time	11nS	<80nS
Load Step Up Max. Under Deviation	<3mV	<10mV
Step Up Response Time	<1.5uS	<3uS
Step Down Response Time	<1uS	3uS

Table II Simulations Comparison
Notes: Over Deviation from Targeted Vcc = VID – (Icc*0.91m + 25m). Load Step Up Max.
Under deviation: - 22mV (6ph), >15mV(4ph) over the allowed minimum limit

VII. The main attributes of the IDC2000 family
The main attributes of the IDC2000 family are summarized in Table III and point out the advantages provided by the UPMC controller platform in comparison to the analog or digital approaches extant in the market.

Advanced Algorithms	Advanced PID combined with non-linear control using look up tables, event machines etc. allows optimal algorithm implementations. Providing different solutions for the different modes of operation of the controlled application (steady-state versus transient, low versus heavy load, etc.)
Fast Control	Calculation and measurements are performed by custom logic for each controlled channel (not by CPU). Latency annulment by using predictive techniques combined with feed-forward and non-linear algorithms.
Complex Pulse Generator	State machine allows creation of multi state pulse sequences. The sequence(s) can be modified on-the-fly due to its configurability nature.
Functionality per Silicon Area	The digital process tends to exist in smaller geometries offering lower cost solutions where there is a high degree of circuit function integration.
S/N	Signal to noise of digital functions is better by definition and noise filtering can be more efficient when using digital filters and digital masking.

Shortens Design Duration	The configuration capability without code programming allows short time to market.
Component Count & Reliability	The component reliability is dramatically improved; the digital functions are not subject to aging and tolerances. There is no need for component "select at test" and "select according to design spec". More functions can be integrated which decreases the component count and contributes towards enhancing the MTBF of the component and of the entire system.
Predictability/repeat-ability/Confidence	The digital design allows easier and more confident prediction of the product behavior. The component behavior will repeat itself precisely in production with absolute confidence. The production files will be simpler with less "special notes".
Ease of design Flexibility	Large degree of configurability of the control component including PID gains, programmable filters, sequences and numerical parameters. All design and optimization is accomplished in front of a computer screen through a communication bus.
On-the-Fly Configuration	Digital control allows on-the-fly modification of parameters in response to condition changes.
Easy to simulate	Digital is mathematical – the simulation does not have the complexity of the analog models and is not ambient dependent.

Table III Attributes of the IDC2000 Family

VIII. Conclusions

The UPMC architecture concept brings to the power electronic market a mature, comprehensive and powerful single chip solution for power control and management.

Designed with the vision of allowing the complete migration path from pure analog to mixed-signal technology solutions for applications in which the technological advantages of digital are indisputable. The generic configurable architecture of the UPMC allows designers to create their own "power control ASIC" with negligible silicon overhead.

The IDC2000 family, the UPMC silicon commercial implementation, provides remarkable performances and capabilities, doing away with the limitations of standard digital based solutions in its targeted market; in computation speed, time to market and cost.

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