# A Four Quadrants HF AC Chopper with no Deadtime

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***Abstract*— A four quadrant HF AC Chopper is described, analyzed and verified experimentally. The main advantage of the proposed topology is the ability to handle reactive loads without the need for a deadtime between switches. This is accomplished by dynamically configuring the chopper as positive or negative Buck or Backward Boost converters corresponding to the momentary polarities of the input voltage and output filter inductor current. A 300W breadboard unit was built to test the proposed concept. The experimental results conform to the expected behavior of proposed chopper.**

***Keywords*- AC chopper, high frequency converter switching deadtime, power factor correction (PFC), Field Programmable Gate Array (FPGA).**

## I. INTRODUCTION

HF AC Choppers are useful in applications that require a controllable line-frequency voltage that is lower than the mains voltage. The simplest design of a HF AC chopper (Fig. 1) includes two bi-directional switches that are driven at a constant duty cycle and an $L_O$ , $C_O$ filter to reduce the HF ripple at the output [1-4]. ThAn important feature of the HF AC is that, for linear loads, the HF AC Chopper will comply 'naturally' with the limits for harmonic current emissions (EN1000-3-2).

The HF AC Chopper design of Fig. 1 poses a practical problem that needs to be addressed especially if high chopping frequency is desired. The problem stems from the need to provide a deadtime between the operations of the two switches to prevent shoot through. The inductor current interruptions during the deadtime need to be absorbed by a snubber to avoid dangerous voltage spike. This will reduce the overall efficiency of the HF AC Chopper. A way to avoid this problem is to configure the chopper as a Buck converter (switch plus diode) for each half cycle [3]. This will avoid the current interruption (save the forward recovery of the diode) when the current commutates between the switch and diode. However, this solution is not suitable for reactive loads (Fig. 2) in which four quadrant operation is required. In this case the diodes need to be switched too. This, inadvertently, brings back the deadtime problem [4].

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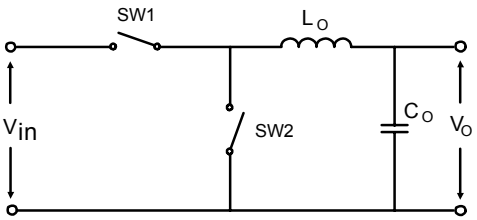


Figure 1. A basic HF AC chopper

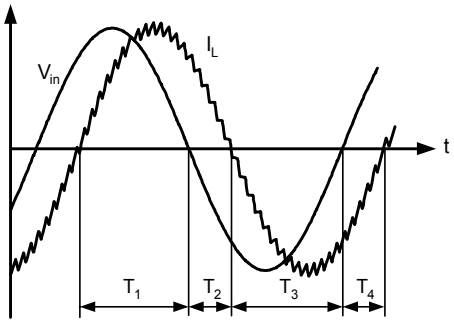


Figure 2. Output voltage and current for a reactive load.

The objective of this work was to develop a four quadrant HF AC Chopper that does not suffer from the deadtime problem.

## II. PROPOSED AC CHOPPER

*a. General Description.* The generic topology of the proposed AC chopper (Fig. 3) includes two switch-diode assemblies (SDA) and an output filter $L_O$, $C_O$. Each SDA can be configured as a diode or switch. To provide four quadrants operation, without the need for a dead time, the SDAs are configured, at any given instance, as a switch and a freewheeling diode in four different chopping topologies (Fig. 4). In the followings we define the polarity of the input voltage with respect to the 'common' (bottom) line of Fig. 3 and the positive current direction is taken when the current is flowing from the input to the output.

For a positive input voltage and a positive current (corresponding to the situation of duration $T_1$ in Fig. 2) the SDAs are configured as a Buck converter for a positive input voltage (Fig. 4a). For a negative voltage and a positive current

(as in $T_2$ of Fig. 2) the SDAs are configured as a Backward Boost converter where the load is acting as a source and the line as a load (Fig. 4b). Figs. 4c and 4d correspond to the remaining combinations of voltage-current polarities.

To obtain a consistent attenuation factor A (A=Vo/Vin), over the four quadrants, the duty cycle of the switches (D) should be:

$$D_{Buck} = A \tag{1}$$

$$D_{Boost} = 1 - A \tag{2}$$

where $D_{Buck}$ and $D_{Boost}$ are the switch duty cycle of the Buck and Backward Boost configuration.

The duty cycle rules (1) and (2) assume that the operation is in the Continuous Conducting Mode (CCM). As shown below, CCM can be assured even for light loads. Hence, operation of the proposed AC chopper is identical to AC choppers that are implemented with two bi-directional switches [1-4]. However, in present case the commutation of the inductor current from the chopping switch to the catching diode is smooth and no snubber is required to handle an interruption in the inductor current path associated with a deadtime, as would be the case when two switches are used.

The SDAs can be implemented by series (as shown in Fig. 3) or parallel connected switches and diodes. The diodes need to be fast diodes to reduce the losses associated with the reverse recovery. The switches could be MOSFETs or IGBTs as there is no need for bi-directional conduction of the switches.

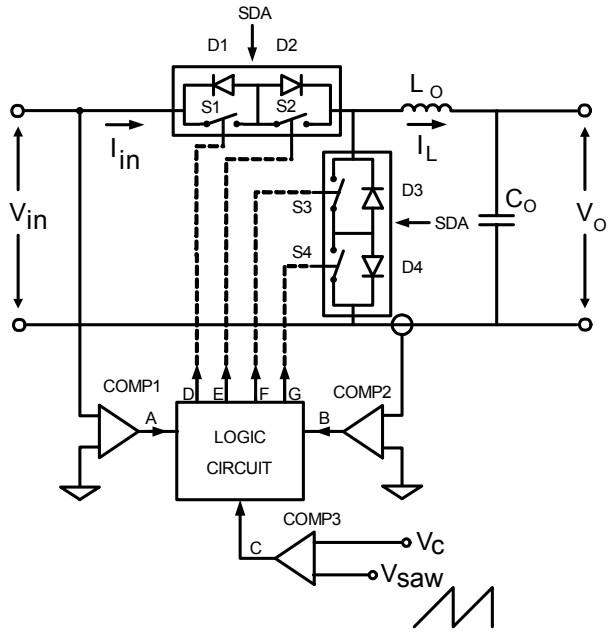


Figure 3. Proposed HF AC Chopper

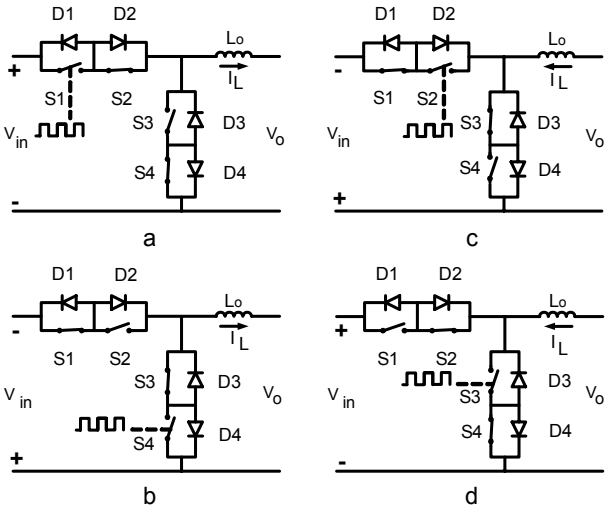


Figure 4. System configuration for different input voltage and output inductor current polarities. Configurations a, b, c, d correspond to periods $T_1$, $T_2$, $T_3$, $T_4$ (Fig. 2) respectively.

In a typical application (Fig. 3) the proposed AC chopper will include the SDAs an input voltage polarity sense, an inductor-current polarity sense, a PWM modulator and a logic circuit that generate the correct gate drives per the voltage and current polarities.

*b. Possible Control Strategies.* Two different control approaches can be considered with regard to the duty cycle generation: a free running or a clocked drive. The latter can be accomplished by applying two D type flip-flops that lock, at the beginning of each switching cycle, the polarity signals corresponding to the voltage and current directions. In this case, a change in the polarity of the voltage or current within a switching period will take effect in the following switching cycle. This implies that if the inductor current drops to zero within the switching cycle, it will stay zero (save reverse recovery effects) till the next cycle. That is, the systems will operate in DCM. However, if the polarity signals of the voltage and current are not locked at the beginning of each switching cycle, the chopper will respond to a polarity change within the switching cycle. In this case the chopper will not enter DCM but rather, the inductor current will wobble between positive and negative values. Namely, as soon as the current will drop to zero, and in fact change polarity due to the reverse diode currents, the configuration will change and the current will continue to increase in the reversed direction. This latter mode of operation, denoted as "free running mode", is demonstrated by considering the case of a positive input voltage. In this situation the four connections, shown in Fig. 5, are possible. It should be noted that connections (e) and (f) are for the "on" duty state while connections (g) and (h) are for the "off" duty state. If the chopper is allowed to reconnect within the switching cycle (no locking D flip-flops) then the expected inductor current waveform for light load will behave as shown in Fig. 6. Consequently, in this operational option, (1) and (2) will hold for low loads too, minimizing the output voltage distortions. It should be noted that the reconfiguration between the Buck and Backward Boost topologies is taken place at

virtually zero current, so the deadtime interruptions pose no problem.

The criterion for the borderline between the CCM and the bi-polar operation is identical to the borderline between CCM and DCM. That is, for a resistive load $R_L$:

$$R_L = \frac{2L_O}{(1-D)T_S} \tag{3}$$

where $T_S$ is the switching period

*c. Ripple Current and Ripple Voltage Considerations.* In most practical cases the output voltage ripple will be relatively small. Hence, the high frequency output inductor current ripple can be estimated by assuming constant output voltage. That is:

$$\Delta I_L = \frac{V_O(t)}{L_O}(1-D)T_S \tag{4}$$

where $V_O(t)$ is the low frequency output voltage. Or:

$$\Delta I_L = \frac{V_{in}(t)}{L_O} D(1-D)T_S \tag{5}$$

where $V_{in}(t)$ is the input voltage.

Hence, maximum inductor current ripple is expected when A =0.5 and :

$$V_O(t) = 0.5V_{in}(t) \tag{6}$$

The magnitude of the output voltage ripple depends on the nature of the load. For a resistive load the output voltage ripple $\Delta V_O$ is like the case of a buck converter:

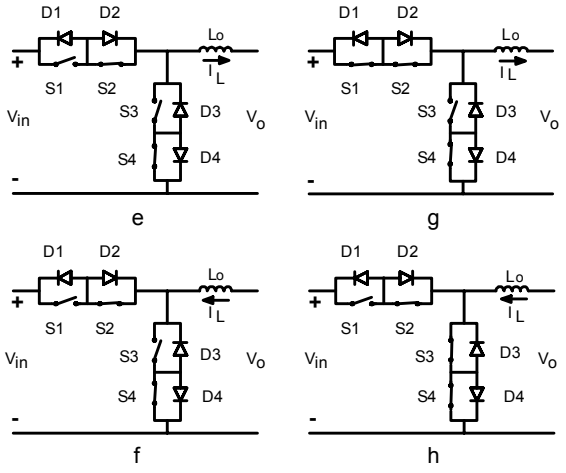


Figure 5. Possible configuration within a switching cycle for a positive input voltage.

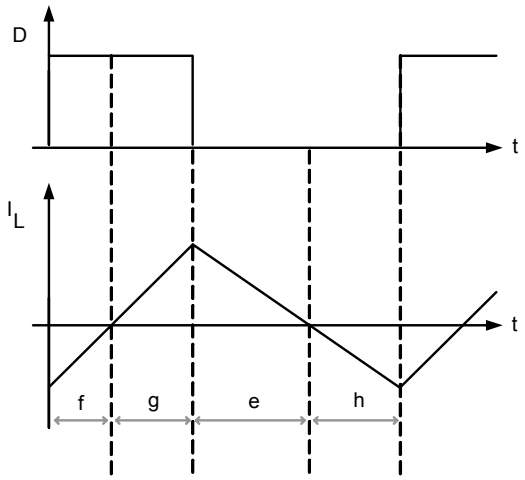


Figure 6. Duty cycle command (upper trace) and inductor current (lower trace) at light load. Periods e, f, g, h, correspond the configurations in Fig. 5.

$$\Delta V_O = \frac{\Delta I_L}{8C_O} T_S \tag{7}$$

For reactive loads, and under the assumption of small ripple, a first order estimate of the output voltage ripple can still be obtained by (7) except that $C_O$ needs to be replaced by $C_{Oeq}$, the equivalent output capacitance. In this case, one has to first calculate the effective output capacitance $C_{Oeq}$ for the switching frequency range:

$$C_{Oeq} = \left| \frac{1}{2\pi \cdot f_S \left( \frac{1}{j2\pi f_S C_O} + X_p \right)} \right| \tag{8}$$

where $X_P$ is the equivalent parallel reactance of the load and $f_s=1/T_s$.

*d. Input-Current Harmonics.* The low frequency component of the input current $I_{inav}$ is the low frequency inductor current sampled during the 'on' time of the series SDA (Fig. 3). That is:

$$I_{inav} = I_L D T_S \tag{9}$$

In the 'free running mode', the average voltage fed to the inductor will be proportional of the input voltage and assuming a sinusoidal input waveform, the inductor current will be sinusoidal. On the other hand, in the 'locked duty cycle mode' an output voltage distortion is expected at low output current levels when the converter enters DCM. One can thus conclude that even for low output currents, the 'free running mode' will theoretically produce an input current of very low distortion for a sinusoidal input voltage.

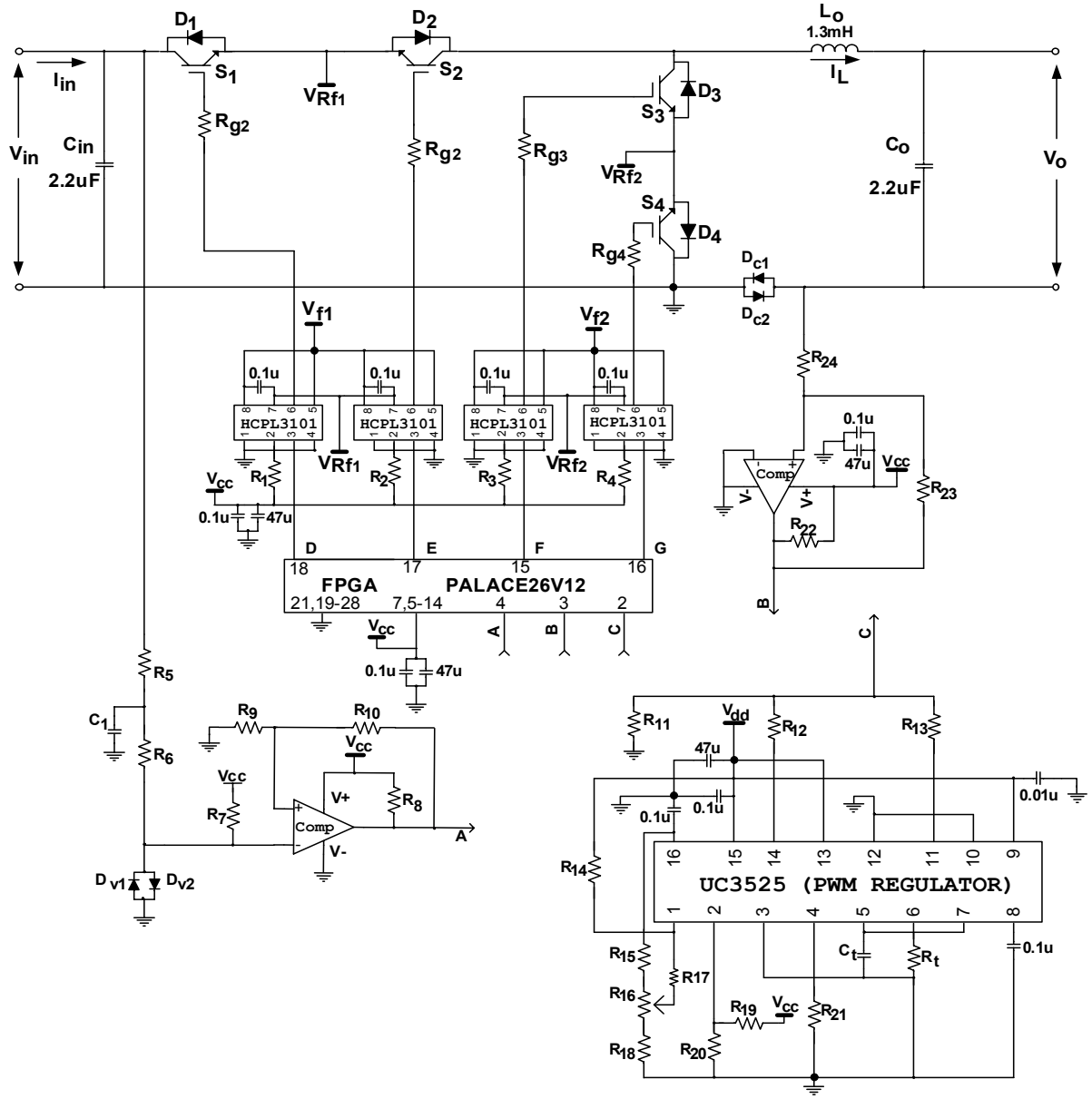


Figure 7. Basic circuit diagram of experimental four quadrants HF AC chopper.

## III. EXPERIMENTAL

A low power laboratory breadboard was constructed and tested to verify the Four Quadrant AC Chopper concept experimentally. The experimental chopper (Fig. 7) was built around IGBT switches ($S_1$-$S_4$), fast diodes ($D_1$-$D_4$) floating drivers and a Field Programmable Gate Array (FPGA). Diodes ($D_{c1}$, $D_{c2}$, $D_{v1}$, $D_{v2}$) and associated comparators were used to sense input voltage polarity and inductor current direction. The unit was operated at a switching frequency of 35kHz and was tested up to a 220Vac input voltage range and at power levels of up to 300W. The output filter components were: $L_O$=1.3mH; $C_O$ = 2.2 μF. Operation was in the "free running mode" that is, the chopper was allowed to change configuration within a switching cycle (relevant to light load conditions). The operation was automatically controlled by the FPGA. The 'truth table' of the programmed logic unit is given in Table I.

Examples of the experimental results are illustrated in Figs. 8-10. Fig 8 depicts the chopping voltage and inductor current under no load conditions – save the output filter. This plot demonstrates the "free running mode" operation (Fig. 6). Fig. 9 shows the chopped voltage between the two SDAs and the

inductor current at no load condition. It verifies the fact that the proposed HF AC chopper keeps the system in CCM even at low current levels. Fig. 10 depicts four quadrants operation with an inductive load (approximately $30^0$ lag of load current with respect to load voltage). The Efficiency of the experimental system was found to be 92%.

Table I. Truth Table of programmable logic.

| A | B | D | E | F | G |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | C | 0 |
| 0 | 1 | C | 0 | 1 | 0 |
| 1 | 0 | 0 | C | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | C |

$$A = \begin{cases} 1 & if \quad Vin < 0 \\ 0 & if \quad Vin > 0 \end{cases}$$

$$B = \begin{cases} 1 & if \quad I_L > 0 \\ 0 & if \quad I_L < 0 \end{cases}$$

$$C = PWM$$

## IV. Discussion and Conclussions

A four quadrant HF AC Chopper was described, analyzed and verified experimentally. The main advantage of the proposed topology is the ability to handle reactive loads without the need for a deadtime between switches. This is accomplished by dynamically configuring the chopper as positive or negative Buck or Backward Boost converters corresponding to the momentary polarities of the input voltage and output filter inductor current. A 300W breadboard unit was built to test the proposed concept. The experimental results conform to the expected behavior of proposed chopper.

The planned applications of proposed HF AC Chopper are dimmers for stage lighting to replace SCR based choppers that generate unacceptable line current harmonics.

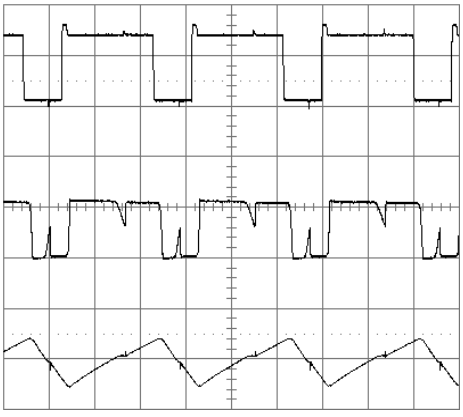

Figure 8. Operation under no load condition. Upper trace: Duty cycle command. Middle trace: chopped voltage (mid point between the SDAs), 100V/div. Lower trace: inductor current, 0.5A/div. Time scale: 10 μs/div.

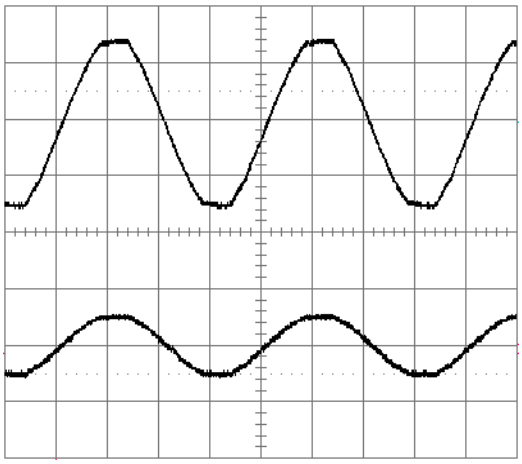

Figure 9. Measured input (upper trace) and output (lower trace) voltages under no load conditions. 100V/div. Time scale: 5ms/div.

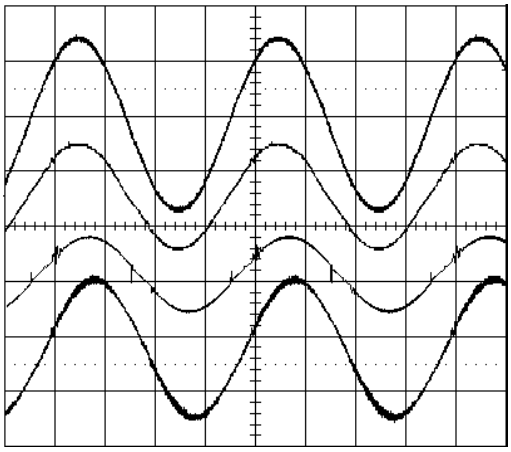

Figure 10. Measured (from top to bottom) input voltage, output voltage (100V/div), input current and load current (1A/div). Time scale: 5ms/div.

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