Resonant Rectifier for Piezoelectric Sources

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Abstract— **A new rectification scheme is proposed for increasing the available output power of electrical generators that have a high output capacitance. The new rectifier could be useful in increasing the output power of piezoelectric generators (PZG) that convert mechanical vibrations to electrical power. The improvement is achieved by a resonant circuit that self commutates the voltage across the output terminals of the PZG and eliminating thereby the shunting of the output current by the output capacitor.**

Keywords- resonant rectifier, piezoelectric generator, dummy, diode bridge, commutation.

I. INTRODUCTION

Piezoelectric (PZ) elements can be used to generate electrical energy from mechanical energy. Such electrical generators could be useful in low power applications where mechanical motion is available. It has been shown [1], for example, that placing a PZ into a shoe sole can generate sufficient electrical power for sport sensors and a local microprocessor. Other demonstrated applications include a manual driven generator for portable radio receivers [2].

Piezoelectric elements (transducers) belong to the general family of generators that are characterized by internal capacitive impedance. The vibrating PZ can be modeled as a sinusoidal current source i_{in} in parallel with its electrode capacitance C_o (Fig. 1). The relative low impedance of the internal capacitor will shut some of the output current and thereby lower the available output power. Considerable effort has been made to reduce or even eliminate this drawback. The classical and intuitive solution is to shunt the capacitor with an external inductor whose value is tuned to the frequency of the excitation. Consequently, the impedance of the LC resonant network will be high and all the available power will dissipate into the load [3]. This technique typically requires a large inductance value (over 1H) and is therefore an impractical solution. Another proposed solution was to synthesize a negative impedance [4] for reducing the equivalent capacitance. In [5] the authors suggest the use of virtual grounded and floating inductors to achieve the required inductor value. However, these types of implementations are generally poor representation of ideal inductors, they are large in size, difficult to tune, sensitive to component variations and require an external power source. Considering the fact that, for a given excitation frequency, the inductances values are

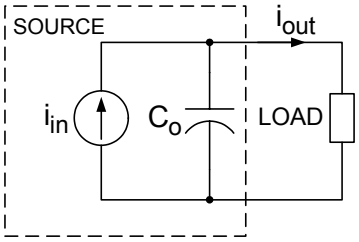

Figure 1. Electrical equivalent circuit of capacitive current source driving a load.

inversely proportional to the equivalent piezoelectric capacitance, the required inductance can be reduced by simply increasing the capacitance [6]. This result is achieved by placing an additional external capacitor in parallel with the piezoelectric transducer. Indeed, the inductance value is reduced significantly, but so does the damping ratio. The high quality factor Q of this arrangement generates high reactive currents and makes the generator very sensitive to the excitation frequency. The reactive current will cause considerable power loss and a slight change in frequency of the source will cause a large power loss due to the shunting effect of the LC network.

In most applications, the AC signal produced by the PZ generator (PZG) needs to be rectified [7-9]. However, considering the low power level involved, the rectification scheme should be as efficient as possible in order to improve the electrical power harvesting.

A basic rectification scheme (Fig. 2) for an AC source such as the PZ generator will include a bridge rectifier or a voltage doubler. Both suffer from the energy loss due to the output capacitor C_o of the PZG. Consequently, for each rectification scheme there is an optimal load resistance for which the output power will be maximal [9-11].

The objective of this study was to develop a new rectification scheme that will improve the energy harvesting from a PZG by eliminating the shunting effect of the output capacitor.

II. STANDARD DIODE BRIDGE RECTIFIER

Since the conventional diode bridge rectifier (Fig. 2) was used as a reference for comparing the improvement of the new

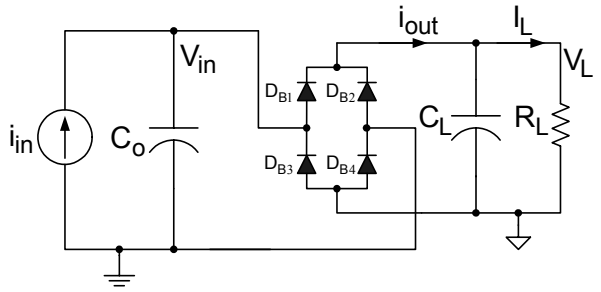

Figure 2. General topology of a capacitive current source loaded by a conventional diode bridge rectifier circuit.

design, we first derive the expression for the maximum output power for this case.

During the time interval t_1~t_2 (Fig. 3) the capacitor C_o is clamped to the negative voltage ($-V_{in(pk)}$) and allows a current path from the source to the load via D_{B2} and D_{B3} (Fig. 2). The clamping voltage is equal to sum of the DC output voltage V_L and 2 diode forward voltages V_D:

$$V_{in(pk)} = V_L + 2V_D \tag{1}$$

During the time interval t_2~t_3 (Fig. 3), the capacitor is charged by the current source, and the capacitor's voltage reverses its polarity from $-V_{in(pk)}$ to $V_{in(pk)}$. At that time period no current is available to the load. The DC current that reaches the load, is the average of i_{out} (Fig. 3),

$$I_L = \frac{2}{T_s}\int_0^{T_s/2} i_{out}(t)dt = \frac{2}{T_s}\int_{t_1}^{t_2} |i_{in}(t)|dt \tag{2}$$

where T_s is the period of i_{in}. Following [7] we obtain,

$$I_L = \frac{\frac{2I_P}{\pi} - \frac{4\omega_s C_o V_D}{\pi}}{1+\frac{2\omega_s C_o R_L}{\pi}} \tag{3}$$

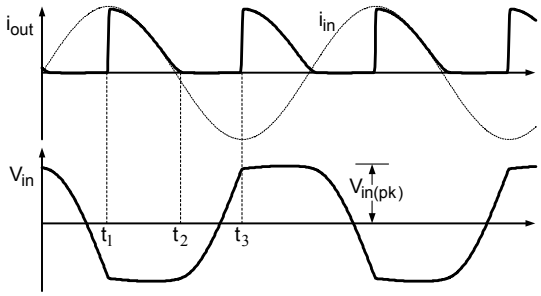

Figure 3. Typical waveforms of diode bridge rectifier circuit.

where I_p and ω_s are the amplitude of the current and angular frequency of the current source, respectively. The load power is,

$$P_L(R_L) = \left(\frac{\frac{2I_P}{\pi} - \frac{4\omega_s C_o V_D}{\pi}}{1+\frac{2\omega_s C_o R_L}{\pi}}\right)^2 \cdot R_L \tag{4}$$

The optimal load that maximizes the output power (taking into account the diode voltage drop) is the load that maximizes the power through the output load-diode combination,

$$P_{out} = P_L + P_D = I_L^2 R_L + 2V_D I_L \tag{5}$$

Differentiating Eq. (5) with respect to R_L and equating it to zero, we obtain:

$$R_{L(opt)} = \frac{\pi}{2}\cdot\frac{1}{\omega_s C_o\left(1+\frac{2V_D}{V_L}\right)} \tag{6}$$

Note that in the absence of capacitance C_o the power will be proportional to load resistance,

$$P_L(R_L)\big|_{C_o=0} = \left(\frac{2I_P}{\pi}\right)^2 \cdot R_L \tag{7}$$

and the power that could be extracted from the source will, theoretically, approach infinity (if R_L is made very high). In reality, the high output voltage generated when R_L is large, will damp the PZ resonator and hence limit the output power.

III. New Resonant Rectifier Circuit

The proposed rectification topology (Fig. 4) includes an inductor (L_{res}), two switches (SW_1, SW_2), two diodes (D_1, D_2), a circuitry that evaluates the derivative of the capacitor's voltage (d/dt), and a comparator (COMP). A capacitor loaded diode bridge rectifies the AC across the PZG output capacitor (V_{in}). The expected waveforms of the proposed rectifier over a complete cycle are presented in Fig. 5.

Assuming that at time t_1 (Fig. 5), the capacitor C_o is pre-charged to ($-V_L$-$2V_D$), the source current flows during (t_1~t_2) to the load via D_{B2}, D_{B3}. At time instance t_2, the source current changes direction, starting to charge C_o during time t_2~t_3 until V_{der}, that is the derivative of the capacitor's voltage V_{in}, reaches the threshold level of the comparator causing its output (V_c) to switch to the low state at time t_3. This turns on switch SW_2 which initiates a self-commutation interval t_3~t_4 via SW_2-D_2-L_{res}-C_o.

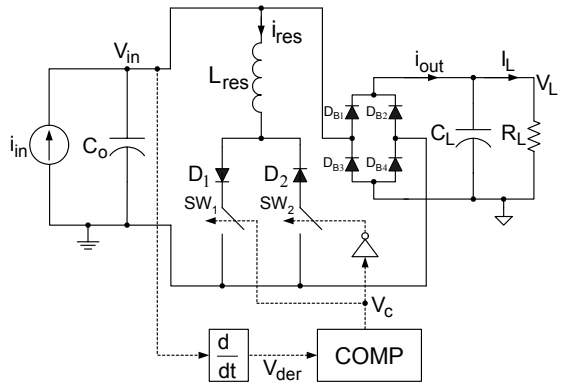

Figure 4. The proposed resonant rectifier circuit.

Assuming a high quality factor Q, the resonant time interval t_3~t_4 can be estimated by:

$$t_{res} = t_4 - t_3 \approx \frac{\pi}{\omega_{res}} = \pi \cdot \sqrt{L_{res} C_o} \tag{8}$$

and the peak current of L_{res} will be:

$$i_{res(pk)} \approx \frac{V_{in(pk)}}{Z_o} = V_{in(pk)} \cdot \sqrt{\frac{C_o}{L_{res}}} \tag{9}$$

where

$$Z_o = \sqrt{\frac{L_{res}}{C_o}} \tag{10}$$

During the time interval t_4~t_5 the inductor's current is already zero and the capacitor is charged by the input source current. There are two reasons for the incomplete commutation. The first one is the fact that the commutation starts after the capacitor voltage has already dropped during the interval t_2~t_3. Therefore, during the next interval (t_3~t_4) less energy is available and the capacitor voltage cannot be fully recovered to V_L+2V_D. A second reason for the incomplete commutation is the power loss during the time duration (t_3~t_4) because of the voltage drop on D_2 and the resistance of L_{res} as well as the "on" resistance of the switch. These power losses are replenished by the power coming from the source and eventually, the input voltage V_{in} will be clamped to V_L+2V_D at time t_5 and a current path to the load is possible through diodes D_{B1} and D_{B4} of the bridge.

The operation of the resonant rectifier is thus based on the fact that the inductor and the PZG output capacitor form a resonant network that is activated by closing switches (SW_1) or (SW_2). The switches are closed at the end of each half cycle and thus the voltage across the capacitor will automatically, by virtue of the resonant current, change polarity. Consequently, except for the need to overcome losses, the PZG current is not required for commutating the capacitor voltage, and a large portion of the current will pass to the output.

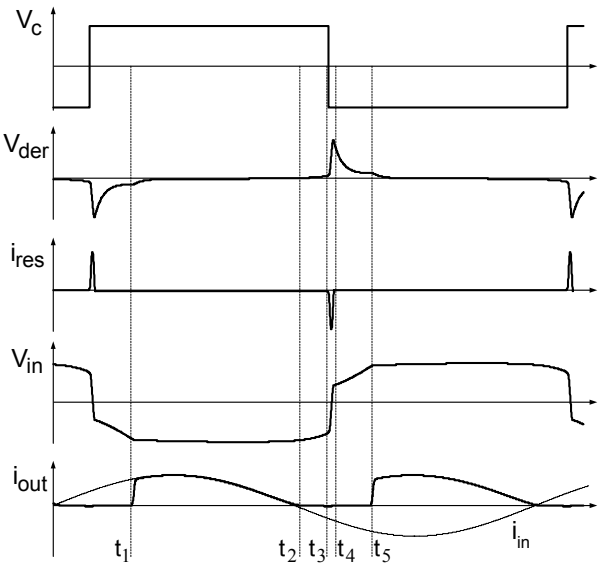

Figure 5. Key waveforms of the resonant rectifier circuit.

IV. Experimental Results

The circuit diagram of the experiment set up is shown in Fig. 6. All the diodes used in the circuit are Schottky diodes (1N5817). The resonant circuit consisted of paralleled MOSFET switches (three VP0104 and three VN0104) for implementing M_p and M_n respectively. The comparator was an ultra low power IC (MAX921, Maxim, USA). The bi-polar power supply for comparator was realized by two extra diodes (D_{S1}, D_{S2}) and bus capacitors (C_{S1}, C_{S2}).

The derivative of V_{in} (V_{der}) was obtained by a differentiator circuit C_{der}-R_{der}. In order to prevent either erroneous or undesired triggers events, hysteresis was introduced by adding resistor R_{hys}.

Two sets of experiments were performed. The objective of the first set was to assess the performance of the proposed rectifier and for verifying the loss estimation. In this set we used a dummy current source for modeling the generator stage. A high voltage floating source V_{ex} of 200$V_{(pk)}$ in series with 100KΩ resistor R_{in} produced a sinusoidal current source i_{in} of 2m$A_{(pk)}$. This current was monitored by a 1KΩ sense resistor R_{sens}. A capacitor C_o of 330nF was placed in parallel with the input of the rectifier to emulate the capacitive behavior of the AC source.

The first measurement set included three rectification schemes: the standard diode bridge rectifier (Fig. 2), the resonant rectifier (Fig. 6), and the resonant rectifier in which the comparator was fed by an auxiliary power supply (+/- 4V). The purpose of the third scheme was to neutralize the power consumption of the comparator and to ensure sufficient gate drive voltage to the MOSFETS. In each case the load was adjusted to maximize the output power.

The results are summarized in Table 1 for the standard rectifier, self-powering resonant rectifier and resonant rectifier with ±4V external supplies. As expected, the latter yielded the highest power level of 3.16mW while the output of the

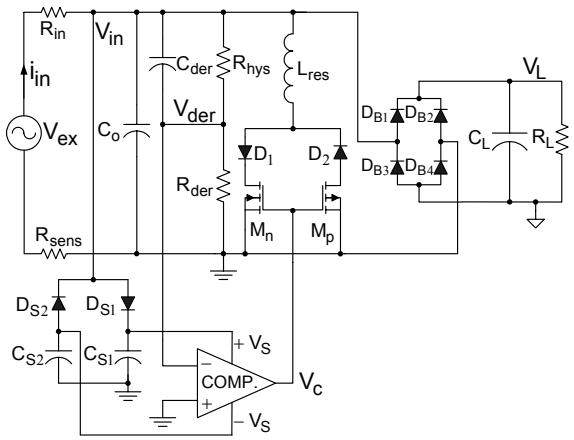

Figure 6. Circuit diagram of experiment set up with dummy current source.

standard rectifier was only 1.26mW.

The resonant rectifier showed a significant improvement (251%) compared with conventional rectification output power. Figs 7 and 8 show the experiment waveforms of the standard rectifier and the resonant rectifier with external supplies respectively. Both figures are marked by the time events corresponding to ones discussed in Sections II and III.

Neglecting comparator losses, total losses of proposed circuit were estimated to be 1.22mW for the experimental parameters: $V_{in(pk)}$=3.5V, L_{res}=1mH, C_o=330nF, R_r=1Ω, V_D=0.5V, f_s=185Hz, C_L=1μF and I_L=0.8mA. The measured total loss of the resonant rectifier with external supplies was 0.8mW (Fig. 8.a and Table 1), lower than the estimated one.

In the second set of experiments a PZ was used as a generator (Fig. 9) for the same three rectification circuits, while testing procedure remained the same. The generator was built by connecting longitudinally two piezoelectric bimorph van elements (RBL1-006 model, Piezo Systems, Inc, USA). One was used as an actuator and the other as a transducer. The actuator was excited by sinusoidal voltage source of $40V_{p\text{-}p}$. This arrangement provided the required mechanical excitation for the second van that was used as the generator. The output capacitance C_o of the transducer was estimated to be 60nF using the technique of [12]. Two adjustments were needed here for maximizing the output power, one for locating the resonance frequency of the PZ device (approximately 185Hz), and the second adjustment for selecting the optimal load of the rectification circuit under test (for a given frequency). The measured extracted power for the three rectification circuits are summarized in Table 2. Maximum extracted output power produced by the resonant rectifier with external supplies was 230% of the power produced by the conventional rectifier.

Table 1. Experiment results with $2mA_{(pk)}$ source.

CIRCUIT TOPOLOGY	OUTPUT VOLTAGE (DC)	OPTIMAL LOAD	OUTPUT POWER	GAIN (%) COMPARED WITH STANDARD RECTIFIER
STANDARD RECTIFIER	1.6V	2.1KΩ	1.26mW	-
RESONANT RECTIFIER	2.2V	2.75KΩ	1.79mW	**142%**
RESONANT RECTIFIER WITH EXTERNAL SUPPLIES V_S=±4V	3.34V	3.51KΩ	3.16mW	**251%**

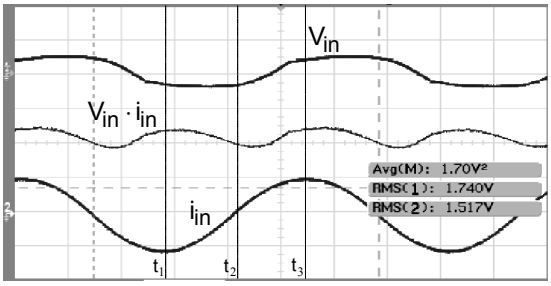

Figure 7. Experiment waveforms of the standard rectifier. Measured input power: 1.7mW. Vertical scales: V_{in}-5V/div; i_{in}-2mA/div.

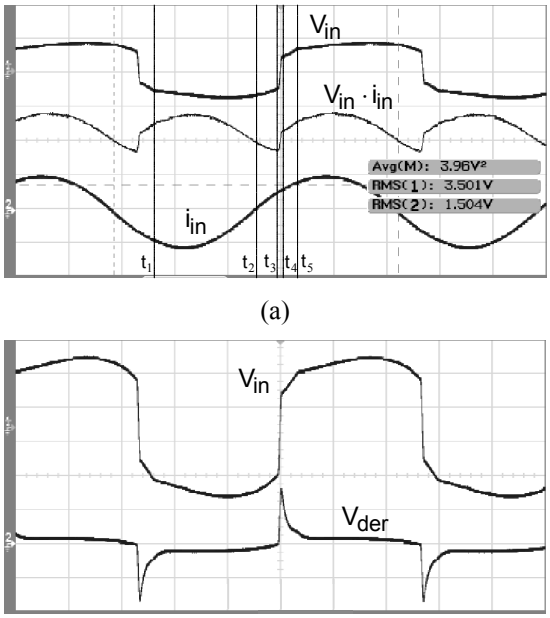

Figure 8. Experiment waveforms of the proposed resonant rectifier. Measured input power: 3.96mW. Vertical scales: (a) V_{in}-5V/div; i_{in}-2mA/div; (b) 2V/div.

V. Discussion and Conclusions

A new resonant rectifier circuit is introduced. The operation of the circuit is based on a highly efficient resonant energy transfer between a capacitive source such as a PZG and an inductor. This mechanism, controlled by self-timed circuitry, facilitates the commutation of the voltage across input capacitor C_o. This was shown to lead to a significant output power improvement of 251% compared to a conventional rectifier for dummy source and 230% for a piezoelectric generator.

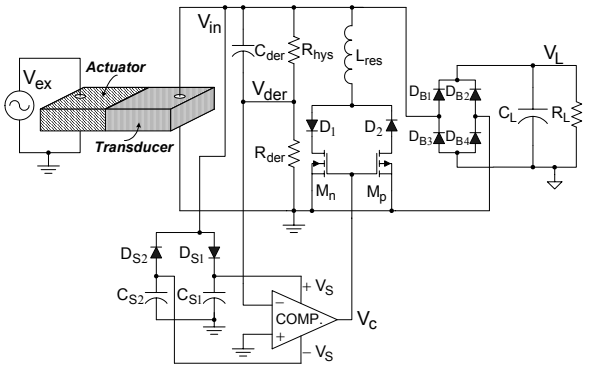

Figure 9. Circuit diagram of experiment set up with piezoelectric generator.

Table 2. Experiment results with the piezoelectric generator.

CIRCUIT TOPOLOGY	OUTPUT VOLTAGE (DC)	OPTIMAL LOAD	OUTPUT POWER	GAIN (%) COMPARED WITH STANDARD RECTIFIER
STANDARD RECTIFIER	1.779V	5.89KΩ	0.537mW	-
RESONANT RECTIFIER	1.818V	5.19KΩ	0.636mW	**118%**
RESONANT RECTIFIER WITH EXTERNAL SUPPLIES V_S=±4V	3.75V	11.43KΩ	1.23mW	**230%**

The first experiment reveals total losses of 0.8mW for the rectifier circuit with external supplies, while the theoretically estimated losses were 1.22mW. A considerable portion of these losses is due to forward voltage drop of the bridge diodes (D_B). This problem can be alleviated by using a synchronous rectification scheme in which the diodes (D_B) are replaced by a switch with low "on" resistance and thereby reducing the forward voltage drop to a negligible value.

The circuit was also tested in self-powering mode. It showed 142% output power improvement compared to the standard rectifier with dummy source and 118% output power improvement with piezoelectric generator. The main reason for this modest improvement is the low power level that was available from the experimental PZG. The relatively low power level resulted in a low output and auxiliary supply voltages which, in turn, was not sufficient to drive M_n and M_p into the range of low "on" resistance $R_{ds(on)}$. Consequently, power dissipation of the circuit was increased in addition to already existing losses due to the resistance of the inductor, power consumption of the comparator and due to the parasitic gate capacitance of the transistors.

The total losses of the resonant rectifier are a function of the parasitic resistances and the voltage drop on the diode. The smaller the resistance and the voltage drops, the lower will be the losses. Optimization of the resonant inductor is less obvious. One might think that a reduction in inductance of L_{res} value will minimize the commutation period t_{res} (Eq. (8)) and hence will increase output power. In reality, a decrease in the value of L_{res} will increase the resonant current (Eq. (9)) which might lead to a larger power dissipation by D_1, D_2, M_n, M_p and the resistance of the inductor. Therefore, in the selection of the inductor one should consider the two factors: (1) the output power loss during the commutation period and (2) the power loss due to the resonant current. In practice, one should strive to make L_{res} as small as possible while keeping the conduction losses a reasonable fraction of the expected total power.

Considering all non-idealities and limitations discussed above, the resonant rectifier exhibits an impressive improvement compared to the conventional rectifier. Additional improvement could be achieved by replacing the diode bridge by a synchronous rectification scheme in a self-powering system suitable for mobile applications.

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