A Novel Optimized Snubber with Time-Varying Capacitor for Synchronous Rectification, Analysis and Implementation

Wei ZHANG, Wei CHEN, Wenxi YAO, Zhengyu LU
Institute of Power Electronics
Zhejiang University
38# Zheda Road, Hangzhou, 310027, P. R. China

Abstract—This paper begins by illustrating the issue of switch stresses on synchronous rectifiers (SRs) which happens during the hot plug-in and plug-out operation – turn on and off moment of the synchronous rectification in isolated non-regulated Dc-Dc converters, such as the single stage unregulated bus converter. Next, full analysis of the working principle of this unfavorable phenomenon is presented theoretically and experimentally. For conquering this difficulty, a novel snubber with time varying capacitor is proposed and experimentally demonstrated with detailed designing considerations and experimental results. Besides, to dig deeply into the idea exhibited from this novel method, this paper also extends the application of the novel snubber and propose many other time-varying snubber cells based on the idea with even more flexible applications. Finally, experiment results are presented to verify this idea by the improvements shown on the prototype of a 1/4 brick bus converter, which generates 12V-300W output from 48V bus input voltage.

I. INTRODUCTION

With the advent of the great challenges of high performance in nowadays power supply development, scalable and adaptable intermediate bus architecture (IBA) with two stages (shown in Fig.1) [1] [2] attracted great numbers of power-supply manufacturers in the field of ever-changing power requirements of computers and telecommunication for its cost-effectiveness and high efficiency. The front-end AC-DC converter is a standardized module with the paralleling capability to convert the AC voltage source into the 48V DC voltage bus widely used as a standard. This DC bus voltage is often distributed via a back-plane into various circuits, isolated/non-isolated and regulated/non-regulated included, in a form of plug-in modules with additional point-of-load DC-DC modules locally supplying the need power levels at the appropriate voltages to the end users [3]. This paper mainly covers the isolated non-regulated Dc-Dc brick bus converters which convert the 48V input voltage directly to the 12V load. These products are mainly used in different point of loads (POLs), such as telecommunication and computer related fields.

In order to achieving higher frequency to get smaller size with higher power density, and in the same time, higher efficiency, as well as the adaptable power supply architecture, many approaches are adopted to fulfill this task, such as soft-switching [4], sensor-less optimization[5][6], various novel driving schemes, including self-driven, current driven methods[7][8][9][10]. At the same time, the on-board converters are always used in parallel with the technology of synchronous rectification to have a higher power density and decrease diode conduction losses [11] [12]. In a plug-in and plug-out board converter system, appropriate time sequence circuit is required in on/off control for synchronous rectification, for the synchronous rectification function should be turned off at a short period in protection from output bus short circuit when hot plug-in and hot plug-off operation of the board converter is carried out. In the isolated non-regulated bus converter, practical experimental results show us that the synchronous rectifiers (SRs) have higher reverse voltage stresses when transition from body diode conduction to SRs happens in zero load current condition than that in the normal synchronous rectification mode. For the purpose of safety in the whole system, the synchronous rectifiers are selected on the principle of most serious stresses in all over the working situations in order to guarantee the reliability and stability in board converters. Traditionally, there are several typical methods to solve this problem: (a) Modulating the traditional RC network snubber to absorb the additional stresses in the period of plug-in and plug-out operation which indubitably has a comparably large time constant. (b) Choosing higher drain-to-source breakdown voltage ($V_{DS}$) synchronous rectifiers to satisfy the requirement of their stresses. Both of the two methods mentioned above have lethal disadvantages of higher losses, for method (a) indubitably has larger capacitor which bring additional losses on the snubber network, and no doubt causes more thermal designing difficulties, and method (b), which employ higher
drain-to-source limit voltage ($V_{DS}$) SRs, always has even worse effects, such as the higher drain-source on-state resistance, which will have much more on-state losses and definitely lower the system efficiency. In conclusion, the two traditional ways mentioned above all have too many obstacles to achieving higher efficiency. Besides, the single-stage isolated non-regulated bus converter always runs on full duty cycle in open loop modulation to have higher efficiency, for the buck topologies dc-dc converter employ the merit of lower freewheeling secondary rectifier diode losses and higher conduction efficiency. In addition, it is hard to have full range soft-switching in wild load range, for example, zero load operation. Because dc-dc converter which employs soft-switching methods, in most cases, does not have enough loop energy to achieve ZCS condition for secondary rectifier diode or synchronous rectifiers (SRs).

This paper will fully describe the working principle for the higher reverse voltage stresses on the SRs happened in the transition from body diode conduction to SRs. And for conquering this difficulty, this paper also proposes a novel optimized snubber with time varying capacitor, shown in Fig. 2 (Part 3 with the red line). In addition, designing considerations with theoretical analysis will be presented into details, and experiment is conducted to verify the novel snubber with time varying capacitor. To delve into the idea exhibited from this snubber, this paper, finally, innovate many other snubber circuits, and, to a great extent, broaden this application even more flexible ways.

II. STRESS ANALYSIS ON SYNCHRONOUS RECTIFIERS (SRs)

Taking into consideration of the natural characteristics of the buck topology, the on-board bus converter always has a comparably higher efficiency with the utility of roughly 50% primary switches duty cycle. What is more, the bus always has numbers of bus converters in parallel to satisfy the requirement of the load. Therefore, the hot plug-in and plug-out function is necessary in on-board converter which satisfies the scalable and adaptable requirement of the intermediate bus architecture (IBA) [1][2]. In addition, on-board converter, which employs synchronous rectification for low output voltage and high load current application, always faces the danger of short circuit at the plug-in operation when the output voltage is not flowing up to the bus voltage. Fig.3 (a) shows up a typical full bridge topology bus converter with center-tapped rectifier, and this circuit on plug-in operation, in which situation the output voltage does not achieve the required bus voltage, have dangers of short circuit through SRs if the synchronous rectification is working at the start. Fig.3 (b) shows the short circuit loop. Therefore, effective measures should be taken to stop this severe phenomenon, and make sure the bus converter can work well in plug-in operation. Currently, industry manufacture always takes the advantage of the body diode to blocking the bus voltage in protection form short in plug-in operation, which necessarily means the synchronous rectification should not come into use before the output voltage climbs up to bus voltage. As a result, the on-board bus converter has two stable states in plug-in operation: (a) Synchronous rectification is not activated and body diode rectification is in function when $V_O$ has not yet followed the bus voltage. (b) Synchronous rectification comes into use to take the place of bode diode in order to decrease the conduction loss of the body diode. When it comes to this transition, suitable time sequence control circuit is needed to implement this function.

Because body diode rectification can just conduct the current in one single direction while the SRs do in both when turned on, like a very small resistor of several milliohms, the operation with body diode conduction and synchronous rectification (SRs) does not follow the same principle in the isolated non-regulated converter. Therefore, the output voltage in body diode conduction mode differs from that in synchronous rectification. As a result of the two different output voltages in two function mode, experiment results show us that the transition between the two mode brings additional reverse voltage stresses on the synchronous rectifiers, which put the SRs in danger in plug-in operation. In

![Figure 2. Novel snubber with time-varying capacitor](image)

![Figure 3. (a): Full Bridge converter with center-tapped rectifier. (b): Short circuit loop when output does not flow up to output bus voltage at the plug-in operation.](image)
order to show the working principle into details and make full analysis, Fig.4 shows the output voltage working in plug-in operation at zero and full load. From these two figures, it is easily to draw that there are 5 stages in this transition. And the analysis of the five stages is given below with detailed explanation:

Stage 1 \([t_0, t_1]\): In this stage, due to the time consumed on the line transmission, even though the control signal is ON, the ON/OFF signal in the bus converter still keeps OFF, and the out voltage is zero in Fig.4 (a) and Fig.4 (b). And this condition lasts till the bus converter actually receives the signal and acknowledges it with a start operation. For a settled system, the transmission time is fixed.

Stage 2 \([t_1, t_2]\): As soon as the converter accepts the ON signal, the system reacts, and the out voltage climbs up. One point must be noted that the synchronous rectification mode with the SRs conduction is not activated, and body diode rectification is in function and conducts the power from the primary to the output. This purpose of setting this time sequence control with diode conduction first is designed to protect the short circuit when output voltage does not fly up to the bus voltage, which mentioned above. Until the moment \(t_2\), circuit comes to on stable state with body diode rectification.

Stage 3 \([t_2, t_3]\): The out voltage keep steady with body diode rectification until the moment \(t_3\) comes, at which synchronous rectification is activated by the system control signal, and the rectification mode changes conduction from body diode to SRs.

Stage 4 \([t_3, t_4]\): At the moment of \(t_3\), synchronous rectification is activated, and SRs starts to replace the body diode rectification with SRs. For the bus converter system working principles, which will be analyzed in detail below on full load current and zero load current application respectively, are theoretically different between these two rectification methods, and the on-board converter has a short period dynamic oscillation on this transition. Fig.4 shows us the output voltage \(V_O\) transition in the plug-in operation, and Fig.4 (a) is working in zero current load while Fig.4 (b) in full load current mode. In Fig.4, \(V_{O1}\) is the output voltage in stable body diode conduction mode, and \(V_{O2}\) is in stable SRs rectification. Differences can be easily drawn form Fig.4 that the change on output voltage \(V_O\) is different between full current load and zero current. In zero current load, \(V_{O1}>V_{O2}\); while in full current load application, \(V_{O1}<V_{O2}\). Full analysis on the difference will be presented below.

Stage 5 \([t_4, t_5]\): on-board bus converter transfers into SRs conduction rectification mode with stable status and lasts. Till now, the circuit system comes into the ideal working condition.

From Stage 1 to stage 5, one major point which must be discussed is that the difference between \(V_{O1}\) and \(V_{O2}\) in zero load current mode and full load current mode, which is mentioned in stage 4. And the theoretical analysis is discussed with the detailed information in both zero current load mode and full current load.

Full load current mode: In stage 3 \([t_2, t_3]\), bus converter in full load current mode is definitely working in continuous current mode (CCM), for the output current and the effective duty cycle are both large enough to keep current flowing through inductor from decreasing into zero. As a result, output voltage can be drawn from this expression:

\[
V_{O1} = \frac{V_{IN}}{n} \cdot D_y - V_F
\]

Where \(V_{O1}\) is the output voltage in body diode rectification, \(V_{IN}\) is the bus converter input voltage; \(n\) represents the primary to secondary transformer turns ratio; \(D_y\) is the effective duty cycle of full bridge topology converter; \(V_F\) is the forward voltage of the synchronous rectifier, which is approximately 1.0V. In stage 5 \([t_4, t_5]\), system comes into steady state of rectification with synchronous rectifier, which has a different working principle. In this condition, the main current flowing to the load is transferring from body diode to synchronous rectifier, which forward voltage decreases to a very small amount, and this voltage can be calculated by the expression below:

\[
V_F = I_{SRs} \cdot R_{DS-on}
\]

Where \(I_{SRs}\) refers to the current following through the synchronous rectifier and \(R_{DS-on}\) stands for the synchronous rectifier MOSFETs drain to source on-state resistance. For the resistance \(R_{DS-on}\) is of milliohm order. Even multiplied by a large current, for example, \(I_{SRs} = \frac{I_o}{3} = \frac{25}{3} \times 10^3\) (3 SRs in parallel in a 300W 12V output bus converter), the forward voltage \(V_F<0.03V\), assuming \(R_{DS-on}=3m\Omega\). Comparing with \(V_F 1V\) in body diode rectification, this will, as a result, increase the output...
voltage by about 1V, which is $V_{O1} < V_{O2}$. And Fig. 4(b) vividly shows us this comparison.

**Zero load current mode:** Different from full load current mode, the principle of the body diode and SRs rectification is totally different in zero load current mode. In stage 3 [$t_2, t_3$] of Fig. 4(a), bus converter is under the rectification based on body diode conduction, which requires the system working in discontinuous current mode (DCM). Taking the full bridge topology bus converter for example, which is shown on Fig. 5, and assuming the body diode is ideal with the forward voltage $V_F = 0V$ for analytical convenience in zero load current mode, the output voltage follows the DCM working principle which could be expressed by the following function [13]:

$$\frac{n \cdot V_{Oi}}{V_{IN}} = \frac{1}{I_o/(4D_y^2I_{OGmax}) + 1}$$

(3)

Where:

$$I_{OGmax} = V_{IN} / (8L \cdot f_s)$$

(4)

and $V_{Oi}$, $V_{IN}$, $n$, $D_y$ have the same meaning mentioned in full load current mode; $f_s$ refers to PWM switching frequency; $I_o$ stands for load current. In zero load current mode, $I_o=0A$. Substituting $I_o=0A$ to the expression (3), it is easy to get:

$$V_{Oi} = \frac{V_{IN}}{n}$$

(5)

While in SRs rectification, shown in stage 5 [$t>t_4$] in Fig. 4(b), principle that the on-board converter follows is continuous current mode (CCM) of full bridge converter, for the synchronous rectifier could conduct in two direction, different from that in the diode conduction. And the output voltage could be shown below, which is:

$$V_{Oi} = \frac{V_{IN}}{n} \cdot D_y$$

(6)

sharing with that in full load current mode. In the real synchronous rectification, for protecting the bridge leg from shoot through, $D_y$ is roughly 100% but not equal, what is more, there must be dead time between the driving signals of the two switches in one leg, for example, $S_1$&$S_2$, and $S_3$&$S_4$, shown in Fig. 5. Therefore, $D_y < 1$. Substituting $D_y < 1$ to the expression (6) and comparing with (5), it is easy to draw the expression:

$$V_{Oi} > V_{O2}$$

(7)

As there is output voltage drop during the transient from stage 3 to stage 5 in zero load current mode, the energy differentiation between the two stages, which can be calculated by:

$$\Delta W = C \cdot (V_{Oi} - V_{O2})^2 / 2$$

(8)

And $\Delta W$ must have been consumed by the secondary center-tapped rectifier, because $I_o$ is zero in zero load current mode operation. Fig. 6 is one test from the 48V-12V, 300W, 1/4 brick bus converter in zero load current mode with the maximum input voltage, in which the comments of $S_E$, $S_R$ and $V_{DS}$ is illustrated in TAB. 1. From Fig. 6, it is obvious to notice that $V_{DSmax}$ happens around $t_4$, the moment that $V_O$ transfers to $V_{O2}$, which is lower than $V_{O1}$. And the reason is that $\Delta W$ causes additional loop resonance in the secondary synchronous rectifiers. Therefore, the resonance caused by $\Delta W$ brings additional reverse voltages stresses to SRs, and then $V_{DSmax}$ is much higher than the normal mode with synchronous rectification.

The additional higher stresses on SRs will cause more difficulties in designing high efficiency high performance power supplies. Therefore, effective measures should be taken to suppress the stresses into acceptable lever without other problems that may arise.

### Table 1: Designation of the comment in Fig. 6

<table>
<thead>
<tr>
<th>$V_O$</th>
<th>on-board converter output voltage</th>
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</thead>
<tbody>
<tr>
<td>$V_{GSE}$</td>
<td>driving signal of $S_E$ (shown in Fig. 2)</td>
</tr>
<tr>
<td>$S_R$</td>
<td>driving signal of SRs</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage of SRs</td>
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</tbody>
</table>
lethal drawbacks. This paper proposes an optimized snubber with time-varying capacitor to suppress the plug-in and plug-out transient stresses on SRs. What is more, the novel snubber overcomes the traditional difficulties and bypass trade-off between the performance of the snubber and the lower efficiencies due to the losses of the snubber.

III. DESIGNING CONSIDERATIONS OF THE OPTIMIZED SNUBBER

In figure 2, optimized snubber with time-varying capacitor is composed of three parts. The part 1 is SR, and part 2 is the traditional RC snubber in parallel with SRs. Part 3 is the proposed snubber with time-varying capacitor $C_E$ which is in parallel with $C_S$ if switch $S_E$ is on. And $V_X$, shown in Fig. 7, is a 0–10V signal, generated by the output voltage $V_O$ and decide whether the SRs turn on at proper time that $V_O$ climbs up to the bus voltage. What is more, the maximum voltage of SRs’ driving signal follows $V_X$ (shown in Fig. 7). And the purpose of the signal $V_X$ is to delay the synchronous rectification until the moment $t_3$ (shown in Fig.4) to a proper moment that the on-board converter output voltage has flew up to the bus voltage. When plug-in operation starts, $S_E$ is off because $V_X$ does not fly up to 10V, as a result, the $S_E$ is ON which makes $C_E$ is in parallel with $C_S$, and this new RC network have a bigger equivalent capacitor:

$$C = C_E + C_S,$$

(9)

which facilities the new snubber in suppressing the additional stresses in the hot plug-in application. In Fig. 8, stresses are evidently suppressed when $S_E$ is on. If we assume that the stresses is $V_1$ without time-varying snubber in hot plug-in situation and the ideal suppressed voltage is $V_2$, then the time varying capacitor can be drawn from the expression below:

$$\frac{1}{2} \cdot C_S \cdot V_1^2 = \frac{1}{2} \cdot (C_S + C_E) \cdot V_2^2,$$

(10)

Then, we could get:

$$C_E = C_S \cdot \frac{V_1^2 - V_2^2}{V_2^2},$$

(11)

When the output voltage $V_O$ flies up to the required bus voltage, and $V_X$, at the same time, comes up to 10V, zener diode $Z_C$ breaks down and switch $V_X$ turns on, which makes $S_E$ turns off, then time-varying capacitor is cut off and get out of the stresses suppression, which can save portions of energy compared with the conventional larger time constant RC snubber. On the other hand, from Fig.2, even though $S_E$ is turned off, there is still the parasitic output capacitor of the MOSFET which in series with time-varying capacitor. Therefore, a new time-varying capacitor, which is:

$$\frac{C_E C_{OSS}}{C_E + C_{OSS}},$$

(12)

is formed and paralleling with $C_S$, helping to absorb the additional stresses and the new snubber capacitor can be expressed below:

$$C' = C_S + \frac{C_E C_{OSS}}{C_E + C_{OSS}},$$

(13)

Clearly,

$$C' > C$$

Due to this parasitic parameter-formed capacitor, it is easily
to draw from Fig 8 that the reverse voltage stresses is lower in Fig. 8 (b) than that in Fig. 8 (a) when on-board converter enters the stable state with SRs conduction after SE is off.

Carefully thinking over the time-varying concept in the application of snubber circuit and delve it into more extended applications, many new types of snubber circuit could be innovated, not only including the time-varying capacitor, but also time-varying resistor to increase the time constant of the RC snubber network, and the combination of the time-varying capacitor and time-varying resistor snubber cell. Fig. 9 shows us several time-varying snubber cells, which could be used in even more application fields with more flexibility.

Fig. 9 shows us several types of time-varying snubber cell, all of which could be used in the hot plug operation of the synchronous rectification. In Fig. 8, (D) (S) are the two definite ports which connect the drain and source of the synchronous rectifier. Besides, Fig. 9 (a) (b) (c) are members of time varying snubber with switch in series, while Fig. 9 (d) (e) (f) in parallel. What is more, Fig. 9 (a) (d) are configured only with capacitor, while (e) only with resistor and (f) the combination of resistor and capacitor.

IV. EXPERIMENTAL RESULTS

The experiment is conducted in a 48V to 12V, 300W, 1/4 brick bus converter, Fig. 8 shows the results under the maximum input of 55V, only under which can $V_{DS}$ achieves $V_{DS\text{max}}$. In Fig. 8 (a), the $V_{DS\text{max}}$ is close to 50V, while the (b) is only 40V. With the employment of the time-varying snubber, we can choose the VISHAY lower voltage lower non-resistance MOSFETs Si7156DP (N-Channel 40-V MOSFET), which on-resistance is as low as 3m$\Omega$, rather than MOSFETs Si7478DP (N-Channel 60-V MOSFET), which on-resistance is roughly 6m$\Omega$, twice as much more as that of Si7156DP, wildly increasing the efficiency in full load current mode by about 1%.

V. CONCLUSION

The stresses of SRs in hot plug-in operation are discussed. Novel time-varying snubber is proposed. Designing consideration is well addressed. Extension of the novel method is described with list of proposed novel snubber cells and detailed explanation. A prototype of 300W bus converter is designed to verify the characteristics of this idea. Experimental results are shown to demonstrate the operation principle and advantage of the proposed time-varying snubber.

REFERENCES