Single-Stage Offline SEPIC Converter with Power Factor Correction to Drive High Brightness LEDs

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Abstract An interleaved SEPIC converter with LED current dimmable and input power factor correction is proposed as a high performance driver for the high brightness white LEDs. The converter is controlled with voltage mode PWM and run in discontinuous conduction mode so that the inductor current follows the rectified input voltage. The critical design constraints and equations for both the power stage and control loop are highlighted and detailed. A practical evaluation board with 110V input and 60V, 700mA output is developed to verify the proposed design. The proposed converter can be used to drive a wide number of high brightness LEDs for industrial or commercial lighting applications.

Index: High brightness white LED, SEPIC converter, Power factor regulation, Interleaving, Voltage Mode PWM, Integrated magnetics, Dimming control, Lighting application, Offline application, Discontinuous conduction mode

1. INTRODUCTION

Worldwide, about 19% of the electric power is consumed by residential, commercial or industrial lighting. This number is 18% in Japan, and 16% in the United States [1]. In 2000, about 567TBKWH of electric energy in USA is for electrical lighting applications [2][3]. Thanks to the technology innovations in the following two aspects, the electrical lighting efficiency has increased significantly in the developed countries, and accordingly the percentage of the electric power consumption decreases, 1) The advancement of lighting materials and lighting devices; and 2) The power electronics technology to drive these devices. The commonly used lighting technologies include incandescent bulbs and halogen bulbs, fluorescent lamps, compact fluorescent lamps (CFL), and high intensity discharge (HID) lamps. Generally, the efficiency of the lighting sources is indexed by efficacy, or lumen per watt. The efficacy of typical energy saving CFL lamps is around 7~8%, compared with 2% for the conventional the incandescent bulbs. Obviously, the savings of energy is huge by replacing the conventional lighting sources with the energy saving CFL.

Low power LED has been used for battery powered applications for decades [4][5][6]. These applications include cell phone handsets, digital still cameras, automotive lighting, emergency lighting, and LCD backlighting, and so on. With the advancement of new materials and manufacture process, a new lighting source, that is, high brightness white (HBW) LED is now attracting more and more attention from both academia and industry [7][8][9][10]. Usually phosphor material is used to convert monochromatic light from a blue or UV LED to broad-spectrum white light. In 2008, Cree Inc. released XLAMP MC-E LEDs that can operate in 700mA with maximum lumen flux 490 (www.cree.com). In 2008, Philips Lumileds, released the LUXEON K2 with TFFC that can operate at 1000 mA, offering minimum flux performance of 160 lm or more (www.lumileds.com).

The high brightness white LED is environmentally friendly and energy efficient as well. Unlike the CFL, it is mercury-free, and not easy to break. It has very long lifespan (100,000 hours which is more than 10 times of CFL). Compared with all the other commonly used lighting sources, typical LED efficacy is about 30% and has much room to improve, implying much less energy consumption, and less environment impact. It can endure very high times of turns on/off. In addition, it is compact and easy to drive compared with the traditional sources. The LED lamps can be directly installed on Printed Circuit Board (PCB), as shown in Fig. 1.

Fig.1 High power LED mounted on PCB

One of the important applications of the high brightness white LED is the offline lighting for residential, commercial, and industry illuminations. It represents the largest segment and fastest growing in terms of dollar sales, according to Darnell’s survey. Although still a new technology, it is predicted that LED lighting will begin accelerating growth in general illumination applications within the next five years (www.darnell.com).

Strings of LED are connected in series and/or parallel to increase the overall brightness. The number of LED for residential lighting is around 10 to 20. For street and parking lot lighting, a total of 30 ~ 50 LEDs can be used, while for commercial lighting, hundreds of units are used to achieve high flux level. The voltage over a series of LED is the voltage drop of individual LED times the number of LED in series. The typical p-n junction voltage drop of these LEDs ranges from 2.5V to 4V. The current of a series of LED in parallel is the sum of the LED currents of all the strings.

For low power offline applications, a single-stage constant-current controlled AC/DC converter is desired with high power factor and low harmonics profile to meet the standards such as IEC-1000-3-2. There are two approaches of power factor correction in single-phase offline power converters [11]~[17]. The first method is the so-called active power factor correction, where the input current is forced to follow the input voltage by active control of the inductor current as in a boost converter. A slow output voltage feedback loop is employed together with a fast current loop. The input voltage signal is needed to generate the reference signal. Current signal may also need for some control schemes, depending on how the current control loop is implemented. In general, there are three analog schemes, that is, average current control, peak current control and hysteresis control. The simple block-diagram is shown in Fig 2.a. The advantages for the active power factor correction include, 1) The converter can run in continuous conduction mode (CCM) that allows for full utilization of the components, 2) High power factors over wide input line/output load combinations, 3) High efficiency. However a dedicated power
factor correction controller is needed and usually need two stages of power conversion.

The other approach is the so-called voltage follower, where the input current naturally follows the input voltage by running the converter in discontinuous conduction mode (DCM). The simple block diagram is shown in Fig. 2b. Since the converter operates in DCM with fixed switching frequency and fixed duty ratio, the input inductor current is proportional to the input voltage in each switching period, and the envelope of the input current follows the input voltage. Obviously, no PFC controller is needed, and current/voltage signal is not needed. It is widely used in the low cost low wattage applications.

A number of topologies can be used as a voltage follower, for instance boost, buck-boost, CUK and flyback converters. Flyback converter is one of the frequently used topologies for low power low cost ac/dc conversions. Running it in discontinuous conduction mode, the current of the primary inductance of the transformer always goes to zero in each switching period. Proper snubber circuit is needed to suppress the high voltage ring caused by the leakage inductance of the flyback transformer. One another commonly used topology is the single-ended primary isolation converter (SEPIC). Compared with the flyback converter, it does not have a transformer and the associated leakage ring effect. It can also be designed for wide range of voltage conversion ratio. In addition, the input inductor current in DCM follows the input voltage with much smaller ripple current as compared with the flyback and boost converters. Isolated SEPIC converter uses a transformer to replace the second inductor. The two magnetic components apparently increases the cost, but can be integrated with one magnetic core in real applications.

A PWM controller with the same saw-tooth carrier signal to generate two PWM signals (PWM A, PWM B) with 180 degree output of phase is used to control the duty ratio of the two switches. The LED brightness is regulated by the current feedback loop. A Type I Error Amplifier integrates the difference between the actual LED current and the reference I_{LED} and generates the PWM modulation signal, which then changes the duty ratio and regulates the LED brightness. Since the EA is designed to have much low bandwidth, the modulation signal will keep almost constant within each line cycle. The interleaved SEPIC converter is designed to run in discontinuous conduction mode. As a result, both of the two converters operate with a constant duty ratio, and the inductor currents of all the 4 inductors will reset to a constant value after each switching period. The envelope of the currents in the input inductors follows the rectified input ac voltage, which results in high power factor and low harmonics. Two kinds of protections are provided, output over-voltage protection, and over-current protection. This circuit is very suitable for offline ac/dc power conversion for high brightness white LED lighting for commercial, residential and industry applications.

Interleaving technology has been widely used in the buck derived topology such as voltage regulation modular (VRM) [21][22][23][24], to reduce the filter size, and increase the dynamic performance. The mechanism is that through interleaving of the paralleled converters with phase shift of each other, the dominant ripple frequency in the passive component is a multiple of the switching frequency of each single converter. Some ripple can be totally cancelled due to the phase shift. Therefore, the size of the harmonics and EMI filter can be greatly reduced. Such technology has also been reported in boost, and buck-boost converters to reduce the input ripple current.

In this paper, we investigate an interleaved SEPIC converter driver for LED lighting applications. The PWMs of the two phases are 180 degree out of phase. The LED brightness is dimmed by the LED current which is controlled by a slow current feedback loop. The design will be verified with experimental results.

II. INTERLEAVED SEPIC CONVERTER

A two-phase interleaved SEPIC converter for ac/dc offline LED applications is shown in Fig. 3a, where D_{1a,b} and D_{2a,b} are the rectifiers. C_{1a} is a small high voltage capacitor. The function of this capacitor is to filter out switching harmonics. L_{1a,b} and L_{2a,b} are the input inductors. C_{2a} and C_{2b} are the high voltage capacitors. D_{1a,b} and D_{1a,b} are the output diodes, and C_{1} is the output capacitor. S_{a} and S_{b} are the two switches. C_{2a} and C_{2b} are the voltage signals of the currents in the two switches S_{a} and S_{b}.

![Fig. 2 Single-phase offline power conversion](image)

![Diagram of Active Power Factor Corrector and Voltage Follower](image)

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The gate drive signal of the switch is generated by comparing the saw-tooth carrier signal of the PWM controller with the current feedback signal. The PWM signals for a two phase interleaved converter are generated with the logic schematic in Fig 3b, where it consists of two comparators, two AND gates and one D Flip-Flop. The operation waveforms are shown in Fig 3c. The clock signal is generated by comparing the carrier signal with a constant DC voltage. This clock signal is then sent to the DFF to generate two complementary signals of 50% duty and 180 degree out of phase. In the meanwhile, the carrier signal is compared with the modulation signal to generate the PWM signal. This PWM signal is AND with the two signals from the DFF to generate the PWM for the two switches.

The operation mechanism of the interleaved converter can be explained with the help of the waveforms shown in Fig 4a, and equivalent circuits in Fig. 4b. Altogether, there are 6 distinctive intervals (I1 ~ I6). Owing to the factor that the switching waveforms for both switches are the same for the successive switching periods, the circuit operation mechanism can be analyzed for only one phase of the converter. Consider the circuit with switch A, it has three different operation intervals depending on the current variations in switch S_{a} and diode D_{a}.

1) Charge interval. The switch S_{a} turns on for a period of time T_{on}, the diode is off. Both inductors are charged and the currents ramp up linearly. 2) The switch S_{a} turns off, the diode is on for a period of T_{off}. Both inductors currents discharge through the diode and inductors currents ramp down linearly. 3) The switch S_{b} and diode are off. The two inductors make up a loop. The inductors current are the same. There is no change in the inductor currents. This interval lasts for T_{off}. As long as T_{off} is greater than zero, this operation mode is regarded as discontinuous conduction mode (DCM). The equivalent circuits for T_{on}, T_{on} and T_{off} are shown in Fig 4b.

During each switching period, the following circuit equations can be derived.

1) Interval I1: switch S_{a} turns on, S_{b} is off

Assume the voltage of the capacitor C_{2} tracks closely the C_{j} voltage which is the rectified input voltage. Before switch S_{a} turns on, the freewheeling current in L_{1a} is I_{1a}. As the switch S_{a} is turned on, voltage applied to the input inductor L_{1a} is V_{dc}. Since the voltage across C_{2a} equals V_{dc}, the same voltage is applied to L_{1a}. Hence both inductors L_{1a} and L_{1b} see the same positive voltage, and are charged up linearly with a slope dependent on the inductance. The diode D_{1a} is reverse biased. The inductor currents are given in (1).

The switch current is the sum of the two inductor currents, and is given in (2), where Z0 denote the initial state of the state variables. During this
interval, the currents in the inductors $L_{1a}$ and $L_{2a}$ are freewheeling. The equivalent circuit is given in Fig.4.b.

\[ i_{L1a}(t) = \frac{v_{c1} - v_{c2}}{L_{1a}} \quad i_{L2a}(t) = \frac{v_{c2}}{L_{2a}} \quad i_{L1a(0)} = -i_{L2a(0)} \quad (1) \]

\[ i_{L2a}(t) = \frac{v_{c2}}{L_{2a}} \quad i_{L2a(0)} = i_{L2a(0)} \quad i_{L1a(0)} = 0 \quad (2) \]

Since the initial currents in the inductors are the same, the switch current is zero at turning on, indicating that the switch turn on loss is eliminated. Because the duty ratio $D$ is approximately constant within one line period, the inductor charge current slope changes with the rectified ac voltage. The peaks of the inductor currents are in proportion to the rectified ac voltage. The energy stored in the inductors is in proportion to the square of the peak inductor currents.

2) Interval I2: switch $S_a$ turns off, $S_b$ is on, diode $D_{1b}$ is on

During this interval, the switch $S_a$ is turned off. The inductor current $I_{L1b}$ freewheels through $C_{2b}$ and the diode $D_{1b}$ to charge the output capacitor $C_o$. The inductor current $I_{L2b}$ freewheels through diode $D_{1b}$ to charge the output capacitor $C_o$. The voltage applied to inductor $L_{1b}$ is $-V_{ac}$ same as inductor $L_{2b}$. Therefore the inductor $L_{1b}$ current reduces according to (3). The $L_{2b}$ current reduces and reverses. This stage ends when $i_{L2b}$ equals $-i_{L2b}$. The diode $D_{1b}$ current is the sum of both the inductor currents. The currents are given in (4). At the end of this interval, the inductor currents equal and the output diode is off with zero current switching off. During this period, the other phase keeps the same state as previous one. The equivalent circuit is given in Fig.4.b.

\[ i_{L1b}(t) = \frac{v_{c1}}{L_{1b}} - \left( \frac{v_{c1}}{L_{1b}} \right)(t - T_m) \]

\[ i_{L2b}(t) = \frac{v_{c2}}{L_{2b}} \quad \left( \frac{v_{c2}}{L_{2b}} \right)(t - T_m) \quad (3) \]

\[ i_{D1b}(t) = \left( i_{L1b(0)} \right) \left( \frac{v_{c1}}{L_{1b}} \right) \quad \left( \frac{v_{c2}}{L_{2b}} \right)(t - T_m) \quad (4) \]

It is noted that although the inductor current charge slope varies with the rectified ac voltage, the current discharge slope is constant, regardless how the input voltage changes. Therefore, around peak of the ac voltage, the discharge time is longer than the
reset of the instants. The diode conducting time can be estimated by the volt-sec balance of the inductors, and given in (5).

\[ T_d = \frac{T_{sw}}{V_o} v_{cl}(t) \]  

(5)

3) All the diodes and switches are off

This is the freewheeling period of both inductors \( L_1 \) and \( L_2 \). In this interval, all the switches and diodes are off. The current variation or energy change of the two inductors is zero. The freewheeling currents are given in (6) and (7).

\[ i_{11}(t) = i_{120} + \frac{V_{cl}}{L_{1a}} T_{sw} - \frac{V_o}{L_{1a}} T_d \]  

(6)

\[ i_{12}(t) = i_{120} + \frac{V_{cl}}{L_{2a}} T_{sw} - \frac{V_o}{L_{2a}} T_d \]  

(7)

After this interval, the other phase begins the same procedure as the above, and the operation will be the same.

Fig. 5 The current waveforms

The current waveforms over half of the line period are demonstrated in Fig. 5 with reduced switching frequency. It is noted that the input line current is continuous and the ripple is much lower than the alternative solutions such as in a boost converter, or flyback converter run in DCM. Also noted is that both the input and output ripple frequency is doubled and therefore the actual filter size can be reduced.

The operation of the output circuit depends on the output current, total inductor current and the instants of operation. Around the valley of the rectified ac input, there is an instant where the output capacitor is discharged, and the load current is increased. The maximum instantaneous value of the load current, \( I_{LED} \), is then the rectified sinusoidal ac voltage, and is given in (8).

\[ I_{LED} = \frac{V_{cl}}{2} \int_{t_d}^{t_{sw}} \left( I_{cl}(t) - I_{LED} \right) dt \]  

(8)

The ripple current is corresponding to the valley of the rectified ac voltage, where the output capacitor voltage keeps decreasing, and the frequency is twice of the line frequency. Because of the factor that the input current is in phase with the input voltage, and is harmonic free, it is evident, that the instantaneous input power pulsates at twice of the line frequency, where \( I \) denotes input ac line, \( V_I \) is the amplitude of the input ac voltage with line frequency \( \omega_l \).

\[ p(t) = V_I \sin(\omega_l t) I \sin(\omega_l t) = \frac{V_I I}{2} (1 - \cos 2\omega_l t) \]  

(9)

At the output port, the ripple voltage is comparatively very small, and the load current is basically DC. Therefore the output power of the load is active power dominant. Hence, the ripple of twice of the line frequency is expected in the output voltage, which is the ac term in (9), and is estimated according to (10). Hence, the voltage ripple can be estimated according to (11).

\[ p_{\Delta}(t) = \frac{V_I I}{2} \Delta I_c = V_o C_s \frac{\Delta V_c}{\Delta t} \]  

(10)

\[ \Delta V_c = \frac{\Delta V_c I_s}{2V_o C_s} \]  

(11)

This ripple component is much higher in amplitude and lower in frequency and is the major ripple to be considered. To reduce the ripple, the output capacitor needs to be selected according to (11).

III. DESIGN CONSTRAINTS AND GUIDELINE

A DCM CONDITIONS

Assume the impedance of the power source is ignorable, and the voltage drop over the rectifier bridge is omitted. The input capacitor \( C_I \) filters out all the high order switching ripple current, but does not change the waveform of the rectified input ac voltage, the voltage across \( C_I \) is then the rectified sinusoidal ac voltage, and is given in (12), where \( V_I \) is the amplitude of the input ac voltage with line frequency \( \omega_l \).

\[ v_{cl}(t) = V_I \sin(\omega_l t) \]  

(12)
Also assume the equivalent resistance $R_s$ represents the load and power loss of the converter, then the average input power seen from capacitor $C_i$ is represented with the equivalent resistor as in (13).

$$P_i = V_i I_i / 2 = V_i^2 / 2R_s$$  \hfill (13)

The output current $I_o$ in one switching period is the average of the current in the output rectification diode, and $I_o = L_p / T_o / 2$, where $T_o$ is the conduction interval of the output diode. One can find the criteria for selecting the inductances in these converters for DCM by considering the factors that the power-balance in the input and output ports, and that the freewheeling time should be larger than zero.

Since the voltage applied to the inductors changes over time within one line period, the worst case occurs when the rectified ac voltage reaches around peak and the circuit runs with high line voltage, which is 275V for universal input design. Around these voltages, the peak inductor current reaches maximum. With the factor that the inductors are reset with the same output voltage, the voltage reaches around peak and the circuit runs with high line within one line period, the worst case occurs when the rectified ac voltage reaches the intermediate capacitor and power loss of the converter, then the average input power seen from the capacitor is represented with the equivalent resistor as in (13).

$$P_i = V_i I_i / 2 = V_i^2 / 2R_s$$  \hfill (13)

The output current $I_o$ in one switching period gives half of the average output current $I_{av}$, and hence the average of the output capacitor current is zero, that is, $I_{cap} = 0$. Around the peak of the ac voltage, because of the voltage-second balance, that is, $T_{av} V_i = T_{av} V_o$. Obviously (14) also implies that the duty ratio $d$ must be less than $V_o / (V_o + V_j)$, where $V_o$ is the LED voltage, which changes with LED current.

$$d < V_o / (V_o + V_j)$$  \hfill (15)

Averaging one diode current in (4) over one switching period gives half of the average output current $I_o(t)$. The total output current over one switching period is given in (16). From (16), one can see that the output current is related to the paralleled inductance of the pair inductors in one phase, $L_1a$, $L_2a$. It is evident that the dominant ripple frequency is twice of the line frequency.

$$I_o(t) = rac{1}{T_o} \int_{0}^{T_o} i_{1a}(t) dt = \frac{1}{T_o} \frac{T_o}{2} \frac{V_t}{T_o}$$  \hfill (16)

Because the average of the output capacitor current is zero, the output current equals the average of the diode current. And average the $I_o(t)$ over one line period, gives the average current of the output as given in (17), which is the same as the average of the $L_2a$ or $L_2b$ current, since the average current of $C_{2a}$ and $C_{2b}$ is also zero.

$$I_{av} = \frac{1}{T_o} \int_{0}^{T_o} I_o(t) dt = \frac{1}{T_o} \frac{T_o}{2} \frac{V_t}{T_o}$$  \hfill (17)

With unit power factor, and power conversion efficiency $\eta$, the equation for the duty ratio $d$ can be derived as shown in (19), which is a function of the output power and input voltage. The duty ratio versus input voltage and output power is plotted in Fig. 7. The duty ratio becomes very small at high line. The rising and falling time become comparatively significant and the inaccuracy of the duty ratio can have negative effect on the current waveform quality.

$$d = \frac{1}{2} \frac{V_o I_o / \eta}{V_o I_o} = \frac{V_o I_o / \eta}{V_o I_o}$$  \hfill (18)

$$d = \frac{1}{2} \frac{V_o I_o / \eta}{V_o I_o} = \frac{V_o I_o / \eta}{V_o I_o}$$  \hfill (19)

From (14), (15) and (17), we get in (20) the constraints for selecting the inductors. As the LED voltage depends on the current, the critical inductance can be found once the LED current is determined. Similar to the V-I curve of commonly used diode curve, the voltage becomes almost constant for high current. Therefore, the critical inductance is almost in reverse proportion to the LED current for high current. Fig. 8 plots the critical inductance versus LED current for different input voltages with the V-I curve of 21 high power white LED in series.

$$L_{1a} = \frac{V_o}{I_o} \frac{V_t}{2 I_o}$$  \hfill (20)

Fig. 7 The duty ratio $d$ versus input voltage and output power (Assume 80% of efficiency, $L_{1a,b} = 560uH$, $L_{2a,b} = 56uH$, $f_s = 200kHz$)

Fig. 8 The critical inductance versus LED ($f_s = 200kHz$, 21 LED)

One other constraint for selecting the inductance is the input current ripple. The input current ripple is dependent of the input power, the intermediate capacitor $C_{2a}$ and the inductance of $L_{1a}$. As can be seen from (1), the maximum ripple current of the input inductor $I_{1a}$ occurs at the peaks of the rectified input voltages $(\omega t = k \pi$, $k = 1,2,3,...)$, that is,

$$I_{1a} = \frac{V_o}{I_o} \frac{V_t}{2 I_o}$$  \hfill (21)

Define the current ripple factor $K_{rp}$ as the ratio of the current ripple to the input current. $K_{rp} = I_{1a} / I_o$, where $I_o$ is the peak of the input current, then the constraints for selecting of the two inductors are given below to keep small ripple in the inductor $I_{1a}$ and $I_{1b}$. From (22), we get the $K_{rp}$ factor of the inductors in (23), which is usually very large.

$$L_{1a} > \frac{V_o}{I_o} \frac{V_t}{2 I_o}$$  \hfill (22)

$$L_{2a} > \frac{V_o}{I_o} \frac{V_t}{2 I_o}$$  \hfill (23)

The peak current of the inductors occurs when $\omega t = k \pi$, $k = 1,2,3,...$ at worst line/load conditions, according to (1). At the peak of the input voltage, the charge is balanced for the intermediate
capacitor \( C_{2a} \). Therefore, with reference to the capacitor current waveforms in Fig. 9, we have (24), from which, we get the freewheeling current at the voltage peak in (25).

\[
0 = I_{t2}\text{on}(t) + I_{t2}\text{off}(t) - I_{t1}\text{on}(t),
\]

\[
I_{t1}\text{on}(t) = \frac{V_o}{2L_{1a}}\left(\frac{V_o}{L_{1a}V_T} - \frac{1}{L_{1a}}\right)I_{LED}
\]

As can be seen from the schematic in Section 3.3, it is important to keep the inductor current positive. Otherwise, the negative current will charge the input capacitor (which is small), so that the input voltage waveform is deviated from a rectified sinusoidal ac voltage. Obviously from (25), in order to keep the inductor current positive, the following constraint in (26) must be met. The inductors should be selected according to (20), (22) and (26). To simplify the design, let \( L_{1a} > L_{2a} \) and \( L_{1b} > L_{2b} \). Then inductor \( L_{2a}, L_{2b} \) can be selected according to (20), with \( L_{1a} = K^*L_{2a}, L_{1b} = K^*L_{2b} \), where \( K > \max \{K_1, K_2\} \).

\[
\frac{L_{2a}}{L_{1a}} > \frac{V_o}{I_a} = K_2
\]

The peak and RMS current of the inductors are given below as a reference for selecting proper inductors.

\[
I_{t1,\text{pk}} = \frac{V_o}{L_{1a}}T_{on(a)} + I_{t1,\text{off}(t)}
\]

\[
I_{t2,\text{pk}} = \frac{V_o}{L_{1a}}T_{d} - I_{t1,\text{off}(t)}
\]

\[
I_{t1,\text{rms}} = \frac{T_{on(a)}}{T_a} \left(\frac{\Delta I_{1a}^2}{3} + I_{t1,\text{off}(t)}I_{t1,\text{off}(t)}^* + I_{t1,\text{off}(t)}^*\right)
\]

\[
I_{t2,\text{rms}} = \frac{T_{d}}{T_a} \left(\frac{\Delta I_{2a}^2}{3} - I_{t1,\text{off}(t)}I_{t2,\text{off}(t)} + I_{t1,\text{off}(t)}\right)
\]

The power factor performance of the converter largely depends on the size of the intermediate capacitor \( C_{2a} \), \( C_{2b} \). As we have assumed in the previous analysis that the intermediate capacitor voltage track the rectified ac voltage closely. This implies that the capacitance should be large enough to hold the voltage constant within one switching period. The ripple voltage of the capacitor \( C_{2a} \) can be estimated by integration of the current during turn on interval, or \( C_{2b} \) during turn on interval. The worst case condition occurs when the rectified ac reaches the peak or \( \tilde{v}_m = k\tilde{v}_r \).

\[
\Delta V_{C_{2a}} = \frac{1}{C_{2a}} \int_{t_{on(a)}}^{t_{off}(t)} I_{t2}(t) dt = I_{t2}\text{on}(t) + I_{t2}\text{off}(t)
\]

Therefore, the capacitance relating to the ripple voltage of the intermediate capacitor \( C_{2a} \) is given below.

\[
C_{2a} = 1 + \frac{2T}{f}\frac{P_o}{L_{2a}}
\]

Define the voltage ripple factor of \( C_{2a} \) as \( K_{rsv} \). \( K_{rsv} = \Delta V_{C_{2a}}/V_0 \), inserting the ripple factor into (31), and get (34).

\[
C_{2a} = \frac{\sqrt{2T (L_{2a} \times L_{1a})}}{f R_{rsv} R_{rsv} R_{rsv}}
\]

The equivalent resistance in the input port and output port are defined below. The minimum capacitance of the intermediate capacitors is plotted in Fig. 10. Obviously the right capacitance should be selected to meet this minimum requirement but as small as possible. Too small capacitor can result in high input ripple current. Too large capacitor will distort the current waveform especially during the rising edge of the rectified sinusoidal voltage waveform.

\[
R_{rsv} = V_o l_a, R_{rsv} = \frac{V_o}{I_a}
\]

**Fig. 10 The minimum capacitance of the intermediate capacitor C2a, C2b versus LED current (Assume 80% of efficiency, \( L_{1a,b} = 560uH, L_{2a,b} = 56uH, f_r = 200kHz, K_{rsv} = 0.1 \)**

Selecting the output filter capacitor is based on the output voltage ripple requirement. The ripple of twice of the line frequency is expected in the output voltage because of the power factor correction. To reduce the ripple, the output capacitor needs to be selected according to (35) with good high frequency characteristics.

**IV. DIMMING AND FEEDBACK CONTROL**

There are two kinds of dimming for LED lighting. One is to control the LED average current, and the other is to control the lux of the LED lamp. Since the brightness or the lux of a LED lamp is not linearly related to the LED current in the whole operation range of the LED, a current based method can’t give a linear brightness control curve. A lux based method is to adjust the LED brightness directly using some light sensor, for example, ISL29101. This device has an output voltage in proportion to the visible light intensity from 0.5 lux up to 10,000 lux, with a bias voltage from 1.5 to 3.3V. The only disadvantage of such method is the addition of light sensor circuit, which compared with the total cost of the LED lamps, is ignorable.

The LED current based control, only current sense resistor or sometimes an op-amp is needed. So it is relatively a low-cost solution. There are two methods, one is to control the LED current by PWM and the other is to change the reference of the control loop. In the PWM method, the LED current is controlled by a small power MOSFET, the duty ratio \( D \) of which varies for dimming. Some controllers based on this dimming method include: ISL97801 and automotive LED controller ISL78100. In these dimming circuits, a low power MOSFET is connected in series with the LED string. The MOSFET is controlled by the PWM of the dimming frequency \( f_d \). At \( D/f_d \), the LED conducts a constant current \( I_o \). So the tune of the color does not change with the brightness. At \( (1-D)/f_d \), LED current is turned off. The LED can be turned on and off very fast without any negative effect. The average of the LED current is \( DI_o \). Hence the
frequency can be around 0.5 to follow the current change in the load. As a trade-off, the cut-off ratio of the converter is not disturbed by the power pulsation, or ripple in the load current. On the other hand, it should be fast enough to respond to the change in the lighting applications.

In a DC dimming method, the reference is derived from a constant 5V source and is changed using a variable resistor or digital controlled resistor. The second method is the AC dimming. In this method, the reference is in proportion to the input ac average voltage. Therefore, the widely used traditional dimmer can be used in combination to adjust the LED current. Both of these methods regulate the LED current to adjust the LED brightness.

For the discussed circuit for lighting application, the brightness of the LED lamp is regulated by the LED current. The duty ratio can be controlled by the difference between the reference signal \(I_{ADJ}\) and the voltage across the current sense resistor \(R_c\). The \(I_{ADJ}\) can be set by variable resistor from a constant voltage source. This can be implemented in combination with some existing remote control circuit. By changing \(R_c\) or \(I_{ADJ}\), the brightness of the LED can be dimmed. The reference can also be set to be proportional to the ac line voltage. In this case, the ac line voltage can dim the brightness of the LED. Such a solution is attractive in large building illumination. Furthermore, in the street lighting applications or parking lot lighting applications, \(I_{ADJ}\) can also be derived from light sensors. The block diagram of conceptual control diagram is shown in Fig. 12.

Type I-EA can be used with the crossover frequency determined by the feedback capacitor \(C_{fb}\) and the resistor \(R_c\), given in (36).

\[ \omega_c = 1/(RC_{fb}) \]  

The bandwidth should be less than the line frequency, so that the duty ratio of the converter is not disturbed by the power pulsation, or ripple in the load current. On the other hand, it should be fast enough to follow the current change in the load. As a trade-off, the cut-off frequency can be around 0.5 \(\omega_0\).

Over voltage protection circuit is needed, due to the nonlinearity of the diode current and voltage relation. This is implemented by a comparing the output voltage with a constant reference voltage. Once the output voltage reaches the threshold, the PWM controller should be shutdown, and wait for a while before starting the next soft-start up. Therefore, a hiccup mode over voltage protection is adopted.

![Conceptual control diagram of the dimming control](image)

**Fig. 12 Conceptual control diagram of the dimming control**

V. EXPERIMENTAL VALIDATION

Prototype circuit was setup to verify the proposed design. Altogether 21 high power LEDs from Cree Co. are used as the load. The maximum output power is about 60W. The LED driver input voltage ranges from 80V to 140V. The design specifications are given in Table I.

**Table I**

<table>
<thead>
<tr>
<th>MAIN DESIGN PARAMETERS</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input ac voltage</td>
<td>80 V–140 V, 60Hz</td>
</tr>
<tr>
<td>Output current</td>
<td>50 mA ~ 700mA</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Typical efficiency</td>
<td>85%</td>
</tr>
<tr>
<td>Typical power factor</td>
<td>&gt; 0.95</td>
</tr>
<tr>
<td>Output voltage ripple</td>
<td>&lt; 5%</td>
</tr>
<tr>
<td>Number of LED in a string</td>
<td>21</td>
</tr>
</tbody>
</table>

Evaluation boards were built in the Lab and tested to verify the design. The main circuit component values and parameters are given according to the design equations in Section II and given in Table II.

**Table II**

<table>
<thead>
<tr>
<th>MAIN COMPONENT PARAMETERS AND VALUES</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Separin inductor, (L_{ia} L_{ib})</td>
<td>560 (\mu)H</td>
</tr>
<tr>
<td>Separin output inductor, (L_{oa} L_{ob})</td>
<td>56 (\mu)H</td>
</tr>
<tr>
<td>Input ceramic capacitor, (C_1)</td>
<td>240 (n)F</td>
</tr>
<tr>
<td>Intermediate ceramic capacitor, (C_2)</td>
<td>1 (\mu)F</td>
</tr>
<tr>
<td>Output electrolye capacitor, (C_3)</td>
<td>680 (\mu)F</td>
</tr>
<tr>
<td>Feedback capacitor, (C_{fb})</td>
<td>2.2 (\mu)F</td>
</tr>
<tr>
<td>Feedback resistor, (R_{fb})</td>
<td>10 (\Omega)</td>
</tr>
<tr>
<td>Power MOSFET, (S_i S_j)</td>
<td>SPD03N60C3</td>
</tr>
<tr>
<td>Power Diode, (D_i D_j)</td>
<td>BYG24J</td>
</tr>
<tr>
<td>High brightness white LED</td>
<td>XREWHT-L1</td>
</tr>
<tr>
<td>Voltage mode PWM controller</td>
<td>ISL6745</td>
</tr>
</tbody>
</table>

The operation waveforms of a two-phase interleaved SEPIC converter are shown below in Figs 13 and 14. Fig 13 shows the operation waveforms of the drain to source voltage of the two MOSFET around peak and valley for ac line 120V. From these waveforms it is noted that the two PWM signals are 180 degree out of phase, and there are three distinct operation intervals as described in the previous sessions.

Figs 14 show the rectified ac voltage and the input current waveforms for low line high current, and high line low current conditions, respectively. The rectified voltage across the input capacitor tracks the input voltage very well. Obviously, the line current follows the input voltage closely. For both low-line and high-line operations, the measured power factors are 0.95 and above.
Fig 13 The drain-source voltages of the MOSFET.

The voltage across the LED strings (of 21 LED in series) is shown in Fig 15. The ripple of the output voltage is governed by Equation (35), and is in proportion to the output power. For the same size output capacitor, the ripple is less than half of the one with only one converter. The reduced ripple allows for smaller size output and input filter. The power factors versus input voltage for different LED currents are shown in Fig 16. For most of the operation conditions, the power factor is above 0.95.

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VI. CONCLUSIONS

In this paper, we proposed a high power factor SEPIC converter solution for high brightness LED lighting applications. The converter is controlled with voltage mode PWM so that the converter has high power factor, and can handle high power with reduced number of component count. The critical design constraints and equations for both the power stage and control loop are highlighted and detailed. A practical evaluation board is developed to verify the proposed design.

REFERENCE