A Novel Monolithic Self-Synchronized Rectifier

H. Jia\(^1\), X. Cheng\(^{1,2}\), X. Wang\(^{1,3}\), P. Kumar\(^4\) and Z. J. Shen\(^1\)

\(^1\)School of Electrical Engineering and Computer Science
University of Central Florida, Orlando, P.O. Box 162450, FL 32816, USA
Tel: 407-823-0379, Fax: 407-823-5835, E-mail: johnshen@mail.ucf.edu
\(^2\)Currently with Freescale Semiconductor, Tempe, Arizona
\(^3\)Currently with Cherokee International, Santa Ana, California
\(^4\)Intel Corporation, Hillsboro, Oregon

Abstract- A monolithic self-synchronized rectifier concept for DC/DC converter applications is presented in this paper. The smart rectifier integrated with a power MOSFET and control circuitry operates based on its drain-source voltage, and does not need external control input. The analysis, simulation, design considerations, and fabrication of the proposed concept are described in detail. Experimental results show that the proposed rectifier functions as designed. Since no dead-time control needs to be used to switch the SyncFET and CtrlFET, it is expected that the body diode losses can be reduced substantially comparing with the conventional synchronous rectifier. The proposed smart rectifier can be operated at high frequency and maintains high efficiency over a wide load range.

I. INTRODUCTION

Power MOSFETs are the most fundamental building block of DC/DC converters and can be used as both control switches and synchronous rectifiers. A synchronous rectifier (SR) MOSFET offers a significantly lower conduction loss than a PN or Schottky freewheeling diode [1]-[3]. Each synchronous rectifier structure consists of a controlled MOS channel and an integral body diode which is in anti-parallel to the MOS channel. The body diode is inherent to the structure of the SR-MOSFET and turns on whenever the drain-source voltage \(V_{DS}\) is reversed during a typical switching operation. Given the fact that MOSFET conduction and switching losses have been reduced substantially in the past years [4]-[7], the body diode loss will contribute to a substantial portion of the total losses in the future due to the large forward voltage drop and reverse recovery characteristics of the PN diode. The body diode power loss will present a fundamental technical barrier for meeting performance and efficiency requirement of future DC/DC converters as they migrate into higher switching frequency ranges [8]-[10].

The objective of this paper is to develop a smart synchronous MOSFET with significantly reduced body diode power loss without employing an additional Schottky diode. More specifically, we propose to investigate a smart auxiliary circuit approach to enable the synchronous MOSFET to operate in a self-synchronized fashion similar to a simple diode. We verify the concept with extensive circuit simulation and a prototype device fabricated with AMIS 0.5\(\mu\)m CMOS technology through MOSIS services.

Compared to the prior work on the smart rectifier concept [11]-[16], this work has the following advantages. First, we use a fully monolithic design with the power MOSFET, driver circuitry, control circuitry and necessary protection circuitry all integrated into a single silicon chip. Second, we target a higher operation speed which allows the smart rectifier to operate at a frequency up to 2MHz over a large range of load current. Even at very light load conditions, the smart rectifier should still maintain a high-speed and high-efficiency operation.

II. CONCEPT

Fig. 1 depicts the concept of the smart self-synchronized rectifier along with a conventional buck converter using an...
externally controlled synchronous rectifier. The proposed self-synchronized rectifier consists of a synchronous MOSFET and an auxiliary control circuit. The core of the auxiliary circuit is a high-speed voltage comparator which senses $V_{DS}$ of the SyncFET and generates a control signal accordingly to switch the SyncFET. When the CtrlFET is on, the SyncFET is off and has a $V_{DS}$ close to the input voltage $V_{in}$ (e.g. 12V). The voltage comparator therefore outputs a logic “0” signal and keeps the SyncFET off. When the CtrlFET turns off, the inductor current will start to freewheel through the body diode of the SyncFET, and $V_{DS}$ of the syncFET becomes negative. A negative $V_{DS}$ triggers the output of the voltage comparator to logic “1”, and turns on the SyncFET to carry the inductor current through its MOS channel. The smart rectifier doesn’t need any external control signals. It automatically adapt to the switching operation of the CtrlFET. The SyncFET only turns on after the CtrlFET turns off and it will turn off before the CtrlFET turns on completely. So the “break-before-make” control is automatically realized and no external dead-time control circuit is needed.

III. DESIGN CONSIDERATIONS

The block diagram of the proposed self-synchronous rectifier is shown in Fig. 2. The POR (Power On Reset) block works like a UVLO (Under Voltage Lock Out), which generates a reset signal (active) to ensure the SyncFET stays off during the power on stage. When the power supply ramps to above 2V, the reset signal turns to low level (inactive). The control circuit starts to function normally. The current source provides proper bias for the voltage comparator. The voltage comparator and control function blocks in our design have distinct features and are described as the follows.

A. Voltage Comparator

The voltage comparator is a critical function block of the self-synchronous rectifier. Dynamic response time and offset voltage are the two most important parameters for its design. A high-speed comparator can minimize the time during which the body diode conducts current and therefore reduce the diode power loss. Offset voltage ($V_{OS}$) is a measure of the accuracy of a voltage comparator. A low offset voltage leads to high accuracy, but inadvertently degrade the dynamic response time. This is because a low offset voltage requires large device size (which results in large capacitance) for good matching while a fast dynamic response time needs small capacitance to minimize the delay time. As shown in the simulated dynamic response waveform in Fig. 3, the propagation delay of the voltage comparator is approximately 10 ns in our final design.

If an ideal voltage comparator is used, zero-crossing $V_{DS}$ detection should be realized in the self-synchronized rectifier. However, non-zero input offset voltage is the mostly like case for the non-ideal nature of practical voltage comparators. $V_{OS}$ serves as the reference voltage of the voltage comparator, and directly affects the delay time of the SyncFET switching. In the prior work [15], a small positive offset voltage of a few mV was designed so that the SyncFET will turn on quickly when the CtrlFET switches off, as shown in Fig. 4. In reality, however, the body diode of the SyncFET still turns on for a short time period due to the delay of the control circuitry. The positive $V_{OS}$ will cause an even larger turn-off delay of the SyncFET when the CtrlFET turns on. The SyncFET has to conduct a large amount of shoot-through current before it turns itself off, as shown in Fig. 4. The large turn-off delay and cross-conduction loss limits the frequency range that this approach can be applied.

![Fig. 2 Block diagram of the proposed self-synchronous rectifier.](image1)

![Fig. 3 Simulated dynamic response of the voltage comparator. The propagation delay is about 10 ns.](image2)

![Fig. 4 $V_{DS}$ waveform of the SyncFET when a small positive offset voltage $V_{OS}$ is used.](image3)
A small negative offset voltage can be used to minimize the turn-off delay and improve the shoot-through problem associated with a positive offset voltage. However, it may cause oscillation under light load condition as shown in Fig. 5. Under light load conditions, the inductor current becomes very small (even operates in DCM), and \( V_{DS} \) (the product of \( R_{DS(on)} \) and inductor current) may rise above \( V_{OS} \). The voltage comparator output will switch from high to low, and turn off the SyncFET. However, this would force the inductor current to flow through the body diode, and bring \( V_{DS} \) again to below \( V_{OS} \). The SyncFET turns on again at that point. Once SyncFET turns on, the voltage comparator output will switch again. So the oscillation occurs. The oscillation results in repetitive on and off of the SyncFET and a large gate drive power loss.

In this paper, we propose to use a small negative offset voltage (around -6.4 mV as shown in Fig. 6) combining with a new control logic to ensure the SyncFET only turns on once in each switching cycle to avoid the oscillation and minimize non-necessary gate drive loss.

B. Control Logic

Fig. 7 shows the detail of the proposed control logic. The control circuit is mainly composed of a mono-stable circuit and a D-type flip-flop. The mono-stable circuit input is tied to the drain of the SyncFET, and triggered at the falling edge of \( V_{DS} \). The D-type flip-flop comes with a Set and Reset function. Its data input port is connected to ground, and its clock signal is tied to the output of the voltage comparator to be triggered at the falling edge. In every switching cycle, when the CtrlFET turns off, \( V_{DS} \) of the SyncFET drops below zero. The mono-stable output sets the D flip-flop. The voltage comparator output turn on the SyncFET. Under very light load conditions, the comparator output trips to low once \( V_{DS} \) goes above \( V_{OS} \). It serves as a clock signal for the D flip-flop and set Q to be zero. The low level Q signal will keep the SyncFET off until the next switching cycle. The repetitive switching ON/OFF of SyncFET at light loads is thus avoided.

Fig. 8 shows the circuit simulation result with and without the proposed logic control. It is shown that there is only one pulse to turn on the SyncFET in every switching cycle with the control logic. One drawback of this control logic is that a very small inductor current will be forced to flow through the body diode. This may introduce some power loss. But comparing to the total switching loss, this diode loss is relatively small. The triggering current for oscillation can be expressed as below.

\[
I_{\text{trigger}} = \frac{|V_{OS}|}{R_{DS(on)}}
\]
C. Physical Design

The proposed self-synchronized rectifier is designed using an AMIS C5 process, which is a 0.5 µm CMOS technology with optional 20V LDMOS devices. Special attention is paid to the physical design to minimize the offset voltage variation of the voltage comparator. The offset voltage variation of the voltage comparator generally comes from two main sources: circuit design and fabrication mismatch. Circuit design may introduce an intrinsic offset voltage due to designated devices sizes and/or circuit structures. Nevertheless, this variation can be controlled. In our design, we introduce a negative offset (around -6.4 mV). Fabrication mismatch offset usually cannot be directly controlled by the circuit designer. Yet a good layout design can help minimize it. We have adopted a split layout strategy in which each of the input pair of the voltage comparator is split in half. The final layout of the comparator is shown in Fig. 9. It is noted that each input transistor is placed with half on the upper left (or upper right) corner and the other half on the lower right (or lower left) corner in the layout.

IV. EXPERIMENTAL RESULTS

Our design was successfully fabricated with the AMIS C5 0.5 µm CMOS process through MOSIS. Fig. 10 shows the die photo of the fabricated smart rectifier. The total chip size is 1.29×0.72 mm². In addition to the external drain and source pads, several internal probe pads are designed onto the chip to allow us to test each individual function block. Testing results are summarized in the following.
Fig. 11 demonstrates the measured transfer characteristics of the voltage comparator. A dc power supply was used as input signal, which sweeps from negative to positive. The offset voltage is found to be around -13 mV.

Fig. 12 shows the measured waveforms of the UVLO function (under voltage lock-out) as part of the POR block during power up and down operation. Both the power supply ramp voltage and the reset signal of POR are shown in Fig. 12. It is shown that the reset signal becomes active when the power supply voltage decreases below 2 V, and inactive when the power supply increases above 2V.

Fig. 13 shows the measured characteristics of the current source on two different chips. The design target is 5µA output at 5V power supply voltage. The testing results are very close to it.

A buck converter shown in Fig. 14 is designed onto the IC chip to verify the operation of the self-synchronized rectifier design. All the devices inside the dashed line box are integrated into one single chip. A pulse function generator is used to provide the input control signal for the upper p-channel CtrlFET. With Vin = 5 Volts and input control signal with the duty circle of 0.5, the measured waveforms are provided in Fig. 15. With the adjustable load current, the system is tested in both CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode). PMOS (CtrlFET) gate signal, inductor current, VDS of the NMOS (SyncFET), and output voltage are shown in channel 1 to channel 4 respectively. No oscillation is observed in the waveform of VDS even when the load current decreases into DCM operation.
V. CONCLUSION

A monolithic self-synchronized rectifier concept for DC/DC converter applications is presented in this paper. The analysis, simulation, design considerations, and fabrication of the proposed device are described in detail. Experimental results show that the proposed rectifier functions as designed. Since no dead-time control needs to be used to switch the SyncFET and CtrlFET, it is expected that the body diode losses can be reduced substantially comparing with the conventional synchronous rectifier. The proposed smart rectifier can be operated at high frequency and maintains high efficiency over a wide load range.

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Fig. 15 Measured switching waveforms of the buck converter testing circuit operating in (a) CCM and (b) DCM mode.