An Improved Current-fed ZVS Isolated Boost Converter for Fuel Cell Applications

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Abstract—This paper proposes a novel current-fed ZVS isolated boost converter suitable for fuel cell applications. Preserving the advantages of the current-fed converter which include smaller input current ripple, lower diode voltage rating and lower transformer turns ratio, the proposed converter does not require any clamping and start-up circuits unlike the conventional current-fed converters. The voltage ratings of the primary switches and secondary diodes of the proposed converter are significantly reduced. The proposed converter can achieve ZVS at a lighter load condition with less leakage inductance. These characteristics of the proposed converter lead to a high overall efficiency over wider load range. Experimental results on a 1kW prototype are provided to validate the proposed concept.

I. INTRODUCTION

In general fuel cells generate a DC voltage, and then the DC voltage is converted to an AC voltage. Since the DC voltage from the fuel cell is usually low and unregulated it should be boosted and regulated by a front end DC-DC converter. High frequency transformers are also involved in the front end DC-DC converter for galvanic isolation and safety purpose. In summary, the front end converter required for fuel cell power generation is an isolated boost DC-DC converter.

The isolated boost DC-DC converter for fuel cell applications could be either voltage-fed or current-fed type. The advantages and disadvantages of the two types are detailed in [1-2]. Compared to the voltage-fed topology, the current-fed topology exhibits smaller input current ripple, lower diode voltage rating, lower transformer turns ratio and negligible ringing phenomenon at the secondary side, in general [3]. Especially, lower transformer turns ratio leads to smaller duty cycle loss and transformer copper losses, which are important for efficient operation with high frequency at high power level. Direct and precise control of the fuel cell current is also possible with the current-fed topology. Therefore, it can be pointed out that the current-fed topology is better suited to fuel cell applications[1].

There are three basic topologies of isolated current-fed dc-dc converters, namely full-bridge, push-pull, and L-type half bridge. Among them, the L-type half bridge converter, shown in Fig. 1, has several advantages over the other topologies: 1) switch conduction losses are lowest as in the push-pull converter, 2) transformer utilization is the best as in the full-bridge converter, 3) input current ripple is lowest due to the interleaved operation, 4) since the transformer turns ratio of the L-type half-bridge converter is halved the voltage rating and the current rating of the primary winding of the transformer are doubled and halved, respectively. Therefore, the L-type half bridge is more suitable to low voltage, high current applications such as front-end dc-dc converters for fuel cell applications [4].

However, the L-type half bridge, one of the current-fed topology, has larger switch voltage rating compared to the voltage-fed topology. The L-type half-bridge converter also suffers from high voltage spikes across the switch caused by leakage inductance of the transformer. Several passive and active clamping methods (see Fig. 1) have been proposed to reduce the voltage spike, but they require additional components and losses. Also, an additional start-up circuit is required for the L-type half bridge converter to prevent the inrush current during the start-up because of restriction of the duty ratio in the conventional current-fed converter based on full-bridge, push-pull, or half bridge topologies.

In this paper a novel current-fed ZVS isolated boost converter is proposed for fuel cell applications. Preserving the advantages of the current-fed converter which include smaller input current ripple, lower diode voltage rating, and lower transformer turns ratio, the proposed converter does not require clamping and start-up circuits unlike the conventional current-fed converter. The voltage ratings of the primary switches and secondary diodes of the proposed converter are reduced to half of those of the L-type half-bridge converter. The proposed converter features ZVS turn-on of the primary switches over wider load range with less leakage inductance of the transformer.

![Fig. 1 Conventional L-type half bridge converter](image-url)
The operating principle of the proposed converter will be discussed in detail. The proposed converter will be compared to the L-type half bridge converter and experimental results on a 1kW prototype will also be provided to validate the proposed concept.

II. OPERATING PRINCIPLES

As shown in Fig. 2, the proposed isolated boost converter consists of two input filter inductors, four MOSFET switches, two auxiliary capacitors at the low voltage side and two series connected voltage doubler rectifiers at the high voltage side. Two high frequency transformers and two voltage doubler rectifiers which are employed for step-up and isolation are connected in series so that the diode voltage rating becomes half of the output voltage. Due to this connection the voltage transfer ratio of the proposed converter can be obtained by,

\[ \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2 \cdot n}{1 - D} \quad (0 < D < 1) \quad (1) \]

The voltage transfer ratio of the proposed converter is twice that of the conventional L-type half bridge converter meaning that the required turn ratio for step-up can be reduced to half. This reduces the number of turns of the transformer winding resulting in reduced copper losses and leakage inductance of the transformer. The two legs at the low voltage side are interleaved with 180° phase shift resulting in reduced input current ripples, and the upper and lower switches of each leg are operated with asymmetrical complementary switching to regulate the output voltage. Figure 3 shows key waveforms of the proposed converter for illustration of the operating principle. The converter has six operating states within each operating half cycle.

Figure 4 shows equivalent circuits of the 6 operating states. It is assumed that the input filter inductance is large enough so that it can be treated as a constant current source during a switching period. It is also assumed that the auxiliary and output capacitances are large enough so that they can be treated as a constant voltage source during a switching period. The average voltages of the auxiliary and output capacitors can be obtained by,

\[ V_{c1} = \frac{D}{1 - D} \cdot V_{\text{in}}, \quad V_{c2} = V_{\text{in}} \quad (2) \]

\[ V_{c3} = V_{c5} = \frac{V_{\text{out}}}{2} \cdot D, \quad V_{c4} = V_{c6} = \frac{V_{\text{out}}}{2} \cdot (1 - D) \quad (3) \]

State 1 \([t_1-t_2]\)

Switches S1 and S3 are conducting and each switch carries both input inductor current and the leakage inductor current. The voltage across the leakage inductor of the transformer is a difference between an auxiliary capacitor voltage \(V_{c1}\) or \(V_{c2}\) and an output capacitor voltage \(V_{c3}, V_{c4}, V_{c5}\) or \(V_{c6}\) referred to the primary. During this state the voltages across the leakage inductors can be obtained by,

\[ V_{lk1} = V_{lk2} = -V_{\text{in}} + \frac{V_{\text{out}} \cdot (1 - D)}{2 \cdot n} \quad (4) \]

Since voltages across the leakage inductors, \(V_{Ilk1}\) and \(V_{Ilk2}\), are small negative values the leakage inductor currents are slowly increasing in the direction shown in the equivalent circuit.
State 2 \([t_2-t_3]\)
Switch \(S_1\) is turned off at \(t_2\), and then parasitic capacitors of switches \(S_3\) and \(S_4\) are charged to \(V_{\text{in}}/(1-D)\) V and discharged to 0V, respectively, by current \(I_{k2}+I_{k3}\). After completion of discharge operation the body diode of \(S_4\) is turned on, and the current flowing through the body diode of \(S_4\) rapidly decreases since voltage \(V_{\text{lk2}}\) becomes large positive as follows,

\[
V_{\text{lk2}} = \frac{D}{1-D} \cdot V_{\text{in}} + \frac{V_{\text{out}} \cdot (1-D)}{2 \cdot n} \tag{5}
\]

The main channel of \(S_4\) starts conducting at the time the gate signal is applied to \(S_4\). This state ends when current \(I_{k2}\) reaches 0V.

State 3 \([t_3-t_4]\)
Since current \(I_{k2}\) reverses its direction, diode \(D_3\) is turned on, and then current \(I_{k2}\) starts slowly increasing due to the small positive value applied across the leakage inductance \(L_{k2}\) as follows,

\[
V_{\text{lk2}} = \frac{D}{1-D} \cdot V_{\text{in}} - \frac{V_{\text{out}} \cdot D}{2 \cdot n} \tag{6}
\]

This state ends when current \(I_{k2}\) becomes equal to \(I_{k3}\), that is, switch current \(I_{k4}\) reaches 0.

State 4 \([t_4-t_5]\)
At \(t_4\) current \(I_{k4}\) reverses its direction, and then \(S_4\) is turned on with ZVS. Current \(I_{k2}\) is continuously increasing with the slope determined at state 3.

State 5 \([t_5-t_6]\)
Switch \(S_4\) is turned off at \(t_5\), and then parasitic capacitors of switches \(S_1\) and \(S_4\) are discharged to 0V and charged to \(V_{\text{in}}/(1-D)\) V, respectively, by current \(I_{k2} - I_{k3}\). After completion of discharge operation the body diode of \(S_3\) is turned on, and the current flowing through the body diode of \(S_3\) rapidly decreases since voltage \(V_{\text{lk2}}\) becomes large negative as follows,

\[
V_{\text{lk2}} = -V_{\text{in}} - \frac{V_{\text{out}} \cdot D}{2 \cdot n} \tag{7}
\]

The main channel of \(S_3\) starts conducting at the time the gate signal is applied to \(S_3\). This state ends when current \(I_{k2}\) becomes equal to \(I_{k3}\), that is, switch current \(I_{k4}\) reaches 0.

State 6 \([t_6-t_7]\)
At \(t_6\) current \(I_{k4}\) reverses its direction, and \(S_3\) is turned on with ZVS. Current \(I_{k2}\) is continuously increasing with the slope determined at state 5. This state ends when current \(I_{k2}\) reaches 0V. This is the end of a half cycle. The other half cycle begins at time \(t_7\) and is repeated except with the correspondingly opposite set of legs.
As explained in State 2 the parasitic capacitor of upper switch \( S_4 \) is discharged by current magnitude \( I_3 = I_{L2} + I_{lk2} \) at time \( t_3 \), as shown in Fig. 5. To ensure the ZVS turn on of switch \( S_3 \) the following condition should be satisfied,

\[
\frac{1}{2} \cdot L_{k2} \cdot I_{L2(max)}^2 + \frac{1}{2} \cdot L_{k2} \cdot I_{lk2(max)}^2 > C_{oss} \cdot \left( \frac{V_{in}}{1-D} \right)^2 \tag{8}
\]

Where

\[
I_{L2(max)} = \frac{1}{2} \left( \frac{P_v}{V_{in}} + \frac{V_{out}}{L_1 \cdot f_s} \right) \tag{9}
\]

\[
I_{lk2(max)} = \frac{D \cdot (V_{in} - V_{out} \cdot (1-D))}{2 \cdot n \cdot L_{k2} \cdot f_s} \tag{10}
\]

Since equation (8) is easily satisfied, in general, ZVS can be achieved over the whole load range for upper switches \( S_2 \) and \( S_4 \).

As explained in State 5 the parasitic capacitor of lower switch \( S_3 \) is discharged by current magnitude \( I_4 = I_{lk3} - I_{L2} \) at time \( t_4 \). To ensure the ZVS turn on of switch \( S_3 \) the following condition should be satisfied,

\[
\frac{1}{2} \cdot L_{k2} \cdot I_{lk2(max)}^2 - \frac{1}{2} \cdot L_{k2} \cdot I_{L2(min)}^2 > C_{oss} \cdot \left( \frac{V_{in}}{1-D} \right)^2 \tag{11}
\]

Where

\[
I_{lk2(max)} = \frac{D \cdot (1-D) \cdot (V_{in} - V_{out})}{2 \cdot n \cdot L_{k2} \cdot f_s} \tag{12}
\]

\[
I_{L2(min)} = \frac{1}{2} \left( \frac{P_v}{V_{in}} - \frac{V_{out}}{L_2 \cdot f_s} \right) \tag{13}
\]

Equation (11) may not be satisfied under the conditions of small transformer leakage inductance, large input filter inductance and/or heavy load. Increasing transformer leakage inductance to enlarge the ZVS region makes the duty cycle loss large resulting in increased turns ratio. Instead, the input filter inductance can be reduced, and hence current magnitude \( I_2 \) can be increased resulting in enlarged ZVS region. Decreasing the input filter inductance increases the current rating of the power devices, and therefore the input filter inductance should be properly chosen considering a trade-off between the ZVS region and the device current ratings. To further enlarge the ZVS region, DCM operation on the input filter inductor may be employed as shown in Fig. 5 meaning that negative current flows on the input filter inductor. However, this may not be a problem in this scheme owing to the interleaved operation of the two input filter inductor currents. It should be noted that ZVS region can be optimized by properly designing the input filter inductance.

Since the ZVS turn on with complementary switching does not interrupt the current flowing through the leakage inductor the proposed converter does not need additional clamping and/or snubber circuits at the primary and secondary.

\[
D_{eff} = 1 + D_{deadtime} - \left( \frac{2 \cdot n \cdot V_{in}}{V_{out} + 2 \cdot n \cdot L_k \cdot \frac{d}{dt} I_{lk}} \right) \tag{14}
\]

The transformer turns ratio is obtained based on the effective duty cycle, and then the component ratings are calculated. The component ratings of the two converters according to the design specification are compared in Table I.
TABLE I
COMPONENT RATING CALCULATION

<table>
<thead>
<tr>
<th>Components</th>
<th>Design items</th>
<th>Conventional Converter (Fig. 1)</th>
<th>Proposed Converter (Fig. 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{pk}$</td>
<td>140 V</td>
<td>70 V</td>
</tr>
<tr>
<td></td>
<td>$I_{pk}$</td>
<td>Main 60 A</td>
<td>60 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clamp 35 A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$P_e / (V_{pk} \cdot I_{pk} \cdot q)$</td>
<td>0.037</td>
<td>0.06</td>
</tr>
<tr>
<td>Diode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{pk}$</td>
<td>400 V</td>
<td>215 V</td>
</tr>
<tr>
<td></td>
<td>$I_{pk}$</td>
<td>11 A</td>
<td>15 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P_e / (V_{pk} \cdot I_{pk} \cdot q)$</td>
<td>0.056</td>
</tr>
<tr>
<td>Transformer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Turns ratio</td>
<td>1 : 3.5</td>
<td>1 : 3.5 : 3.5</td>
</tr>
<tr>
<td></td>
<td>Primary</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{rms}$</td>
<td>76 V</td>
<td>27 V</td>
</tr>
<tr>
<td></td>
<td>$I_{rms}$</td>
<td>15 A</td>
<td>22 A</td>
</tr>
<tr>
<td></td>
<td>Secondary</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{rms}$</td>
<td>265 V</td>
<td>95 V</td>
</tr>
<tr>
<td></td>
<td>$I_{rms}$</td>
<td>4.3 A</td>
<td>6 A</td>
</tr>
<tr>
<td></td>
<td>$kVA$</td>
<td>1140 VA</td>
<td>580 VA x 2</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>Capacitance</td>
<td>5.5 uF</td>
<td>7 uF x 4</td>
</tr>
<tr>
<td></td>
<td>$V_{pk}$</td>
<td>400 V</td>
<td>160 V</td>
</tr>
<tr>
<td></td>
<td>$CV^2(\text{PU})$</td>
<td>1</td>
<td>0.81</td>
</tr>
<tr>
<td>Input Inductor</td>
<td>Inductance</td>
<td>17 uH x 2</td>
<td>13 uH x 2</td>
</tr>
<tr>
<td></td>
<td>$I_{rms}$</td>
<td>25 A</td>
<td>25 A</td>
</tr>
<tr>
<td></td>
<td>$LI^2(\text{PU})$</td>
<td>1</td>
<td>0.76</td>
</tr>
<tr>
<td>Auxiliary Capacitor</td>
<td>Capacitance</td>
<td>7 uF</td>
<td>14 uF x 2</td>
</tr>
<tr>
<td></td>
<td>$V_{pk}$</td>
<td>140 V</td>
<td>50 V</td>
</tr>
<tr>
<td></td>
<td>$CV^2(\text{PU})$</td>
<td>1</td>
<td>0.51</td>
</tr>
</tbody>
</table>

The switch voltage rating of the proposed converter is half of that of the L-type half bridge converter so that the MOSFETs with lower $R_{d(on)}$ can be chosen for the proposed converter resulting in significantly reduced conduction losses. The diode voltage rating of the proposed converter is also half of that of the L-type half bridge converter due to the series connection of the two voltage doubler rectifiers. Due to reduced diode voltage rating shottky diodes with low reverse recovery time and forward voltage drop can be used, and the losses associated with rectifier diodes can also be reduced. The proposed converter employs two high frequency transformers connected in series. The total kVA rating of the proposed converter is almost the same as that of the L-type half bridge converter, which can slightly increase the total transformer volume, but this can allow a low profile. It is also noted that the proposed converter could have smaller size and weight of the passive components such as input inductors, output capacitors and auxiliary capacitors. The proposed converter employs four output capacitors, but total energy volume of the capacitors are smaller for the proposed converter due to halved capacitor peak voltage.

An efficiency calculation according to the component ratings listed in Table I has been performed in the following manner:
1) All components are designed based on the given specification, 2) Actual devices from manufactures are selected with appropriate safety margin based on the designed value, 3) The power losses are calculated considering conduction and switching losses of switches and diodes, core losses and copper losses of transformers, and ESR losses of capacitors, etc al.

It can be seen from the calculated efficiency curves in Fig. 6 that the efficiency of the proposed converter is higher than that of the conventional L-type converter over the whole load range. This is mainly because MOSFET’s with lower voltage rating, that is, lower $R_{d(on)}$ and Schottky diodes with lower $t_r$ could be used for the proposed converter. The efficiency of the proposed converter at light loads is especially high due to the enlarged ZVS region as discussed in section II.

In general, a soft starting technique without any additional circuit can be applied to the voltage-fed converter in order to prevent the inrush current during start-up. This is because the duty cycle of the voltage-fed converter can be gradually increased from 0. However, some additional start-up circuitry is required for the current-fed isolated converter based on the conventional push-pull, half-bridge, or full-bridge topologies to apply the soft-starting. This is because of the restricted duty cycle, which is larger than 0.5. The duty cycle of the proposed converter ranges from 0 to 1, and therefore no start-up circuitry is required for the proposed converter.

The quasi-square-wave ZVS turn-off technique can be applied to the proposed converter, whereas it can not be applied to the L-type half bridge converter.

IV. EXPERIMENTAL RESULTS

A 1 kW laboratory prototype of the proposed converter has been built and tested to verify the operating principle. The system parameters used in the experiment are the same as those in Section III. The transformer is built using 44020-EC core with the number of turns of $N_p : N_s = 4 : 14$. The transformer leakage inductance is 0.5 uH. A primary switch is implemented with three International Rectifier IRFB4321Pbf(150V, 80A, 12m ohm) MOSFET’s in parallel.

Schottky diodes of IXYS DGS20-025A (250V, 18A) are used for secondary rectifier. Fig. 7 shows experimental waveforms obtained at 700W load ($V_{in} = 32V$, $V_{out} = 400V$).
The waveforms of interleaved inductor currents and input current are shown in Fig. 7(a) and Fig. 7(b), respectively. It can be seen from Fig. 7(c) and (d) that both lower switch S\textsubscript{1} and upper switch S\textsubscript{2} are being turned on with ZVS. The measured overall efficiency of the proposed converter is shown in Fig. 6. A good agreement between calculated and measured overall efficiency was obtained for the entire load level. The maximum overall efficiency of 95.6% was measured at 600W load.

V. CONCLUSIONS

In this paper a new current-fed isolated boost converter has been proposed for low voltage and high current application such as fuel cells. Preserving the advantages of the conventional current-fed converter which include smaller input current ripple, lower diode voltage rating and lower transformer turns ratio, the proposed converter has the following advantages over the conventional current-fed converter:

* Significantly reduced voltage ratings (halved compared to L-type half-bridge) of the main switches and diodes which allows use of devices with lower $R_{d\text{son}}$ and $t_{tr}$, respectively.
* Reduced size and weight of the passive components such as input filter inductors, auxiliary capacitors, and output capacitors.
* Enlarged ZVS region at light load with smaller leakage inductance.
* No clamping or snubber circuits required due to the ZVS operation without interruption of leakage inductor current.
* No start-up circuitry required for implementation of the soft-starting because of duty cycle range between 0 and 1.

These characteristics of the proposed converter lead to higher overall efficiency over wide load range and reduced size and weight. Experimental results on a 1kW prototype have been provided to validate the proposed concept.
REFERENCES


