An Improved Active-clamp ZVS Forward Converter Circuit

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Abstract—In order to achieve Zero Voltage Switching (ZVS) easier for both primary switch and auxiliary switch in the active clamp forward converter, an improved active-clamp ZVS forward converter topology is proposed in this paper. Compared with the conventional active-clamp forward converter, the improved one with an auxiliary network which is consisted of a clamp capacitor and an inductor could easily achieve ZVS in full-load range. Therefore the circuit efficiency is increased by reducing the switching loss of the switches. The operation principles of the proposed converter circuit are analyzed in detail and the performance is compared with the conventional one. The design procedure and the experimental results are presented for a converter with a 230 V input; 14.4 V/10 A output. The experimental results match the theoretical analysis very well.

Keywords—ZVS, active-clamp, forward.

Ⅰ. INTRODUCTION

Structure of forward converters has been used in more and more applications (about 50 W – 500 W) because of its simpleness, high-efficiency and good-performance. But the duty circle could not exceed 50% and the high voltage stress of the switch suffered from the leakage inductance reaches more than two times of the input voltage if the reset turns equal to the primary turns. Then, the structure of active clamp forward converter was proposed to solve the problems above. The magnetic core is fully used because it works in both first and third quadrant while the reset winds are necessary in conventional forward converter since the magnetic core almost just works in the first quadrant. The voltage stress is clamped by the auxiliary clamp capacitor as well as the duty circle problem is solved in this topology. On the other hand, the hard switching techniques in the forward converters results in low efficiency. Theoretically, with one auxiliary switch in the active-clamp forward converter to recycle the energy stored in the transformer leakage, the primary switch could turn off under zero voltage if the driver is fast enough. However, the primary switch, in fact, is hard to achieve zero voltage turn-on in this circuit. The result turns out that the switching losses can not be reduced greatly and which leads to the total efficiency is not improved greatly also.

In this paper an active clamp ZVS forward converter with an auxiliary network is presented. With this new technique proposed, ZVS of the primary switch can be easily achieved in full-load range; hence the switching loss of the converter is reduced. A detail of the design procedure and the converter operation principles are analyzed in this paper. Finally, the experimental results based on the input voltage of 230 V and the output voltage of 14.4 V prototype working at rated output load of 10 A and a switching frequency of 100 kHz are provided to support this new topology theory.

Ⅱ. OPERATION PRINCIPLE

The proposed active-clamp ZVS forward circuit is given in the Fig.1. The basic forward converter in the primary side is consisted of the transformer, primary switch Q1. The auxiliary switch Q1 and clamp capacitor Cc are used to absorb the surge energy from the leakage inductance so as to reduce the voltage stress of the main switch Q1. Theoretically, the main switch could achieve ZVS by the resonant circuit include the junction capacitance Coss, the leakage inductance Lr and the magnetizing inductance Ln. However, it is difficult to meet the demand since the magnetizing current is not large enough. So, the ZVS active clamp forward converter with an auxiliary network consisted of a clamp capacitance Ca and inductance La is proposed in Fig.1 below.

Fig.1 The proposed active clamp ZVS forward converter circuit

Before analyzing the circuit, there are several assumptions must be made.

1. The leakage inductance Lr is much smaller than the magnetizing inductance Ln.
2. Clamp capacitor Cc is much lager than the junction capacitance Coss.
3. The clamp capacitor Cc and Ca are large enough so that the voltage on them are constant.
4. The output inductance filter is large enough that the output voltage and current are constant.

The key waveforms of the converter are shown in Fig.2. The detailed operation principles are described as below:
The clamp capacitor voltage is obtained easily because the voltage-second products balance principle. The voltage is given as:

\[ V_c = V_a = \frac{D V_{in}}{1 - D} \]  

\[ \text{(1)} \]

**State 1** \([t_0 < t < t_1]\): At \( t_0 \), primary switch \( Q_1 \) is turned on. The secondary side diodes are both conducting so that the input voltage is added on the leakage inductor \( L_r \) and the current \( i_{L_r} \) is linearly increasing. The current is given as:

\[ i_{L_r}(t) = I_{L_r}(t_0) + \frac{V_m}{L_r}(t - t_0) \]  

\[ \text{(2)} \]

**State 2** \([t_1 < t < t_2]\): At \( t_1 \), the secondary diode current \( i_{D_2} = 0 \) and \( D_2 \) is off. Magnetizing current \( i_m \) is linearly increasing while current \( i_a \) flows through \( L_a \) and \( C_{oa} \) is linearly decreasing. The current \( i_a \) will change from a positive value to a negative one during the interval. And the current flows through the primary switch \( Q_1 \) is consisted of \( i_a, i_m \) and the primary part of the output current \( I_o \).

\[ i_m(t) = I_m(t_0) + \frac{V_m}{L_m}(t - t_0) \]  

\[ i_a(t) = I_a(t_0) - \frac{V_m + V_a}{L_a}(t - t_0) \]  

\[ \text{(3)} \]

**State 3** \([t_2 < t < t_3]\): Main switch \( Q_1 \) is turned off at time \( t_2 \). The primary current charges the resonant capacitance \( C_{oss} \) from 0 to \( V_{in} \).

**State 4** \([t_3 < t < t_4]\): This stage begins when \( v_{ds} = V_{in} \) and ends at time \( t_4 \) when \( v_{ds} = V_{in} + V_c \). The secondary side diodes are both conducting. The resonant tank is consisted of \( L_o, L_r \) and \( C_{oss} \).

\[ v_{ds}(t) = V_{in} - V_{in} \cdot \cos(\omega_1(t-t_4)) + I_m(t_4) - I_m(t_4) + \frac{I}{N} \sin(\omega_2(t-t_5)) \]  

\[ \text{(4)} \]

**State 5** \([t_4 < t < t_5]\): Since the anti-parallel diode across auxiliary switch is conducting current, \( Q_2 \) can be ZVS turned on in this interval when \( D_1 \) and \( D_2 \) are both still conducting.

**State 6** \([t_5 < t < t_6]\): At time \( t_5 \), \( i_{D_1} = 0 \) and \( Q_2 \) is turned on. The voltage \( V_s \) forces current \( i_a \) to increase linearly while the magnetizing current \( i_m \) decreases linearly.

\[ i_a(t) = I_a(t_5) + \frac{V_s}{L_a}(t - t_5) \]  

\[ i_m(t) = I_m(t_5) - \frac{V_s}{L_m}(t - t_5) \]  

\[ \text{(5)} \]

**State 7** \([t_6 < t < t_7]\): The auxiliary switch \( Q_2 \) is turned off at time \( t_6 \). The junction capacitor \( C_{oss} \) is discharged via current \( i_a \) and \( i_m \) at the same time. This state ends at time \( t_7 \) when the voltage \( v_{ds} \) decreases to \( V_{in} \).
are both turned on. The voltage \( v_{dt} = 2 \) and 2 for operation.

The resonant capacitor voltage is expressed as:

\[
\begin{align*}
C_{res} \frac{dv_{dt}}{dt} &= i_{s} - i_{a} \\
(L_e + L_m) \frac{di_{a}}{dt} &= V_{in} - v_{di} \\
L_s \frac{dv_{di}}{dt} &= v_{di} - V_{in}
\end{align*}
\]

The resonant capacitor voltage is expressed as:

\[
v_{di}(t) = V_{in} + V_c \cdot \cos \omega_i (t - t_6) + \frac{[I_m(t_6) - I_s(t_6)] \sin \omega_i (t - t_6)}{\omega_i C_{res}}
\]

Where \( \omega_i = \omega_s \) (10)

**State8** \([7 < t < 8]\): At time \( t \), the voltage \( v_{di} \) decreases to \( V_{in} \). Diodes \( D_1 \) and \( D_2 \) are both turned on. The voltage \( v_{di} \) decreases to zero and the anti-parallel diode across primary switch is turned on, then the main switch could realize ZVS operation.

\[
\begin{align*}
C_{res} \frac{dv_{di}}{dt} &= i_{s} - i_{a} \\
L_e \frac{di_{a}}{dt} &= V_{in} - v_{di} \\
L_s \frac{dv_{di}}{dt} &= v_{di} - V_{in}
\end{align*}
\]

The resonant capacitor voltage is expressed as:

\[
v_{di}(t) = V_{in} + \frac{I_s(t_6) - I_m(t_6)}{\omega_i C_{res}} \sin \omega_i (t - t_7)
\]

Where \( \omega_i = \omega_s \) (12)

To ensure ZVS operation of \( Q_s \), the condition of

\[
V_{in} < -\frac{I_s(t_6) - I_m(t_6)}{\omega_i C_{res}}
\]

must be satisfied.

### III. DESIGN PROCEDURE

1. The Key Issue to Realize The ZVS

The voltage across the junction capacitor \( v_{di} \) should resonate to zero via the current \( i_s \) and \( i_m \) during the time when the auxiliary switch \( Q_s \) is turned off until the primary switch \( Q_s \) is turned on.

One assumes that the period of switch is \( T \), and the duty cycle is \( D \). To simplify the analysis, it is assumed that:

\[
\begin{align*}
I_s(t_6) &= I_m(t_6) = \left| i_{a - max} \right| \\
I_s(t_7) &= I_e(t_7) = -\left| i_{m - max} \right|
\end{align*}
\]

The interval between \( t_6 \) and \( t_7 \) could be obtained by the equation (10), and is given as:

\[
t_7 - t_6 \approx \frac{V_c \cdot C_{res}}{\left| i_{a - max} \right| + \left| i_{m - max} \right|}
\]

The interval between \( t_6 \) and \( t_7 \) is a quarter period of the resonance could be the best condition and the primary
switch \( Q_1 \) will achieve ZVS since
\[
|I_{\text{max}}| + |I_{\text{in-max}}| \sin \omega_t (t_h - t_g) \geq V_{\text{in}}
\]
must be satisfied.

One can obtain the inductance \( L_o \) should meet the condition of
\[
L_o \leq \frac{D \cdot T \cdot L_n}{2 \cdot \frac{C_{\text{out}}}{L_r} - D \cdot T}
\]

It is assumed that the interval when the auxiliary switch \( Q_2 \) is turned off until the primary switch \( Q_1 \) is turned on is \( t_{dd} \).
On the basis of the analyses above, the \( t_{dd} \) is given as:
\[
t_{dd} = t_h - t_g = \frac{2 \cdot L_o \cdot L_n \cdot C_{\text{out}}}{D \cdot (L_o + L_n) \cdot T} + \frac{1}{2} \sqrt{L_r \cdot C_{\text{out}}}
\]

2. The Procedure

2.1 Transformer

Since the relation between input voltage and output voltage, one obtained:
\[
V_{\text{in}} \cdot D = n \cdot (V_o + V_D)
\]

According to the equation (1) and (17), the \( V_c \) could be presented as:
\[
V_c = \frac{n \cdot (V_o + V_D)}{V_{\text{in}}} = \frac{n \cdot (V_o + V_D) V_{\text{in}}}{V_{\text{in}} - n \cdot (V_o + V_D)}
\]

The turn ratio of the transformer \( n \) could be calculated from the equation (19). It is given as:
\[
n = \frac{V_{\text{in-min}} \cdot V_{\text{in-max}}}{(V_o + V_D)(V_{\text{in-min}} + V_{\text{in-max}})}
\]

2.2 Switch on the primary side

Therefore, the voltage stress of the primary switch \( Q_1 \) and the auxiliary switch \( Q_2 \) could be calculated as:
\[
V_{\text{dss-max}} = \frac{n \cdot (V_o + V_D)}{V_{\text{in-min}} - n \cdot (V_o + V_D)} + V_{\text{in-min}}
\]

The maximum current flow through the primary switch \( Q_1 \) and auxiliary switch \( Q_2 \) is given as:
\[
I_{\text{Q1-max}} = \frac{n}{n} + \frac{1}{2} \Delta I_o + |I_{\text{in-max}}|
\]
\[
I_{\text{Q2-max}} = |I_{\text{in-max}}| + |I_{\text{in-min}}|
\]

Where \( \Delta I_o \) is the ripple current of the \( I_o \).

2.3 Diodes on the secondary side

The voltage stress of the rectify diodes on the secondary side are presented as:
\[
V_{\text{D1-max}} = \frac{V_{\text{max}}}{n} ; V_{\text{D2-max}} = \frac{V_{\text{in-max}}}{n}
\]

While the current stress of \( D_1 \) and \( D_2 \) are given as:
\[
I_{\text{D1-max}} = D_{\text{max}} \cdot I_o ; I_{\text{D2-max}} = (1 - D_{\text{min}}) \cdot I_o
\]

Where the maximum and minimum duty circles are presented as:
\[
D_{\text{max}} = \frac{n \cdot (V_o + V_D)}{V_{\text{in-min}}} ; D_{\text{min}} = \frac{n \cdot (V_o + V_D)}{V_{\text{in-max}}}
\]

2.4 The output filter

The output inductor should be calculated as below:
\[
L_o \geq \frac{V_o \cdot (1 - D_{\text{max}}) \cdot T}{\Delta I_o}
\]

The output filter capacitance \( C_o \) for the aluminum electrolytic capacitors can be expressed as:
\[
C_o = 6 \cdot 10^{-6} \frac{\Delta I_o}{\Delta V_o}
\]

2.5 The auxiliary network

When the primary switch \( Q_1 \) and the transformer are designated, then \( L_o \) is obtained by the equation (15). The peak current value through the auxiliary net is given as:
\[
|I_{\text{max}}| = \frac{D \cdot T \cdot V_{\text{in}}}{2 \cdot L_o}
\]

The value of the clamp capacitance \( C_o \) will be confirmed due to the ripple voltage across the \( C_o \). It is expressed as:
\[
C_o = \frac{|I_{\text{max}}| \cdot T}{4 \cdot \Delta V_o}
\]

As the same situation as the capacitance \( C_o \), the capacitance \( C_e \) is given as:
\[
C_e = \frac{|I_{\text{max}}| + |I_{\text{in-max}}| \cdot T}{4 \cdot \Delta V_c}
\]

IV. DESIGN EXAMPLE

To verify the theoretical analysis of the circuit proposed, a 230 V input, 14.4 V/10 A output active clamp ZVS forward converter has been implemented. The parameters and key components are listed as follows:

<table>
<thead>
<tr>
<th>Table I. Parameters and key components of the converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Q_1 )</td>
</tr>
<tr>
<td>SPA11N60C3</td>
</tr>
<tr>
<td>EE19 635 ( \mu )H</td>
</tr>
</tbody>
</table>

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Fig. 4 shows the driving signals of $Q_1$ and $Q_2$. Fig. 5 shows the driving signal and drain to source voltage of $Q_1$.

![Fig. 4 driving waveforms of two switches](image)

![Fig. 5 gate to source and drain to source waveforms of main switch](image)

Fig. 6 presents the driving signal and current waveforms of $Q_1$. As can be seen from these two figures, before $Q_1$ is turned on, current $i_{Q_1}$ flows through the anti-parallel diode across $Q_1$ and $v_{ds}$ is zero.

![Fig. 6 gate to source voltage waveform and current signal of the main switch](image)

Fig. 7 shows the driving signal and drain to source voltage of $Q_2$ in the conventional active clamp forward converter without the auxiliary network. As it shows, the main switch can not achieve ZVS. Fig. 8 & Fig. 9 present the efficiency curves of the active clamp ZVS forward converter compared with the conventional one and it is clear that the efficiency of the proposed circuit in this paper is improved greatly. The experimental results match the theoretical analysis very well.

![Fig. 7 gate to source and drain to source voltage waveforms of main switch in the conventional active-clamp forward converter](image)

![Fig. 8 efficiency curve @ Vo=12 V](image)

![Fig. 9 efficiency curve @ Io=10 A](image)

V. CONCLUSION

An improved active clamp ZVS forward converter is proposed in the paper. With the auxiliary network, the switches of the converter could realize ZVS. A 230 V input, 14.4 V/10 A output active clamp ZVS forward converter is built up and the experimental results match the theoretical analysis very well.

VI. REFERENCES

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