Elimination of Dead-time in PWM Controlled Inverters

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Abstract- A dead-time elimination method is presented in this paper for PWM controlled inverters. In comparison to using expensive current sensors, this method precisely determines the load current direction by detecting the operating conditions of active devices and their anti-parallel diodes. A low-cost diode-conducting detection circuit is developed to measure the operating status of the anti-parallel diode. In comparison with complicated compensators, this method features with simple logic and flexible implementation. This method significantly reduces the output distortion and regains the RMS value. The principle of proposed dead-time elimination method is described. Simulation and experimental results are given to demonstrate the validity and features of the dead-time elimination method.

I. INTRODUCTION

To avoid shoot-through in PWM controlled voltage source inverters (VSI), dead-time, a small interval during which both the upper and lower switches in a phase leg are off, is introduced into the control of the standard VSI phase leg. However, such a blanking time can cause problems such as output waveform distortion and fundamental voltage loss in VSIs.

Fig. 1 shows the dead-time effect in a voltage source inverter. The output voltage error $\Delta V$, shown in figure 1 (a), caused by dead-time is depicted as:

$$\Delta V = \frac{2t_\Delta}{T_s} V_k \times \text{sgn}(i_c)$$  (1)

where $t_\Delta$ is the dead-time interval, and $T_s$ is the carrier switching period. As a result, the effect of the dead-time on the output voltage becomes severe when the modulation index is small. Fig 1 (b) shows the output voltage waveform distortion caused by dead-time effect.

![Fig. 1. Dead-time effect.](image)

To overcome dead-time effects, most solutions focus on dead-time compensation [1-4] by introducing complicated PWM controller and expensive current detection hardware. In practice, the dead-time varies with the devices and output current, as well as temperature, which makes the compensation less effective, especially at low output current, low frequency, and zero current crossing. [5] proposed a new switching strategy for PWM power converters. [6] presented an IGBT gate driver circuit to eliminate the dead-time effect. [7] proposed a phase leg configuration topology which prevented shoot through. However, an additional diode in series in the phase leg increases complexity and causes more loss in the inverter. Also, this phase leg configuration is not suitable for high power inverters because the upper device gate turn off voltage is reversely clamped by a diode turn on voltage. Such a low voltage, usually less than 2 V, is not enough to ensure that a device is in off state during the activation of its complement device.

In this work, an effective dead-time elimination method is proposed, which can be easily implemented in the inverter PWM controller or gate driver. The principle will be discussed first and then simulation and experimental results are provided to demonstrate the validity and features of the proposed novel method.

II. PRINCIPLE OF DEAD-TIME ELIMINATION

To explain the principle of the proposed dead-time elimination method, we refer to a generic phase leg of VSIs, as shown in figure 2.

![Fig. 2. A generic phase leg of VSIs.](image)

Assuming the output current flows out of the phase leg, in each switching cycle, the current comes out from the upper device when $K_p$ is on and freewheels through diode $D_n$ when $K_p$ is off. Here this current direction is defined as positive. Under this condition, the generic phase leg can be equivalently expressed as a P type switching cell shown in the left figure of Fig. 3. Similarly when load current flows into the phase leg, defined as negative, the current goes into the lower device when $K_n$ is on and freewheels through diode $D_p$ when $K_n$ is off. Under this condition, the generic phase leg can be equivalently expressed as a N type switching cell shown in the right figure.
of Fig. 3. Actually a generic phase leg is a combination of one P switch cell and one N switch cell. There is no question that dead-time is not required for either a P switch cell or a N switch cell because both cells are configured with a controllable switch in series with a uncontrollable diode.

![P Switch Cell N Switch Cell](image)

Fig. 3. Equivalent switch cells.

The control scheme for a generic phase leg can be illustrated in figure 4. Only one gate control signal is needed for each phase leg. When the output current is positive, the gate control signal is selected to gate-on and gate-off upper device, Kp, only. When the output current is negative, the gate control signal will be inverted and used for manipulating lower device, Kn. The control scheme can be mathematically described as logic functions as follows:

\[ S_P = S \cdot \text{sgn}(i_L) \]  \hspace{1cm} (2)

\[ S_N = \overline{S} \cdot \overline{\text{sgn}}(i_L) \]  \hspace{1cm} (3)

As analyzed above, the determination of load current direction is key for dead-time elimination. Contrary to using an expensive current sensor, the load current direction can be precisely determined by the operating status of switches and their anti-parallel diodes. For example, in a generic phase leg, if switch Kp is on or diode Dn is on, the load current flows out from phase leg. Analogously the load current flows into phase leg if either switch Kn or diode Dp is on. In implementation, the operating status of a switch can be easily determined by measuring its gate signal level if its activation delay is negligible. A diode-conducting detection (DCD) circuit shown in figure 5 is used to determine the anti-parallel diode operating status. As shown in Fig. 5, when the anti-parallel diode, Dp, is on, in which \( V_{ce} \) is negative, the comparator \( U_I \) output is low. As a result, a current flows through the LED \( D_0 \) and causes it to light up. This signal will be level shifted or transferred through optic-electrical interface circuit. On the other hand, when the anti-parallel diode is off, the LED \( D_0 \) will be turned off.

![Fig. 5. Diode-conducting detection circuit.](image)

To validate the proposed dead-time elimination method, an H-bridge inverter shown in Fig. 6 has been simulated using Saber software. The load is composed of an 8 mH inductor and a 2.4 ohm resistor. \( V_{dc} \) is set to 250 V and the inverter is controlled by unipolar sinusoidal PWM with switching frequency 10 kHz. The fundamental frequency of the output voltage is set to 60 Hz.

![Fig. 6. H-bridge voltage source inverter.](image)

Table 1 gives a comparison of output current RMS value and THD for case 1: with 2 usec dead-time, and case 2: with the proposed dead-time elimination method. The results show that, in case 2, the output current RMS value increases to 6.99 A. However, after the dead-time elimination, the output current RMS value increases to 6.99 A.

Fig. 7 shows the output current waveforms when the modulation index is 0.2. The dark brown curve is the output current with a dead-time of 2 usec, and the blue curve is the output current with the proposed dead-time elimination method. The dark brown curve shows a notable distortion, however, the blue curve is pure sinusoidal. It shows that the dead-time effect has been minimized when the proposed method is used. The RMS value of output current is only 8.82 A when there is a 2 usec dead-time. However, after the dead-time elimination, the output current RMS value increases to 6.99 A.
**Fig. 7. Simulated output current waveforms with MI=0.2**

**Table 1. Comparison of output current for case 1: 2 usec dead-time, and case 2: with proposed method.**

<table>
<thead>
<tr>
<th>Modulation Index</th>
<th>( I_o ) (RMS) (A)</th>
<th>( I_o ) (%THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2 usec dead time</td>
<td>Dead time eliminated</td>
</tr>
<tr>
<td>0.1</td>
<td>2.0</td>
<td>4.24</td>
</tr>
<tr>
<td>0.2</td>
<td>6.94</td>
<td>8.83</td>
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<tr>
<td>0.4</td>
<td>16.33</td>
<td>18</td>
</tr>
<tr>
<td>0.8</td>
<td>34.8</td>
<td>36.3</td>
</tr>
<tr>
<td>1.0</td>
<td>43.95</td>
<td>45.5</td>
</tr>
</tbody>
</table>

**IV. IMPLEMENTATION METHODS AND TEST RESULTS**

To validate the proposed dead-time elimination method, an H-bridge inverter, shown in figure 6, and its gate drivers have been built and tested. Two Powerex IGBT modules (CM300DY-12H) have been chosen to configure this H-bridge inverter, and the load is composed of an 8 mH inductor and a 2.4 ohms resistor, which are exactly the values used for simulation in section 2.

![Test circuit block diagram](image)

**Fig. 8. Test circuit configuration.**

Four DCD circuits are employed to detect the anti-parallel diodes, \( D_{ap} \), \( D_{bp} \), \( D_{an} \), and \( D_{bn} \), operating condition, and their output signals, \( C_{ap} \), \( C_{an} \), \( C_{bp} \), and \( C_{bn} \), are fed back to a complex programmable logic device (CPLD). The digital signal processor (DSP), TMS320LF2407A, only sends two PWM signals, \( S_{an} \) and \( S_{bn} \), to the CPLD; The control logic is implemented within the CPLD with hardware description language (HDL). The level shift for DCD circuit outputs and gate signals are achieved by an electrical-optic-electrical method implemented with optical fibers.

The test conditions are the same as those used for simulation. Fig. 9 through Fig. 11 show the test results with the modulation index of 0.2. In all three figures, ch4 is the output current waveform with 5A/div. Logic signal \( A_0 \) though \( A_3 \) are \( C_{ap} \), \( C_{an} \), \( C_{bp} \), \( C_{bn} \), \( S_{ap} \), \( S_{an} \), \( S_{bp} \), and \( S_{bn} \), respectively. It should be noted here that all logic levels are negative, in which logic low means the anti-parallel diode is conducting or the switch is gated on. Figure 9 is the test results with the proposed dead-time elimination method. It clearly shows that the output current is very close to a sinusoidal waveform. The anti-parallel diode operating conditions are effectively detected as shown in \( A_0 \) through \( A_3 \). When \( i_o \) is positive, switches \( K_{an} \) and \( K_{bp} \) are always off. Switches \( K_{ap} \) and \( K_{bn} \) are always off if \( i_o \) is negative. As a comparison, standard PWM control with 2 usec dead-time is also tested and the results are shown in figure 10. It is obvious that the output current has a reduced RMS value and notable distortion.

![Experimental waveform using the proposed method](image)

**Fig. 9. Experimental waveform using the proposed method.**

Figure 11 shows the waveforms at a small time scale when the output current crosses zero. When \( i_o \) is negative, diodes, \( D_{ap} \) and \( D_{bn} \), conduct current in each switching cycle. Logic signals, \( A_0 \) and \( A_1 \), are the measurement results of the operating status of diodes \( D_{ap} \) and \( D_{bn} \). Logic signals, \( A_3 \) and \( A_0 \), are gate signals to control switches \( K_{an} \) and \( K_{bp} \), respectively. The switches \( K_{ap} \) and \( K_{bn} \) are always forced off. Analogous situation applied to the condition when output current is negative. Fig. 11 shows that during the process of load current direction change, the gate control signals, \( S_{ap} \), \( S_{an} \), \( S_{bp} \), and \( S_{bn} \), divert smoothly.

In practice, the DCD circuit has a measurement dead zone. When the load current is extremely small, the operating condition of both anti-parallel diodes in a phase leg can not be
effectively detected. During which, a very limited delay (0.8 usec) is applied to the gate signals. This delay has a negligible effect on the output waveforms, and that is confirmed as shown in the output current waveform in figure 9.

Fig. 10. Experimental waveform with dead-time effect.

In the test prototype circuit, all control logics were implemented within a CPLD. The proposed dead-time elimination method can also be implemented in the gate driver circuit of the switches. Fig. 12 shows a block diagram of proposed method implemented in the gate drivers of a generic phase leg. The anti-parallel diode operating condition will be detected and fed to both upper and lower gate drivers. The control scheme will be implemented within gate driver logic circuit. In addition, the dead-time elimination method can be implemented within a PWM controller, contained in the DSP software.

Fig. 11. Experimental waveforms when the load current cross zero.

V. CONCLUSION

In this paper, a method was proposed to eliminate dead-time in the PWM controlled inverters. Compared to the conventional PWM control with dead-time, this method significantly reduces the output distortion and regains the RMS value. Compared to using expensive current sensors and complicated compensators, the low-cost DCD circuit, simple logic and flexible implementation make it an attractive option for VSI applications.

REFERENCES