An Integrated Reconfigurable Switched-Capacitor DC-DC Converter with a Dual-Loop Adaptive Gain-Pulse Control

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Abstract – This paper presents a new integrated reconfigurable switched-capacitor dc-dc converter with a dual-loop adaptive gain-pulse control. The converter employs interleaving dual cell power stage for low ripple voltage and fast load transient. It effectively exploits a reconfigurable power stage structure to achieve for fast gain control and adaptive pulse control. The converter was designed with TSMC 0.35-μm CMOS N-well process. With an input voltage ranging from 2.1 to 3.3 V, the converter achieves variable step-down voltage conversion with an output from 0.9 to 1.8 V and a maximum efficiency of 76%. The measured line regulation is 6 mV/V. The system has continuous dynamic voltage scaling capability with the tracking speeds of 7.1 μs/V and 23.3 μs/V for step-up and step-down voltage changes, respectively. The research provides an effective solution to fast-transient low-ripple integrated power converters.

I. INTRODUCTION

In recent years, multi-function portable devices have been proliferating over the electronic industry. The multiple function modules in such a device are usually optimized at different power supply levels. To achieve a long battery runtime and low system profile, efficient and compact power conversion circuits become essential in these systems.

Conventional switching converters provide high power efficiency, but suffer from severe electromagnetic interference (EMI) and bulky system profile, due to the employment of inductive components. Thus, switched-capacitor (SC) dc-dc converters emerge as an alternative solution to integrated power conversion circuit designs. The most commonly used voltage conversion for SC converters is step-up conversion. Classic examples include Dickson charge pumps [1] and cross-coupled voltage doublers [2, 3]. The difficulty of implementing step-down SC converters lies in the fact that it is much harder to maintain high efficiency than its step-up counterparts. Linear regulator does not suffice under this scenario when the dropout voltage is large between the output and the input, due to the inherently poor efficiency. However, as low power operation gets ever-critical in VLSI systems, step-down voltage conversions are on high demands. It will be very attractive if a power-efficient low-EMI step-down SC converter can be invented.

In addition to the concerns on the converters’ topologies, new requirements on system performances also arise. As more and more self-powered portable devices are invented [4, 5], power efficiency in a SC converter can hardly stay high with a fixed voltage conversion ratio. The converter should have excellent line regulation to ensure the reliability when the power source is very unstable. More preferably, it should have adaptively adjustable conversion gain to maintain high efficiency. On the other hand, the output of a converter should be able to promptly respond to fast and frequent load changes. In some applications, the output voltage is required to be variable to dynamically optimize the power and speed of load applications. One perfect example can be found in dynamic voltage scaling (DVS) applications [6]. In this sense, excellent load transient response and even voltage tracking capabilities are paramount to new power converter designs.

In this paper, we introduce a SC power converter with an adaptive gain-pulse control. The converter adaptively employs a reconfigurable SC power stage with adjustable conversion gain ratio and variable power pulses for efficient operation under a wide input range. The dual-loop control ensures fast transient response as well as excellent line and load regulations. Following this introduction, the rest of the paper is organized as follows. In Section II, we address the details of system design and implementation. Section III verifies our design ideas with transistor-based HSPICE simulations. At last, we conclude this research in Section IV.

II. THE PROPOSED SC POWER CONVERTER DESIGN

A. Reconfigurable Interleaving Step-Down Power Stage

Fig. 1(a) Schematic of a CMOS voltage doubler, with (b) timing diagram.
To facilitate a low-noise, fast-transient, efficient SC power converter, we first examine the major drawbacks in the prior arts. Fig. 1 depicts a typical CMOS cross-coupled voltage doubler and its timing diagram. CLK and CLK are the two complementary non-overlapping clocks that determine the switching actions among the power transistors M1-M4. Since the charging time of the pumping capacitor C is usually designed much shorter than the discharging time of the output capacitor C, the doubler’s output voltage V can thus be plotted as in Fig. 1(b). Because the pumping capacitor C connected to V would not be recharged until the next half clock cycle begins, V drops during most of each half clock cycle. Problem occurs when there is a sudden load change. For example, in Fig. 1, a load change from I to I occurs at t. Large voltage ripple (ΔV) would be observed at V, because the circuit cannot respond to this change until the current half clock cycle expires. This affects the transient response and leads to large variation and noise at the regulated power line. In addition, because M1 and M2 are required to be turned on in two non-overlapping phases alternately, the input current of power supply V is discontinuous with a large ripple. This current ripple causes substantial switching noise, which will then be coupled into the entire IC chip, through the power supply metal lines and the substrates of power transistors. Recently, an interleaving SC power converter successfully overcomes these problems by introducing four effective regulation sub-cells and operating each of them with 90° phase shift [6]. However, the design can only achieve step-up conversion with a fixed conversion gain.

Besides the interleaving operation, the two sub-cells, Cell A and B, achieve a step-down conversion in the same manner. We use Cell A and 2/3 conversion gain implementation as one example. In each switching cycle, the operation of Cell A can be divided into two phases: charging phase Φ and discharging phase Φ. During Φ (“0” effective), the PMOS switches M1a, M2a, M5a, and M6a are on. Pumping capacitors C and C are connected in parallel between V and V. The charging current flows from V into the capacitors. During Φ (“0” effective), the switches M1b, M2b, M5b, and M6b are on, and M1a, M2a, M5a, and M6a are off. C and C are connected in series across V. The stored charges are then transferred into V. If C=C, these charging and discharging processes make V equal to 2/3 of V. Similarly, the cells can be reconfigured for different conversion gains.

The method of topology reconfiguration can be explained as follows. Unlike a switching converter, a SC power converter’s efficiency is highly related to its voltage conversion gain. As mentioned in Section I, with a fixed conversion gain, when the input power source is highly variable, the efficiency could drop dramatically. Hence, a reconfigurable SC converter with variable conversion gain is very desirable. This is also achieved in this design and is depicted in Fig. 3. By sensing V through a feed-forward control loop (Section II-B), the controller of the converter determines the instant optimal conversion gain (also called as gain ratio setting). By controlling the gate voltages at each power switch, power stages with different gain ratio setting (GS) can be obtained. In the figure, we demonstrate the reconfiguration scenarios when implementing the GS of 1, 2/3, 1/2, and 1/3, respectively.

![Fig. 2 The proposed step-down power stage with dual interleaving cells.](image)

![Fig. 3 Power stage single cell reconfiguration scenarios.](image)
B. Dual-loop Adaptive Gain-Pulse Control

The control of the proposed converter is in fact a combination of adaptive gain (AG) control and adaptive pulse (AP) control. Different gain ratio in the SC converters has different charge and energy transfer capability. The reconfigurable nature of the power stage allows us to exploit this characteristic to optimize the performances of efficiency and transient response.

However, if only AG control is applied, it faces one critical drawback: the durations for charging and discharging phases are fixed. In the steady state, if the energy delivered in charging phase is much higher than the actual load demand, the converter does not have a ‘fine-tuning’ mechanism to make a self-adjustment. As a result, ripple voltages are high. In addition, at light load, this fixed-frequency fast switching actions dominates the entire power consumption and degrades the efficiency. The AP control thus takes into effect in this scenario. At light load, the load has no urgent energy demand. The controller adaptively reduces the frequency of assigning the pulses. Switching loss of the converter is then reduced and the efficiency thus remains at a relatively high level. When the load has a sudden increase and adaptive pulse control could not supply sufficient energy, AG control takes into charge. It moves the conversion gain ratio to a higher level to maintain low ripple characteristics.

The aforementioned control flows and state transitions are illustrated in Fig. 4. As shown in Fig. 4a, the controller first takes the digital output signals \( a, b \) and \( c \) from the input A/D converter, and then compares them with the pre-stored values of \( a^*, b^* \) and \( c^* \) to detect any line variations from the input power source \( V_{IN} \). If \( V_{IN} \) becomes too higher/too lower, the controller adjusts the GS to a lower value \((-1 \text{ or } -2 \text{ or } -3) / a \) higher value \((+1 \text{ or } +2 \text{ or } +3) \) according to the state diagram in Fig. 4b. Which value will be selected depends on the degree of the variations. If no change is observed at \( V_{IN} \), the converter remains at the previous GS value. After the line variation is settled, the controller then takes the digital load signals \( d, e \) from the output A/D converter. Depending on the values of \( d \) and \( e \) according to the figure in Fig. 4c, if the instant \( V_{OUT} \) is lower than \( V_L (e = 1) \), the GS will be re-adjusted based on the state diagram in Fig. 4d. Otherwise, if the instant \( V_{OUT} \) is higher than \( V_L (e = 0) \) and no GS value needs to be changed in the previous line regulation step, the AP control is initialized to maximize the efficiency. In AP control, when \( V_{OUT} > V_H (d = 1) \), all power switches stay idle to stop the power delivery and save extra switching power. As the load drains charge from \( C_{OUT} \) and \( V_{OUT} \) drops below \( V_H (d = 0) \), the converter resumes the switching actions and charge up to the output \( V_{OUT} \) to the desired level.

C. System Architecture

Fig. 5 shows the system block diagram of the proposed SC dc-dc converter. It consists of four major blocks: Input and Output A/D converters, digital controller and power stage. In this design, the controller employs dual control paths: feedforward and feedback path respectively. In the feedforward path, three hysteretic comparators are used to compare \( V_{IN} \) with \( V_{OREF} \) and feed the result to AG control. AG control block detects the line variation or any change in the reference voltage and changes the GS as discussed in section II-B. It also determines the optimum GS and sends it to the control logic block which decides the activation of AP control. This way, the feedforward path regulates \( V_{OUT} \) and provides fast transient response in case of line variation or DVS implementation. In the feedback path, two fast and accurate comparators compare \( V_{OUT} \) With \( V_{OREF} \) and send the result to both AG and AP control block. Controller then effectively follows the flow chart in Fig. 4a as discussed in section II-B. Thus, the feedback path keeps the output voltage stable and maintains low ripple characteristics. The clock generator in the digital controller provides a pair of non-overlapping phase clocks for the power stage as well as synchronized digital modules in the controller.

III. Simulation Results

The proposed converter was designed and simulated with TSMC 0.35-μm digital CMOS N-well process. All the simulations are HPSICE Level 49 transistor-based. This converter was designed considering a fully integrated solution to low-power low-profile applications. The value of each pumping capacitor in the power stage is 1.5 nF, making the total capacitance only 6 nF. As a tradeoff, the switching frequency was designed at 10 MHz to keep the ripple voltage...
low. The maximum efficiency is 76% at a load power of 39mW with an input voltage of 3.3V and an output voltage of 1.5V. Thanks to excellent line regulation, the converter performs well when the input power source varies from 2.1 to 3.3 V. The dual-loop controller regulates an output voltage, which can continuously stay at any voltage level between 0.9 and 1.8V.

Fig. 6 shows the line regulation performance of the SC converter. With an output reference $V_{OREF}$ of 1.5 V and a load current of 10mA, the input source has severe interference – step changes between 2.1 to 3.25V. The corresponding output waveform shows less than 7% undershoot voltage. With the output voltage change of only 7 mV, the line regulation reaches 6.01 mV/V. The bottom two traces in Fig. 6 demonstrate the gain setting dynamics.

Fig. 7 shows the load regulation performance. With $V_{IN}$ at 3.3 V and $V_{OREF}$ at 1.2 V, the load current experiences a sudden step change from 5 to 75 mA. It takes the converter only 13 us to respond the change and effectively maintain $V_{OUT}$ stable (only 3-mV voltage variation is observed at $V_{OUT}$). As shown in the last two traces in the figure, instead of one high fixed conversion gain ratio (1/2), the converter adapts to a new configuration with a higher gain ratio (1). The high gain stage (1) and regular gain stage (1/2) then operate alternatively to provide a higher equivalent gain. This helps the converter avoid large voltage drops during severe load transient with fast response time.

Fig. 8 shows the dynamic voltage tracking performance for dynamic voltage scaling (DVS) applications. With $V_{IN}$ at 2.7V, the system demands supply voltage changes. $V_{OREF}$ thus steps up and down between 0.9 to 1.8 V. Thanks to adaptive gain control, the converter only takes 6.4 μs to settle at 1.8 V and stay stable there with adaptive pulse control. When the step-down tracking occurs, it takes 20.9 μs to discharge the energy from the output capacitors. These results are much faster than many prior arts. Accordingly, the lower two traces in the figure clearly show the effectiveness of the adaptive gain control during DVS dynamics.

IV. CONCLUSION

A new integrated SC dc-dc converter dual-loop adaptive gain-pulse control is presented. The proposed converter has excellent dynamic response to provide good line and load regulation. Its output reference tracking ability makes it a good candidate for DVS applications. With the reconfigurable power stage, the system can provide high efficiency over a large input range. The compactness along with excellent dynamic response makes the converter an excellent candidate for robust low power supply applications.

REFERENCES