A Family of Zero Current Switching Switched-Capacitor DC-DC Converters

Dong Cao
Department of Electrical & Computer Engineering
Michigan State University
East Lansing, MI 48824, USA
caodong@msu.edu

Fang Zheng Peng
Department of Electrical & Computer Engineering
Michigan State University
East Lansing, MI 48824, USA
fzpeng@egr.msu.edu

Abstract—This paper presents a new zero current switching (ZCS) technique for a family of switched-capacitor dc-dc converters. Compared to the traditional ZCS switched-capacitor dc-dc converters by inserting a magnetic core in the circuit, these new ZCS switched-capacitor dc-dc converters employ the stray inductance present in the circuit as the resonant inductor and provide soft switching for the devices. These ZCS switched-capacitor dc-dc converters do not utilize any additional components to minimize switching loss and reduce the current and voltage spike, thus leading to high efficiency and reliable benefit over traditional switched-capacitor dc-dc converters. Moreover, the bulky capacitor bank existing in traditional switched-capacitor circuits for high power high current application to achieve high efficiency was reduced significantly. Small size, low capacitance, low ESR, high current rating and high temperature rating ceramic capacitors can be employed. Therefore, by using proposed ZCS technique, small size, high power density, high efficiency, high temperature rating, and high current rating switched-capacitor dc-dc converter could be built. Simulation and experimental results are given to demonstrate the validity and features of the soft switching switched-capacitor dc-dc converters.

I. INTRODUCTION

With the technological development of silicon carbide (SiC) and ceramic materials, very high temperature (250 °C) SiC switching devices and ceramic capacitors will be available. But the magnetic cores become dysfunctional at very high temperature. Therefore, magnetic-less switched-capacitor dc-dc converters operating at very high temperatures become possible and attractive with the adoption of natural air cooling by eliminating bulky heat sinks and magnetic cores. There are three main basic structures of traditional switched-capacitor dc-dc converters that is most popular, Marx generator type switched-capacitor dc-dc voltage multiplier shown in Fig. 1 [1-3], charge pump type multi-level modular switched-capacitor dc-dc converter shown in Fig. 2 [4, 5], and generalized multi-level type switched-capacitor dc-dc converter shown in Fig. 3 [6-9]. The derivation circuits of generalized multi-level type switched-capacitor dc-dc converter are also popular in automotive applications [10-14]. However, there are many common drawbacks in traditional switched-capacitor dc-dc converters for high power and high current automotive application. A huge capacitor bank with high capacitance has to be utilized in order to
reduce the voltage ripple of the capacitors and achieve high efficiency, which will undoubtedly increase the size of the converter [7, 10, 13, 15]. Besides, with the increase of current rating, huge turn off current leads to unneglectable switching loss of the device. High voltage overshoot is also caused by large turn off current. Moreover, EMI problems caused by the di/dt and dv/dt generated during the switching transient are undesirable in automotive applications.

In order to reduce the switching loss, voltage spikes, and EMI, several ZCS methods have been proposed by inserting an inductor in series with the capacitor [16-21]. But these methods require a relatively big resonant inductor (larger than 1 µH) which is not viable to be achieved by the circuit stray inductance as claimed. By inserting a magnetic core in the switched-capacitor circuit to achieve ZCS is a contradiction by itself. The switched-capacitor circuit with a magnetic core is not a switched-capacitor circuit anymore. Many good features of switched-capacitor will lose including good integration capability, small size and high temperature operation. Also, to utilize the parasitic inductance in the circuit, the switching frequency has to be pushed to tens of megahertz by using these methods, which is not technically feasible [22-24].

This paper presents a new ZCS strategy for a family of switched-capacitor dc-dc converters that is able to overcome the aforementioned drawbacks of traditional switched-capacitor dc-dc converters without inserting big magnetic cores or increasing switching frequency to megahertz level. This new strategy can achieve the ZCS for all the switches without losing any the good features of switched-capacitor circuit compared to the traditional ZCS strategy. This ZCS strategy employs the distributed parasitic inductance in the circuit resonating with the capacitors to provide zero current transition to the switching devices. So, the switching loss is minimized, voltage spike is reduced and EMI is limited. In case the stray inductance is not sufficiently large or equalized as expected, small air core inductors (less than 100n) or layout PCB wires can be used to meet the requirement of the stray inductance. By considering the influence of stray inductance, the power loss is only related to the conduction loss of capacitors and switching devices without considering gate drive and control loss, which is different from the traditional switched-capacitor circuits. Therefore, bulky capacitor banks with high capacitance to reduce voltage ripple and achieve high efficiency are no longer needed, while small size MLCC capacitors with low ESR and low capacitance can be adopted to increase power density and reduce the converter size. No extra components are added in the presented soft switching strategy, thus making it reliable and low in cost. A 160 W ZCS switched-capacitor dc-dc multiplier is analyzed and simulated to confirm the proposed ZCS strategy. A 12 V input 480 W ZCS voltage doubler prototype is also designed and built to confirm the operation, simulation and experiment results are provided.

II. PROPOSED ZCS SWITCHED-CAPACITOR DC-DC CONVERTER FAMILY

Fig. 4, Fig. 5, and Fig. 6 show the proposed ZCS switched-capacitor family utilizing the distributed parasitic inductance existing in the circuit. Fig. 4 shows the N-level ZCS switched-capacitor dc-dc voltage multiplier. Fig. 5 shows the N-level ZCS multi-level modular switched-capacitor dc-dc converter (ZCS-MMSCC) which has already been discussed in detail in [25]. Fig. 6 shows the N-level ZCS generalized multi-level switched-capacitor dc-dc converter. The parasitic inductance mainly includes the stray inductance due to the circuit layout, MOSFETs package parasitic inductance and the capacitor ESL. The stray inductance caused by circuit layout is usually the dominant part. By designing the circuit layout properly, the inductance needed for resonant can be achieved. In case the circuit layout is not well designed or equalized as expected, an air core inductor could be inserted to achieve the prerequisite distributed stray inductance. Because resonant inductors are distributed in the circuit, only small resonant inductance is needed for resonant. Therefore, ZCS of all the switching devices can be achieved by the resonant of the capacitor and the distributed stray inductance in the circuit.

III. OPERATION PRINCIPLE

A. ZCS Switched-Capacitor DC-DC Voltage Multiplier

Fig. 7 shows the four-level ZCS switched-capacitor dc-dc voltage multiplier as an example. Similar to the four-level ZCS-MMSCC, this circuit also works as a four times step-up dc-dc converter. \( V_{in} \) represents the ideal input voltage source.
L_{S1} - L_{SP} represents the equivalent stray inductance present in the circuit. L_{S2}, L_{C4} and L_{SP} are the equivalent stray inductance when the capacitor is charged in parallel. L_{S2}, L_{C5} and L_{SP} are the equivalent stray inductance between each capacitor when the capacitor discharges in series. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_1 to C_3 are the capacitors with the average voltage of input voltage, while C_4 has the average voltage of four times of input voltage. L_S does not have to be in the position drawn in Fig. 7, it could be distributed anywhere in series with switches or capacitors in the circuit. Similar to the ZCS-MMSCC, the total equivalent stray inductance is the sum of the connection wire parasitic inductance, capacitor parasitic inductance and the MOSFETs package parasitic inductance. Usually the connection wire parasitic inductance is the major part of the stray inductance. For the analysis convenience, only one equivalent L_S is used to represent the total stray inductance present in each parallel resonant loop. And one equivalent L_S is used between two capacitors in the series resonant loop.

Fig. 7. Four-level ZCS switched-capacitor voltage multiplier main circuit.

Fig. 8 shows the idealized waveform of proposed ZCS switched-capacitor dc-dc voltage multiplier under steady-state conditions. V_{GS_Sp} and V_{GS_SN} are the gate signal of switch S_P and S_N with 50% duty cycle. V_{DS_SP} and V_{DS_SN} are the drain source voltage of the switch S_P and S_N. Actually, the drain source voltage of different S_P and S_N are different in value but similar in shape due to the characteristics of voltage multiplier circuit. I_{SP} and I_{SN} are the drain source current of the switch S_P and S_N. All the switches of S_P or S_N have the same current waveforms. Assume input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches S_P, S_N and stray inductance will decrease to zero when the switches are turned off. The half switching period is a half sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. The capacitor C_1, C_2 and C_3 are charged in parallel in the half-period with the sinusoidal current waveform when S_P is on. And they are discharged in series with the input voltage source in another half-period also in the sinusoidal shape when S_N is on. I_{C1,2,3} are the current through capacitor C_1, C_2, and C_3, which is the sum of the current through the switch with the sinusoidal shape. When the capacitor is charged, the current is the positive part; when the capacitor discharges, the current is negative. The capacitor C_4 is charged when other capacitors are in series with input voltage when S_N is on. And it is discharged to the load when S_P is on. I_{C4} is the current through capacitor C_4, which is a sinusoid waveform when S_N is on. When S_P is on, the current through C_4 is the negative dc load current with small ripple.

V_{C1,2,3} is the voltage across the capacitor C_1, C_2 and C_3 with the input voltage dc offset and a sinusoidal ripple. The voltage ripple is determined by the capacitor current and capacitance. V_{C4} is the voltage across the capacitor C_4, with the dc offset four times input voltage and a voltage ripple also determined by the capacitor current and capacitance. The operation of this circuit can be described in two states shown in Fig. 9 and Fig. 10 with different switches turned on.

Fig. 8. Ideal waveforms of four-level ZCS voltage multiplier.

Fig. 9. Operation modes of state I when S_P is on.

Fig. 10. Operation modes of state II when S_N is on.
1) State I \([t_0,t_1]\)

Fig. 9 shows the state when \(S_P\) is turned on at \(t = t_0\) while \(S_N\) is off. During this state, \(C_1\), \(C_2\) and \(C_3\) are charged by \(V_{in}\). Fig. 11 show the three simplified equivalent circuits of state I. Fig. 11(a) shows the situation when \(V_{in}, L_{S2}, S_{P1}, C_1\) and \(S_{P2}\) form a resonant loop. Fig. 11(b) shows the situation when \(V_{in}, L_{S4}, S_{P3}, C_2\) and \(S_{P4}\) form a resonant loop. Fig. 11(c) shows the situation when \(V_{in}, L_{S5}, S_{P5}, C_3\) and \(S_{P6}\) form a resonant loop. Because of the presence of the stray inductance \(L_{S}\), before the switch is turned on, the current through \(L_{S}\) already decreases to zero. The current through \(S_P\) will increase from zero when the switch is turned on, so \(S_P\) is turned on at zero current. For the case shown in Fig. 11(a), after \(L_{S2}\) and \(C_1\) resonate for half cycle, the current through \(S_{P1}\) and \(S_{P2}\) falls to zero. Therefore \(S_{P1}\) and \(S_{P2}\) turn off at zero current. Similarly, for the case shown in Fig. 11(b) and Fig. 11(c) the current through \(S_{P3}\), \(S_{P4}\), \(S_{P5}\) and \(S_{P6}\) will realize zero current turn on and turn off too. So, ZCS is achieved on all the switches. The required stray inductance value is the same for the three circuit and is easy to be achieved by the circuit layout due to the symmetry of the circuit, assuming the capacitance are the same.

![Simplified equivalent circuits of state I when \(S_P\) is on.](image)

Fig. 11.

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assuming \(C_1 = C_2 = C_3 = C_4\), so in order to have the same resonant frequency, \(L_{S2} = L_{S4} = L_{S6}\). Assume \(L_{S1} = L_{S3} = L_{S5} = L_{S7}\). The state equations of Fig. 11(a) are:

\[
V_{in} = L_{S2} \frac{d}{dt} i_{S2} + v_{C1} \\
\]

\[
i_{S2} = C_1 \frac{dv_{C1}}{dt} \\
\]

The solutions are:

\[
i_{S2}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \\
\]

\[
v_{C1}(t) = V_{in} - \frac{\pi P_o}{4V_{in}C_1 \omega_r} \cos \omega_r t \\
\]

Where \(V_{in}\) is the value input voltage, \(L_{S2}\) is the value of stray inductance, \(\omega_r\) is the resonant frequency equals to \(1/\sqrt{L_{S2}C_1}\), and \(P_o\) is the output power. After half cycle, the capacitor voltage is charged to:

\[
v_{C1}(t) = V_{in} + \frac{\pi P_o}{4V_{in}C_1 \omega_r}. \\
\]

The capacitor voltage ripple is:

\[
\Delta v_{C1} = \frac{\pi P_o}{4V_{in}C_1 \omega_r} \\
\]

The state equations of Fig. 11(b) and Fig. 11(c) are similar to the state equations of Fig. 11(a). The voltage across \(C_2\) and \(C_3\) are the same as the voltage across \(C_1\). The voltage ripples of \(C_2\) and \(C_3\) are also the same as \(\Delta v_{C1}\).

2) State II \([t_1,t_2]\)

Fig. 10 shows the state when \(S_N\) is turned on at \(t = t_1\) while \(S_P\) is off. During this state, \(C_4\) is charged by the \(V_{in} C_1\) \(C_2\) and \(C_3\) in series. Assume the load is zero. Fig. 12 shows the simplified equivalent circuits of state II. It shows the situation when \(V_{in}, L_{S1}, S_{N1}, C_1, L_{S3}, S_{N2}, C_2, L_{S5}, S_{N3}, C_3, L_{S7}, S_{N4}, C_4\) and \(L_{S7}\) form a resonant loop. Similar as the last state, because of the presence of the \(L_5\), the current through \(S_N\) will also increase its value from zero in a resonant manner. The zero current turn-on of \(S_N\) can be achieved. After stray inductance \(L_{S1}, L_{S3}, L_{S5}\) and \(L_{S7}\) in series resonate with capacitor \(C_1, C_2, C_3\) and \(C_4\) in series for half cycle at \(t = t_2, S_{N1}, S_{N2}, S_{N3}\) and \(S_{N4}\) will have a zero current turn-off when the current through them decreases to zero. Hence, zero current switching can be achieved on these switches.

![Simplified equivalent circuits of state II \(S_N\) is on.](image)

Fig. 12.

The state equations of Fig. 12 are:

\[
V_{in} + v_{C1} + v_{C2} + v_{C3} = 4L_{S1} \frac{di_{S1}}{dt} + v_{C4} \\\n\]

\[
i_{S1} = C_4 \frac{dv_{C4}}{dt} \\\n\]

The solutions are:

\[
v_{C4}(t) = 4V_{in} - \frac{\pi P_o}{4V_{in}C_4 \omega_r} \cos \omega_r t \\\n\]

\[
i_{S1}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \\\n\]

After half cycle, the capacitor voltage is charged to:

\[
v_{C4}(t) = 4V_{in} + \frac{\pi P_o}{4V_{in}C_4 \omega_r} \\\n\]

The capacitor voltage ripple is:
If zero load is considered, the required stray inductance in the series resonant loop is the same as the parallel resonant loop shown in Fig. 11 which means \( L_{S1} = L_{S2} = L_{S3} = L_{S4} = L_{S5} = L_{S6} = L_{S7} = L_{S8} = L_{S9} = L_{S10} \). After considering the load effect with a negative dc offset in the capacitor \( C \) current. The required stray inductance of series resonant loop will be a little bit smaller than the parallel resonant loop. Because the resonant frequency of a pure LC network is different with the LCR network.

**B. ZCS Voltage Doubler**

Fig. 13(a) shows the two-level ZCS generalized multi-level switched-capacitor dc-dc converter as an example. This circuit is called ZCS voltage doubler in short because the output voltage is twice as much as the input. \( V_{in} \) represents the ideal input voltage source. \( L_{S1}, L_{S2}, L_{S3}, \) and \( L_{S4} \) can be considered as the distributed stray inductance in series with the switches in the circuit layout. \( S_P \) and \( S_N \) are the same switching devices controlled complementary at 50% duty cycle. \( C_1 \) and \( C_2 \) are the capacitors with the average voltage the same as the input voltage. Because of the symmetry of the circuit, the distributed stray inductance \( L_{S1}, L_{S2}, L_{S3}, \) and \( L_{S4} \) can be replaced with an equivalent stray inductance \( L_S \) in the input side shown in Fig. 13(b) for the analysis convenience. Only one equivalent stray inductance \( L_S \) is needed to represent the total stray inductance in two resonant loop.

![ZCS voltage doubler and its topology simplification.](image)

**Fig. 13.** ZCS voltage doubler and its topology simplification.

Fig. 14 shows the idealized waveform of proposed ZCS voltage doubler under steady-state conditions. \( V_{GS_{Sp}} \) and \( V_{GS_{Sn}} \) are the gate drive signal of switch \( S_P \) and \( S_N \) complementary with 50% duty cycle. \( V_{DS_{Sp1}} \) to \( V_{DS_{Sn2}} \) are the drain source voltage of switch \( S_P \) and \( S_N \). \( I_{Sp} \) and \( I_{Sn} \) are the drain source current of the switch \( S_P \) and \( S_N \). All the switches of \( S_P \) or \( S_N \) have the same current waveforms. Assume input voltage is an ideal voltage source. By considering the equivalent stray inductance in the input side, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches \( S_P, S_N \) and stray inductance will decrease to zero when the switches are turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. \( I_{C1} \) and \( I_{C2} \) are the current through capacitor \( C_1 \) and \( C_2 \). The capacitor \( C_1 \) and \( C_2 \) are charged in each half-period with the sinusoidal current waveform when \( S_P \) or \( S_N \) is on. And they are always discharged in series with load current. So, the current through the capacitor \( C_1 \) and \( C_2 \) is the current through the switch subtracts the output current. \( V_{C1} \) and \( V_{C2} \) are the voltage across the capacitor \( C_1 \) and \( C_2 \). \( Vo \) is the output voltage with the voltage ripple half of the voltage ripple of the capacitor. Because of the 180 degree phase shift of the capacitor voltage ripple, the capacitor voltage ripple will cancel out with each other. The operation of the circuit can be described in two states as shown in Fig. 15(a) and Fig. 15(b) with different switches turned on.

![Ideal waveforms of ZCS voltage doubler.](image)

**Fig. 14.** Ideal waveforms of ZCS voltage doubler.

![Operation modes of state I when \( S_P \) is on.](image)

**Fig. 15.** (a) Operation modes of state I when \( S_P \) is on. (b) Operation modes of state II when \( S_N \) is on.
IV. Design Guidelines

The 480 W ZCS voltage doubler design procedure is shown here as an example. The specification of the prototype converter is $V_{in}=12$ V, $V_o=24$ V, $P_o=480$ W, $f_s=44.25$ kHz.

A. Capacitance

Capacitance value should be chosen according to the voltage ripple of the capacitor using the following equation.

$$C = \frac{\pi P_o}{2V^2_m\Delta V_c\omega_s} \quad (13)$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors are the same. And the value of the voltage ripple is determined by the output power, input voltage, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the capacitor from resonating to the negative region and lose the zero current switching. The output voltage ripple is about five times smaller than the capacitor voltage ripple because of the 180 degrees phase shift operation of the switches. And the capacitor voltage ripple will cancel out and the output voltage is two times bigger than one capacitor voltage. The output ripple is chosen around 8% of output voltage. So the capacitor voltage ripple is 40% of the capacitor voltage. According to the (13), the capacitance is chosen 47 μF in the simulation.

B. Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. Assume all the stray inductance in the circuit is equalized. And the required stray inductance can be satisfied by using proper input inductance. Required stray inductance for ZCS can be determined by the resonant LCR network.

C. Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used for the input inductance, and the switching frequency can be determined by the input inductance value. If the input inductance is determined, the switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

V. Simulation and Experiment Results

A. ZCS Voltage Multiplier

Fig. 16 shows saber® simulation waveforms of a 160 W ZCS voltage multiplier, where $V_p$ and $V_n$ are the switch gate-source control voltage, $V_{ds_Sp}$ and $V_{ds_Sn}$ are the switch drain-source voltage, $I_{Sp}$ and $I_{Sn}$ are the switch drain-source current. $I_{C1,2,3}$ is the current through capacitor $C_1$, $C_2$ and $C_3$. $V_{C1,2,3}$ is the voltage across the capacitor $C_1$ and $C_2$. $V_{in}$ is the input voltage. $V_o$ is the output voltage or the voltage across the capacitor $C_4$. The input voltage is 5 V. Switching frequency is about 70 kHz. Capacitance is 47 μF and the value of the stray inductance $L_{S2}=L_{S4}=108$ nH, $L_{S1}=L_{S3}=L_{S5}=L_{S7}=98$ nH. The series resonant stray inductance is smaller caused by the load effect. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

B. ZCS Voltage Doubler

Fig. 17 and Fig. 18 shows saber® simulation waveforms of a 480 W ZCS voltage doubler, where $S_p$ and $S_n$ are the switch gate-source control voltage, $V_{ds_Sp1}$, $V_{ds_Sn1}$, $V_{ds_Sp2}$, $V_{ds_Sn2}$ are the switch drain-source voltage of switch $S_{p1}$, $S_{n1}$, $S_{p2}$ and $S_{n2}$. $I_{Sp}$ and $I_{Sn}$ are the switch drain-source current of switches $S_{p1}$ and $S_{n1}$. The current through $S_{p2}$ and $S_{n2}$ is the same as $S_{p1}$ and $S_{n1}$. $I_{in}$ is the current through the input stray inductance $L_S$. $I_{C1}$ and $I_{C2}$ are the current through capacitor $C_1$ and $C_2$. $V_{C1,2,3}$ and $V_{C4}$ are the voltage across the capacitors $C_1$ and $C_2$. $V_{in}$ is the input voltage. $V_o$ is the output voltage. The input voltage is 12 V. Switching frequency is about 44 kHz. Capacitance is 47 μF and stray inductance $L_S=165$ nH. The simulation results is consistent with the theoretical analysis, which verifies the analysis.
In the 480 W ZCS voltage doubler prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from Infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 µF MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are twelve 16 V 470 µF conductive polymer aluminum solid electrolytic capacitors PLG1C471MDO1 from Nichicon connected in parallel. Gate drive voltage is 7 V. The switching frequency is about 40 kHz. The input stray inductance is around 200 nH.

Fig. 19 and Fig. 20 show the experiment waveforms of the 480 W ZCS voltage doubler prototype with the parts mentioned above. Fig. 19 shows the complementary gate drive signals of $S_P$ and $S_N$ with duty cycle about 49% due to some dead time. $V_{GS_Sp}$ and $V_{GS_SN}$ are the complementary gate-source control voltage.

VI. CONCLUSION

In this paper, a family of zero current switching switched-capacitor dc-dc converters is proposed. By eliminating the bulky, lossy inductive component with a magnetic core, the
converter is able to operate at very high temperatures with high efficiency. By using the proposed soft-switching strategy, switching loss has been minimized and EMI has been restricted; the size of capacitors has been reduced, thus making the converter small and light. Owing to the utilization of distributed stray inductance or distributed air core inserting technique, the big inductor is avoided to achieve ZCS. Hence, the proposed ZCS switched-capacitor converter family shows great potential in high temperature, high power future automotive applications.

REFERENCES


