and continues until an EOM pulse occurs.

Playback begins at selected starting address

OE ← 0 momentarily or longer.
OE ← 0
Pd ← 1
D0 - D7 Set to Playback Start Address

P/A ← 1
P/A ← 1
Pd ← 1
To Playback

The system stores an End Of Message pulse (1.0-1.15 ms) at end of recording (20 secs. max.).

OE ← 0
OE ← 0 during record
OE ← 0
OE ← 1
Pd ← 1
D0 - D7 Set to Record Start Address

P/A ← 1
Pd ← 1
To Record

Control function
3 bits which

Power Down and Reset
OE ← 0
 OE ← 0
 OE ← 0
 PD ← 1
 P/A ← 1
Pd ← 1

Playback/Record
OE ← 0
OE ← 0
OE ← 0
PD ← 1
PA ← 1
Pd ← 1

Chip Enable
OE ← 0
OE ← 0
OE ← 0
PD ← 1
P/A ← 1
Pd ← 1

End Of Message signal
OE ← 0
OE ← 0
OE ← 0
PD ← 1
P/A ← 1
Pd ← 1

Built-in 16G

Loudspeaker

Supply

+10V

Input from

July 1196

2:24 now apt.

Modification

Drawing name: Programmable Sound Recorder

Project name: Midgumim - Model 1347 Lab
ISD1012A/1016A/1020A Single-Chip Voice Record/Playback Devices

FEATURES

- Natural, high-quality playback suitable for voice, music, and tones
- Single-chip voice record and playback device
  - Direct analog storage technology
  - Microphone preamplifier
  - Automatic gain control
  - Anti-aliasing and smoothing filters
  - Speaker amplifier
- Eliminates digital memory, data converters, modulators, and battery back-up circuits
- Easy-to-use; programming and development system not required
- Flexible record and playback control options
- Nonvolatile EEPROM technology—zero power storage and 10K record cycles
- 10-year voice retention
- Power down mode for lowest power consumption
- Single 5-volt power supply
- Multiple message address options
- Directly cascadable for longer storage duration
- Manual switch or microprocessor controllable
- Significantly reduced EMI generation and high immunity to external EMI

ISD1000A FAMILY SUMMARY

The ISD1000A Family includes three device types. ISD1000A Family replaces ISD1000 Family with improved noise characteristics. The ISD1000A Family is fully compatible with the ISD1000 Family. The table summarizes the characteristics of each device.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Record/Playback Duration (seconds)</th>
<th>Input Sample Rate (KHz)</th>
<th>Upper Pass Band Limit (KHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISD1012A</td>
<td>12</td>
<td>10.6</td>
<td>4.5</td>
</tr>
<tr>
<td>ISD1016A</td>
<td>16</td>
<td>8</td>
<td>3.4</td>
</tr>
<tr>
<td>ISD1020A</td>
<td>20</td>
<td>6.4</td>
<td>2.7</td>
</tr>
</tbody>
</table>

ISD1012A, 1016A, 1020A BLOCK DIAGRAM
GENERAL DESCRIPTION

The ISD1000A Family of devices is designed to record and playback audio and voice information in a single chip with a minimum of circuit complexity. This compact, easy-to-use, nonvolatile, low-power solution has been made possible by ISD’s patented DAST™ technology—a breakthrough in Direct Analog Storage Technology in EEPROM. ISD’s DAST technology results in storage density that is eight times greater than digital memory. The DAST nonvolatile analog array consists of 128K cells—the equivalent of 1M bits of digital storage.

The ISD1000A Family eliminates the need for digital conversion, digital compression, and voice synthesis techniques that often compromise voice quality and complicate usage. The ISD1000A Family of devices includes signal conditioning circuits and control functions which enable a complete, high quality recording and playback system in a single device. The ISD1000A is available in three versions which store voice in 12, 16, or 20 second DAST arrays. Additional devices may be cascaded to achieve longer recording durations. The nonvolatile storage array is based on production-proven, low-power CMOS EEPROM technology.

The highly integrated ISD1000A Family contains all of the basic functions required for high quality voice recording and playback. The noise cancelling Microphone Preampifier and Automatic Gain Control (AGC) records both low volume and high volume sounds. The AGC attack and release times are adjusted by an external resistor and capacitor. Antialiasing is performed by a continuous fifth-order

Chebyshev filter requiring no external components nor clocks to give toll quality reproduction. The low corner of the passband is user-settable by two external capacitors. The devices contain their own temperature-stabilized time-based oscillator.

The ISD1000A devices drive a speaker directly through differential outputs which boosts output by four times and eliminates the need for an output amplifier. A series capacitor requirement is also eliminated. The device will operate from single 5-volt power supplies or from batteries. The device also includes a power down function for applications where minimum power consumption is critical. The CMOS-based design, combined with the nonvolatile storage array, assures lowest possible overall power consumption.

On-chip control functions make the ISD1000A Family very easy to use in virtually any application. Each device offers a variety of operating modes and interface options. The devices may be used in applications that require little more than a few switches and a battery. The devices may also be integrated into electronic systems where digital addresses can be provided for more sophisticated message addressing and control. The ISD1000A DAST arrays are organized in 160 segments. Addresses A0 through A7 provide access to each segment in the array for message addressing. Addressing provides the capability of constructing messages by concatenating stored phrases and sounds.

PIN NAMES

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin #</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0–A5</td>
<td>1–6</td>
<td>Address</td>
</tr>
<tr>
<td>A6–A7</td>
<td>9, 10</td>
<td>Address</td>
</tr>
<tr>
<td>VCCD</td>
<td>28</td>
<td>VCC Digital Power Supply</td>
</tr>
<tr>
<td>VCCA</td>
<td>16</td>
<td>VCC Analog Power Supply</td>
</tr>
<tr>
<td>VSD</td>
<td>12</td>
<td>VSS Digital Ground</td>
</tr>
<tr>
<td>VSSA</td>
<td>13</td>
<td>VSS Analog Ground</td>
</tr>
<tr>
<td>SP+</td>
<td>14</td>
<td>Speaker Output +</td>
</tr>
<tr>
<td>SP−</td>
<td>15</td>
<td>Speaker Output −</td>
</tr>
<tr>
<td>Test (CLK)</td>
<td>26</td>
<td>Test—Must be tied Low</td>
</tr>
<tr>
<td>Aux In</td>
<td>11</td>
<td>Auxiliary Input</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin #</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ana Out</td>
<td>21</td>
<td>Analog Output</td>
</tr>
<tr>
<td>Ana In</td>
<td>20</td>
<td>Analog Input</td>
</tr>
<tr>
<td>AGC</td>
<td>19</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>Mic</td>
<td>17</td>
<td>Microphone Input</td>
</tr>
<tr>
<td>Mic Ref</td>
<td>18</td>
<td>Microphone Reference</td>
</tr>
<tr>
<td>PD</td>
<td>24</td>
<td>Power Down</td>
</tr>
<tr>
<td>P/R</td>
<td>27</td>
<td>Playback/Record</td>
</tr>
<tr>
<td>EOM</td>
<td>25</td>
<td>End-of-Message</td>
</tr>
<tr>
<td>CE</td>
<td>23</td>
<td>Chip Enable</td>
</tr>
</tbody>
</table>
ISD1000A FAMILY PIN ASSIGNMENTS

ISD1012A
ISD1016A
ISD1020A

DIP and SOIC

28 V㎜
27 P/R
26 Test 9CLK)
25 EOM
24 PD
23 ₍
22 NC
21 Ana Out
20 Ana In
19 AGC
18 Mic Ref
13 Mic
16 Vᵦᵦ
15 SP−

Microphone Input (Mic)
The microphone is AC-coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor (together with the 10K ohm resistance internal to the ISD1000A) determines the low frequency cut-off for the ISD1000A passband.

Microphone Reference (Mic Ref)
When AC is coupled to microphone ground, the recorded noise level is significantly reduced. Ground noise is referenced to the preamplifier. If this pin is not used, it must NOT be connected to any signal or voltage. It must float.

Analog Output (Ana Out)
The microphone signal is amplified and is output to the Ana Out pin. The voltage gain of the pre-amp is determined by the voltage level at the Automatic Gain Control (AGC) pin. It has a maximum gain of about 24dB for small input signal levels.

Analog In (Ana In)
The external capacitor connects Ana In to the Ana Out pin. The value of the external capacitor, together with the 2.7KΩ input impedance at Ana In, can be chosen to give additional cut-off at the low frequency end of the voice passband. The Ana In pin may also be used to input alternative sources of analog signal, other than the microphone signal.

Automatic Gain Control (AGC)
The purpose of the AGC is to dynamically adjust the preamplifier gain, and therefore extend the range of input signals which can be applied to the microphone input without distortion. The AGC considerably extends the range of recordable sounds from whispers to loud voices. Peak voltage levels at the Amplifier output are detected in the AGC circuit, and charge the external capacitor C2 on the AGC Control pin. The source resistance (5KΩ) of the internal AGC circuit and the external capacitor C2 determine the “attack” time of the gain control. Release time is determined by the RC time constant of the external resistor (R2) and capacitor (C2). For AGC voltages of 1.5V and below, the preamplifier is at its maximum gain 24dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8V.

Speaker Outputs (SP+/SP−)
The SP+ and SP− pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct drive loudspeakers, the two opposite polarity outputs give an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP− connections are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC coupling capacitor between the SP pin and the speaker. The speaker outputs are held at V㎜ during recording and Power Down.
PIN DESCRIPTION, continued

Power Down (PD)
The Power Down pin is taken high (when not recording or playing back) to provide a very low power mode to the ISD1000A. When EOM goes for overflow condition, PD must be brought High to reset addresses.

Chip Enable (CE)
The Chip Enable pin is taken low to enable all playback and record operations. The address inputs (A0-A7) and the playback/record input are latched into the ISD1000A by this falling edge. When CE is taken high, the ISD1000A is unselected, and the auxiliary input is directed into the speaker power amplifier.

Playback/Record (P/R)
The state of the P/R is latched into the ISD1000A on the falling edge of CE. A High level selects a playback cycle, while a Low level selects a record cycle. During record, the playback circuits and speaker output amplifiers are powered down, and the SP+ and SP- outputs are held at Vma. During playback, the internal record and analog inputs are disabled. In playback mode, it is only necessary to supply the starting message address. The ISD1000A will playback until an End of Message is encountered (see Table 1, Page 5 for other options). In record mode, the start address determines the beginning of the message. The ISD1000A Family records until CE is brought High or until an overflow is detected.

Address Inputs (A0-A7)
The Address Inputs provide two functions in the ISD1000A Family:

1. Message address (A6 OR A7 = Low)
2. ISD1000A Family Operational Mode Options (A6 AND A7 = High)

Operational mode options are shown in Table 1 (Page 5). There are a maximum of 160 message addresses (or segments). Each segment corresponds to one of 160 rows in the analog storage array. The message addresses (segments) are in locations 0 through 159 contiguous. The playback/record duration of each segment depends on the device and is as follows:

<table>
<thead>
<tr>
<th>Family Member</th>
<th>Segment Playback/Record Duration (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISD1012A</td>
<td>0.075</td>
</tr>
<tr>
<td>ISD1016A</td>
<td>0.100</td>
</tr>
<tr>
<td>ISD1020A</td>
<td>0.125</td>
</tr>
</tbody>
</table>

An operation may be started at any address, as defined by address pins A0-A7. Record or playback continues with automatic incrementing of internal on-chip address until either CE is brought high (record), an end of message bit is encountered (playback with CE high) or an overflow (device full) condition results.

Test (CLK)
Test (CLK) is normally only used by manufacturing for test. In applications circuits it is tied to ground, however, if greater timing precision is desired, (internal clock has ±2% tolerance over temperature and voltage range) the chip can be externally clocked through this pin.

For the ISD1016A this clock is a 1024 KHz signal; the ISD1012A is 1365 KHz; and the ISD1020A is 819 KHz. The duty cycle is not critical, as this clock is immediately divided by two.

End of Message (EOM)
A digital End-of-Message marker is automatically inserted in an internal nonvolatile register at the end of each recorded message. The EOM output goes Low under the following conditions:

- At end of each message
- Message overflow (device full)

The ISD1000A Family has an internal Vcc detect circuit. When Vcc drops below 3.5V, EOM is forced Low and the device is placed in playback mode. The EOM marker provides a convenient handshake signal for a processor. The EOM function also facilitates cascading.

Auxiliary Input (Aux-In)
The input to the internal output power amplifier is multiplexed between the storage array and the auxiliary input pin. The auxiliary input is active when CE=High and playback has ended or EOM=Low due to overflow. The active power amplifier input (storage array or auxiliary input) inhibits the other input. (For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.) The Auxiliary Input also facilitates cascading.

Vccx and Vcc (±5.0 Volts)
Analog and digital circuits internal to the ISD1000A Family use separate power buses to minimize noise on the chip. These +5 Volt buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the +5 Volt supply be decoupled as close as possible to the package.

Vma and Vma (Ground)
Similar to Vccx and Vcc, the analog and digital circuits internal to the ISD1000A Family use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.
OPERATIONAL MODES

The ISD1000A Family can be used in systems with various levels of control sophistication, from microprocessor-controlled environments to simple push-buttons or switches. Different operational modes are enabled by taking address pins A7 AND A6 HIGH. In this mode, the states of address pins A5 through A0 determine the control function and NOT the message address. The options are shown in the Table below. Each option is selected by bringing the appropriate address High. Multiple options may be selected by applying a High level to each of the desired address pins.

Table 1. Operational Modes

<table>
<thead>
<tr>
<th>Function</th>
<th>Address Control (High)</th>
<th>Pin #</th>
<th>Typical Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Message cueing (speaker output disabled).</td>
<td>A0</td>
<td>1</td>
<td>Selecting messages when address is unknown.</td>
</tr>
<tr>
<td>(See Note 1)</td>
<td></td>
<td></td>
<td>Indirect message addressing.</td>
</tr>
<tr>
<td>EOM markers are deleted by the next message use with (A4 = 1). (Available Q3/1992)</td>
<td>A1</td>
<td>2</td>
<td>Position a single EOM marker at the end of the last message.</td>
</tr>
<tr>
<td>During playback, EOM pulses low at array overflow only (used for cascading function).</td>
<td>A2</td>
<td>3</td>
<td>Playing back messages whose duration exceeds a single chip limitation.</td>
</tr>
<tr>
<td>Continuous playback (at EOM loops back to beginning and repeats message).</td>
<td>A3</td>
<td>4</td>
<td>Continuous repeat.</td>
</tr>
<tr>
<td>Consecutive addressing – Message start pointer is reset only when operational mode is changed (playback/record). (See Note 2)</td>
<td>A4</td>
<td>5</td>
<td>Recording consecutive multiple messages.</td>
</tr>
<tr>
<td>Playback is chip enable level activated.</td>
<td>A5</td>
<td>6</td>
<td>Terminate playback with CE.</td>
</tr>
</tbody>
</table>

Notes:

1. **Message Cueing (Available Q3, 1992)**

   Message cueing allows the user to skip through messages. Each time CE memory is pulsed Low with the address inputs set to this mode, the internal message pointer skips forward until it encounters an end-of-message marker and then stops. By providing a certain number of pulses to the CE pin in message cueing mode and then changing to consecutive addressing mode, the user can select and then record or playback a desired message. Message cueing should not be used in Record mode.

2. **Consecutive Addressing**

   Consecutive addressing allows for recording and playback of consecutive messages without the need for direct addressing or any other kind of message management. During recording, each time CE is taken Low, a message is recorded at the next position in memory. When CE is taken High again, an End-of-Message marker is written to indicate the position of the End of the message. In this fashion, a string of messages is recorded, each one placed immediately after the previous one.
APPLICATION EXAMPLE— DESIGN SCHEMATIC

Note: If desired, this pin may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage.

APPLICATION EXAMPLE— BASIC DEVICE CONTROL

<table>
<thead>
<tr>
<th>Control Step</th>
<th>Function</th>
<th>Action</th>
</tr>
</thead>
</table>
| 1            | Power-up chip and select record/playback mode | 1. PD = Low  
2. P/R = As desired |
| 2            | Set message address for record/playback  | Set addresses A0–A7         |
| 3            | Begin record/playback                    | CE = Low                   |
| 4            | End cycle                                | CE = High                  |

APPLICATION EXAMPLE— PASSIVE COMPONENT FUNCTIONS

<table>
<thead>
<tr>
<th>Part</th>
<th>Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>Microphone power supply decoupling network</td>
<td>Reduces power supply noise</td>
</tr>
<tr>
<td>R2</td>
<td>Release time constant</td>
<td>Sets release time for AGC</td>
</tr>
<tr>
<td>R3</td>
<td>Microphone biasing resistor</td>
<td>Provides biasing for microphone operation</td>
</tr>
<tr>
<td>C1</td>
<td>Microphone DC-blocking capacitor, Low frequency cutoff</td>
<td>Decouples microphone bias from chip. Provides single-pole low frequency cutoff</td>
</tr>
<tr>
<td>C2</td>
<td>Attack/Release time constant</td>
<td>Sets attack/release time for AGC</td>
</tr>
<tr>
<td>C3</td>
<td>Low frequency cutoff capacitor</td>
<td>Provides additional pole for low frequency cutoff</td>
</tr>
<tr>
<td>C4</td>
<td>Microphone power supply decoupling network</td>
<td>Reduces power supply noise</td>
</tr>
<tr>
<td>C5</td>
<td>Noise reduction</td>
<td>Reduces input noise</td>
</tr>
</tbody>
</table>