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A Ternary Schmitt Trigger

K. RAMKUMAR AND K. NAGARAJ

***Abstract*—A new ternary circuit, namely, a ternary Schmitt trigger, is presented. This novel circuit which is based on the well-known lambda diode, is suitable for integration using CMOS technology. The circuit has been simulated using the SPICE 2G Program. The results of the simulation are presented. The circuit offers a high degree of design flexibility. This circuit is expected to be a very useful functional block in the processing of ternary and pseudoternary signals.**

Introduction

Multilevel logic has a distinct advantage over binary logic in terms of functional density. Several functional circuits for multilevel logic systems have been developed. Some examples of CMOS ternary logic circuits can be found in [1]–[4]. This paper presents the study of a new ternary circuit, namely, a ternary schmitt trigger. A ternary Schmitt trigger is expected to be a useful functional block in ternary signal processing. An example of such an application is a ternary line receiver which has to be used to shape ternary signals, received over a line, into proper ternary logic levels.

Manuscript received June 21, 1984; revised December 4, 1984.

K. Rajkumar is with the Department of Electrical Communication Engineering, Indian Institute of Science, Bangalore 560 012, India.
K. Nagaraj is with Digital Communication Group, Transmission R & D, Indian Telephone Industries, Ltd., Bangalore 560 016, India.

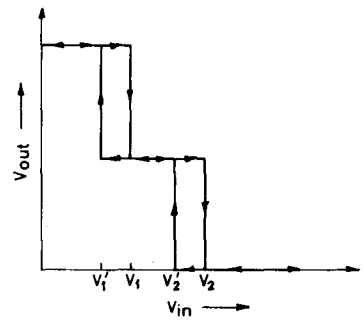

Fig. 1. Transfer characteristics of a ternary Schmitt trigger.

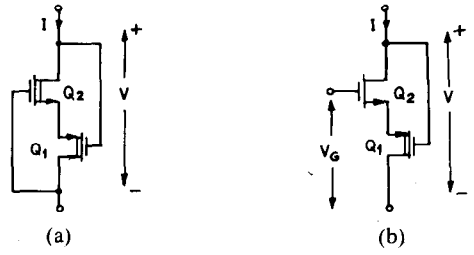

Fig. 2. (a) Lambda diode. (b) Lambda transistor.

The transfer characteristic that is required of a ternary Schmitt trigger (inverting type) is shown in Fig. 1. It is seen that this characteristic has two hysteresis loops, one bounded by the two threshold voltages V_1 and V_1' and the second bounded by the threshold voltages V_2 and V_2'. Such a transfer characteristic can probably be realized using two separate binary Schmitt triggers and combining their outputs suitably to obtain a ternary output. However, this paper describes a simpler and a more elegant circuit for realizing this function. This circuit uses only six devices and also offers a high degree of design flexibility.

Description of the Circuit

This Schmitt trigger circuit is based on the lambda diode, which is a voltage-controlled two-terminal negative resistance device made up of a pair of complementary depletion type FET's. Fig. 2(a) shows the circuit schematic of a MOS lambda diode (A similar lambda diode can be realized using two complementary junction FET's.) Its operation is briefly as follows. When a voltage V is applied across the diode, the current through the device increases until V nearly equals the cutoff voltage of either of the FET's. The current is then at its peak value, I_P and the corresponding voltage level is called the peak voltage, V_P. If V is increased further, the current decreases until V equals the sum of the cut off voltages of the two FET's. Beyond this valley voltage V_C, both the FET's are turned off, and the current through the diode consists only of the leakage current. The characteristics of a lambda diode have been studied extensively [5]–[7]. In the present application, the structure of the lambda diode is altered slightly by disconnecting the gate of one of the two transistors and using it as an independent control terminal, as shown in Fig. 2(b). The modified structure may be termed a lambda transistor

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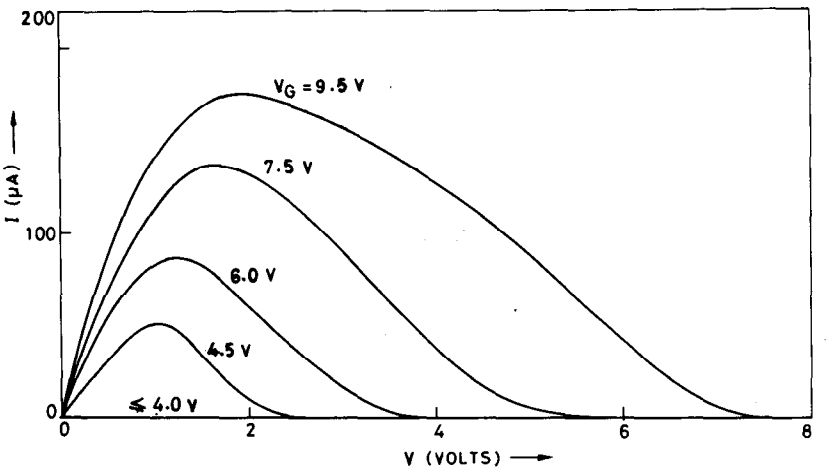

Fig. 3. Simulated $V-I$ characteristics of the lambda transistor.

This lambda transistor is simpler than one proposed earlier [5] which used three FET's.) The structure shown in Fig. 2(b) may be called an n-type lambda transistor. A p-type lambda transistor can be obtained by using the gate of Q_1 as the control terminal. The lambda transistor shown in Fig. 2(b) has been simulated on a computer using the SPICE 2G program and its $V-I$ characteristics obtained for various values of V_G. Some typical computed characteristics are shown in Fig. 3. In this simulation the threshold voltages of Q_1 and Q_2 were assigned values of 2 and 4 V, respectively. Other device parameters used in the simulation are listed in Appendix A. It is seen from Fig. 3 that by varying V_G, the $V-I$ characteristics can be altered significantly. The peak current I_P, the peak voltage V_P, and the valley voltage V_C are all functions of V_G. It is seen that as V_G is decreased, V_P, I_P, and V_C all decrease. In fact, below a certain value of V_G, the enhancement device Q_2 is cut off and consequently the $V-I$ characteristic of the lambda transistor disappears. The parameters V_P and I_P can be expressed in terms of the device parameters by empirical relations which are given in Appendix B. The valley voltage V_C can be expressed as follows [7]:

$$V_C \simeq V_G - V_{T2} + V_{T1}. \tag{1}$$

The feature of being able to alter the $V-I$ characteristics of the lambda transistor by varying V_G has been exploited here to conceive of a ternary schmitt trigger which is described in detail below.

The circuit schematic of the proposed schmitt trigger is shown in Fig. 4. It comprises an n-type lambda transistor ($Q_1 - Q_2$), a p-type lambda transistor ($Q_3 - Q_4$) and two equal resistors R_1 and R_2. During this discussion, the lambda transistor $Q_1 - Q_2$ and the resistor parallel to it will be designated as one single device D_1, whereas the other lambda transistor with its resistor will be designated as D_2. The behavior of this structure can be analysed by considering D_1 as the active stage and D_2 as the load stage and superimposing the $V-I$ characteristics of the two devices over one another. If the input voltage V_{IN} is varied, it affects the $V-I$ characteristics of both D_1 and D_2 and consequently affects the operating point of the composite structure. The composite structure normally has three stable states of operation. By altering the $V-I$ characteristics through the variation of V_{IN}, transitions of the structure from one stable state to another may be achieved.

To describe the operation of the circuit, we assume that initially the input voltage V_{IN} is zero. Consequently the lambda transistor $Q_1 - Q_2$ is totally cut off and the $V-I$ characteristic of D_1 is essentially that of the resistor R_1, as shown in Fig. 5(a). The

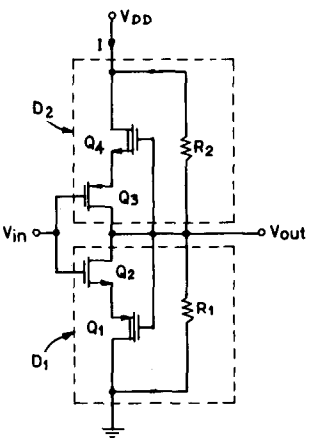

Fig. 4. Circuit schematic of the ternary Schmitt trigger.

point "C" at which the $V-I$ characteristics of D_1 and D_2 intersect is the operating point of the circuit. The output voltage V_{OUT} in this state is close to V_{DD} and corresponds to logic "2". If now V_{IN} is increased, the $V-I$ characteristic of D_2 moves downwards, whereas the $V-I$ characteristic of D_1 initially continues to be that of R_1. When V_{IN} reaches a certain value V_1 the intersection point "C" disappears (as seen in Fig. 5(a)). Consequently the circuit makes a transition to the next possible stable operating point "B". The output voltage V_{OUT} in this state is equal to $V_{DD}/2$ and thus corresponds to logic "1". If V_{IN} is increased further, the downward shift of the $V-I$ characteristic of D_2 continues further, whereas the $V-I$ characteristic of D_1 starts shifting upwards. When V_{IN} reaches a value V_2, the intersection point 'B' also disappears (as in Fig. 5(b)). It may be realised that this occurs when the valley voltage of the lambda transistor $Q_1 - Q_2$ becomes equal to $V_{DD}/2$. The circuit now makes a transition to the only available stable state "A". The output voltage V_{OUT} in this state is close to zero and thus corresponds to logic "⊙".

IF V_{IN} is now decreased, a sequence of events very similar to the one described above takes place, but with the roles of D_1 and D_2 interchanged. When V_{IN} is lowered to a value V_2', the intersection at "A" vanishes (as shown in Fig. 5(c)) and the circuit switches to state "B". When V_{IN} reaches a still lower value V_1', the intersection at "B" also vanishes (as shown in Fig. 5(d)), thus forcing the circuit to switch to state "C".

It is evident from the above discussion that in both the transitions, between states "A" and "B" and states "B" and

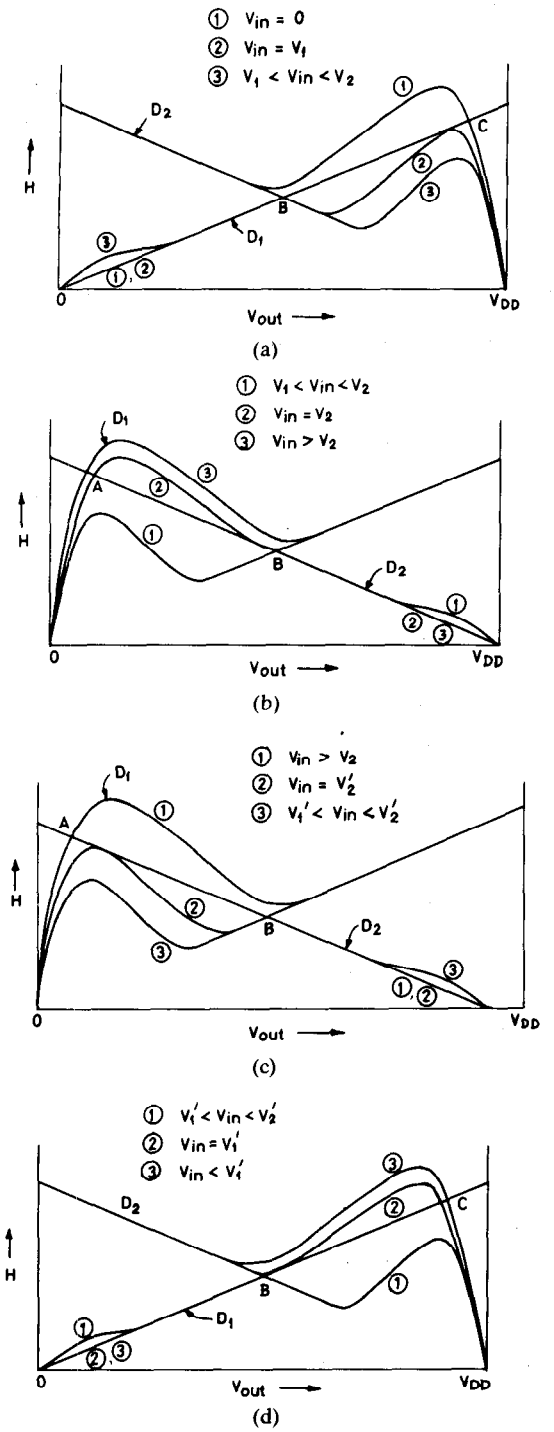

Fig. 5. $V-I$ characteristics of D_1 and D_2 under various input conditions. (a) V_{IN} increasing, in the vicinity of V_1. (b) V_{IN} increasing, in the vicinity of V_2. (c) V_{IN} decreasing, in the vicinity of V_2'. (d) V_{IN} decreasing, in the vicinity of V_1'.

"C", hysteresis is involved. Thus the circuit satisfies the requirements of a ternary Schmitt trigger.

A ternary Schmitt trigger of this type has been simulated extensively using the SPICE 2G program. Fig. 6 shows a typical simulated transfer characteristic. The important parameters used in this simulation are (1) V_{T1} (threshold voltage of Q_1) = 2 V, (2) V_{T2} (threshold voltage of Q_2) = 5 V, (3) V_{T3} (threshold voltage of Q_3) = −5 V, (4) V_{T4} (threshold voltage of Q_4) = −2 V, (5) $R_1 = R_2 = 65$ kΩ and (6) $V_{DD} = 12$ V. The other parameters of the MOS transistors are given in Appendix A.

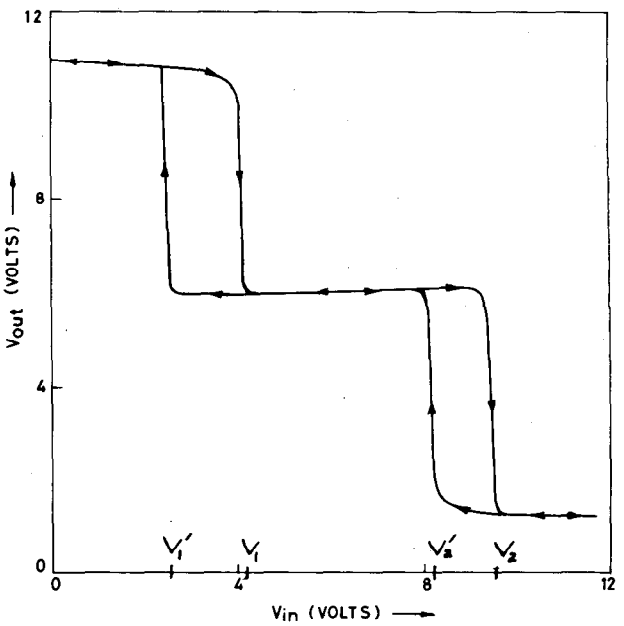

Fig. 6. Simulated transfer characteristics of the ternary Schmitt trigger.

Design Considerations

In this section we discuss how the four threshold voltages governing the operation of the Schmitt trigger can be controlled.

As stated earlier, the threshold voltage V_2 occurs when the valley voltage of the lambda transistor $Q_1 - Q_2$ becomes equal to $V_{DD}/2$. Thus using (3), the expression for V_2 can be written as

$$V_2 \simeq V_{DD}/2 + V_{T2} - V_{T1}. \tag{4}$$

It is seen from (4) that V_2 is a function of the threshold voltages of Q_1 and Q_2 and is practically independent of the other circuit parameters. In a similar way, the expression for V_1' can be written as

$$V_1' \simeq V_{DD}/2 + V_{T3} + |V_{T4}|. \tag{5}$$

It is clear from the above discussion that the threshold voltages V_2 and V_1' can be set by adjusting the threshold voltages of the transistors. For best results, V_{T1} and $|V_{T4}|$ must be made small, so that the output voltage levels in the states "A" and "C" are close to zero and V_{DD}, respectively. (It is evident from (B−2) in Appendix B that the peak voltage of the lambda transistor $Q_1 - Q_2$ is always smaller than V_{T1}. Similarly the peak voltage of the lambda transistor $Q_3 - Q_4$ would always be larger than $V_{DD} - |V_{T4}|$). Having thus fixed V_{T1} and V_{T4}, V_1' and V_2 can be set by adjusting V_{T2} and V_{T3}, respectively.

The threshold voltage V_1 is a function of β_3 and β_4. Referring to Fig. 5(a), if β_3 and β_4 are increased, the $V-I$ characteristic of D_2 (for a given V_{IN}) shifts upwards in relation to that of D_1 (The dependence of the $V-I$ characteristic on the conductance constants is given by (B-1) in Appendix B). This evidently results in an increase in V_1. Similarly the threshold voltage V_2' is affected by β_1 and β_2.

The dependence of V_1 on β_3 and β_4 has been simulated. The values of the other parameters are the same as stated earlier. The simulated variation is shown in Fig. 7. The variations of V_1', V_2, and V_2' are also plotted, to show that they are virtually independent of β_3 and β_4. The threshold voltage V_2' would exhibit a similar dependence on β_1 and β_2.

It is evident from the above discussion that the four threshold voltages governing the operation of the Schmitt trigger can be set

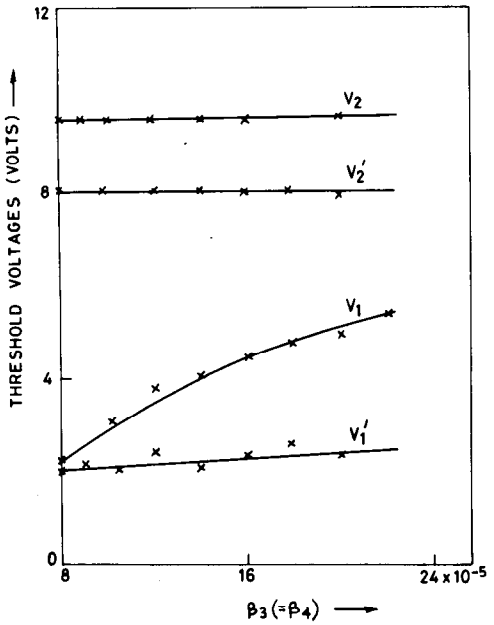

Fig. 7. Dependence of the threshold voltages on β_3 and β_4.

independently of each other by a proper selection of the threshold voltages and the geometries (which determine the conductance constants) of the transistors. Thus there is considerable flexibility in the design of the Schmitt trigger.

The dependence of the threshold voltages on the value of R_1 and R_2 has also been studied. When the value of R_1 and R_2 was increased (decreased) from 65 to 75 kΩ (55 kΩ), with the other parameter unchanged, V_1 was found to increase (decrease) by about 0.4 V whereas V_2' decreased (increased) by about 0.4 V. This dependence is to be expected, because variations in the value of R_1 and R_2 result in vertical shifts in the $V-I$ characteristics of D_1 and D_2. On the other hand it was found that as long as R_1 and R_2 are equal, the other two threshold voltages V_1' and V_2 are virtually independent of the value of R_1 and R_2.

This ternary Schmitt trigger can be integrated using CMOS technology. The threshold voltages of the transistors can be set to the desired values using ion-implantation, which enables the realisation of both enhancement and depletion MOS transistors with precisely controlled threshold voltages [8], [9]. The resistors can be formed with polysilicon [10]–[12]. Again, the values of the resistors can be adjusted using ion-implantation [11], [12]. By using double polysilicon technology, the resistors can be formed over the transistors [10]–[12], thus resulting in a saving in chip area. Alternatively, an all-MOS realization can be obtained by using two MOS transistors to perform the function of the resistors. (It is well known that an MOS transistor with its drain and gate terminals shorted together, closely simulates a resistor.)

Conclusion

A new ternary circuit, namely, a ternary Schmitt trigger has been described in this paper. This circuit is based on the lambda transistor, which is obtained by modifying the structure of the well-known lambda diode. The circuit has been simulated extensively using the SPICE 2G program. The circuit offers a high degree of design flexibility. It can be integrated using CMOS technology. The ternary Schmitt trigger is expected to be a useful functional block in ternary signal processing. It may also find application in binary transmission systems which employ pseudo-ternary coding.

Appendix A
Parameters used in the SPICE 2G Simulation

1) Conductance constant of all the four transistors ($\beta_1 = \beta_2 = \beta_3 = \beta_4$) $= 13 \times 10^{-5}$ A/V^2 (The conductance constant β of an MOS transistor equal to $\mu C_0(W/L)$, where μ is the mobility of carriers, C_0 is the gate oxide capacitance per unit area, and W/L is the width-by-length ratio of the channel).

2) Channel length modulation factor λ equal to 0.01 V^{-1} for all four transistors.

3) Body effect factor γ equal to 0.2 V$^{1/2}$ for all four transistors.

Appendix B

The peak current I_P and the peak voltage V_P of a lambda diode are given by the following empirical relations:

$$I_P = I_n(\max)\left[1 - \exp - \frac{I_P(\max)}{I_n(\max)}\right] \qquad (B-1)$$

$$V_P = V_{Tn}\left[1 - \exp - \frac{V_{TP}}{V_{Tn}}\right] \qquad (B-2)$$

where $I_n(\max)$ and $I_P(\max)$ are the maximum currents carried by the n-channel and the p-channel transistors respectively. $I_n(\max)$ and $I_P(\max)$ are directly proportional to the conductance constants of the transistors. V_{Tn} and V_{TP} are the threshold voltages of the n-channel and p-channel transistors, respectively.

Acknowledgment

The authors wish to thank Paul Anthony of the Department of Electrical Communication Engineering, Indian Institute of Science, Bangalore, India, for his help in the simulation work. The authors are also grateful to the referees for their valuable suggestions.

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