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Abstract

The binary logic system formed by ternary logic circuit has error detecting and error correcting function. Three valued-polar code and ternary logic error detecting and error correcting circuit for the data transmission system are presented in this paper. This data transmission system has powerful capability to detect and correct error, so the reliability of the data transmission improves greatly and the error rate reduces rapidly.

I Introduction

The task of a data transmission system is to transfer digital signals. The main problems are efficiency and reliability, i.e. a higher signal rate and a lower error probability. However they are always contradictory. Figure 1 shows a simple data transmission system. Noise causes the error of output signals. Usually, there are two types of errors. One is the random error caused by Gaussian noise, the other is burst error caused by pulse

noise. Therefore, the coding for error detecting and error correcting is required to improve reliability.

The Data rate of prime codes is higher than that of error detecting and error correcting codes, but its error probability is also higher than that of the later. Normally, [2] a parity-check code with minimum distance D can detect E errors when $D \geq E+1$, and can correct T errors when $D \geq 2T+1$. A convolutional code with $L-1$ bits can correct one error. But encoder and decoder for convolutional codes are rather complex.

There are many kinds of three-levels codes, for example, AMI, B6ZS, HDDBS etc. which are applied widely for digital communications. Their capability for detecting errors and correcting errors is more powerful. However, their error probability is greater than that of binary codes. Suppose that the transmission digital data sequences $\{a_n\}$ have $M-1$ levels and each probability of them is identical. If signal levels are $\pm d, \pm 3d, \dots, \pm(M-1)d$ and threshold levels of receiver are $0, \pm 2d, \dots, \pm(M-2)d$, then error probability in baseband transmission is [6]

$$P_e = (1 - \frac{1}{M}) \operatorname{erfc} \left[\frac{A}{\sqrt{2(M-1)}\sigma} \right] \quad (1)$$

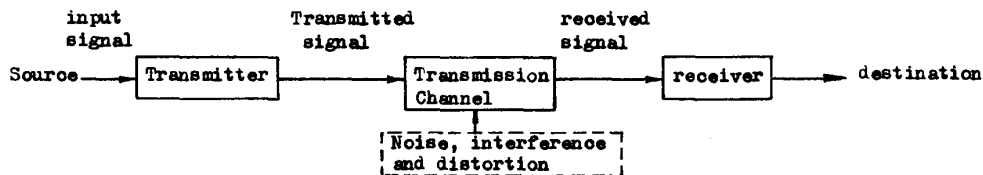


Figure 1

where A - the amplitude of input signal

σ - rms value of noise

and the transmission channel has an ideal frequency characteristic.

When M is equal to 2 the error probability has minimum value.

However, in practice some compromise between conflicting consideration of reliability, efficiency, and equipment complexity were made. So a new three valued-polar code and ternary logic circuit for error detection and error correction are presented in this paper, they have high reliability and efficiency as well as simple circuit configuration.

II Three valued-polar code

Let X, Y, F be three valued logic variable over Q , and $Q = \{-1, 0, 1\}$ i.e. symmetric ternary logic system (ST system) is used in this paper. To specify problems, logic variable fundamental operations of ST system are defined as follows [4].

Definition 1: complement operator "-" is defined

$$\bar{X} = -X \quad (2)$$

From equation (2), it is known that $\bar{\bar{1}}$ equals to -1 , i.e., $\bar{\bar{1}} = -1$

Table 1 is truth table of complement operator.

Table 1

X	\bar{X}
$\bar{1}$	1
0	0
1	$\bar{1}$

Table 2

X	Y	XAY
$\bar{1}$	$\bar{1}$	$\bar{1}$
$\bar{1}$	0	0
$\bar{1}$	1	0
0	$\bar{1}$	0
0	0	0
0	1	0
1	$\bar{1}$	0
1	0	0
1	1	1

Definition 2: AND operator "." or "^" is defined

$$F = X \wedge Y = \begin{cases} 1 & \text{if } X, Y \in \{1\} \\ \bar{1} & \text{if } X, Y \in \{-1\} \\ 0 & \text{if } X, Y \in \{1\} \text{ OR } X, Y \in \{-1\} \end{cases} \quad (3)$$

Truth table of AND is shown in table 2.

Definition 3: OR operator "V" is defined

$$F = X \vee Y = \begin{cases} 1 & \text{if } X, Y \in \{0, 1\} \\ \bar{1} & \text{if } X, Y \in \{-1, 0\} \\ 0 & \text{if } X, Y \in \{0, 1\} \text{ OR } X, Y \in \{-1, 0\} \end{cases} \quad (4)$$

Truth table of OR is given in Table 3.

Table 3

X	Y	XVY
$\bar{1}$	$\bar{1}$	$\bar{1}$
$\bar{1}$	0	$\bar{1}$
$\bar{1}$	1	0
0	$\bar{1}$	$\bar{1}$
0	0	0
0	1	1
1	$\bar{1}$	0
1	0	1
1	1	1

In [3] a two rail 2-of-3 valued system was proposed and indicated that an error caused by any fault is a correctable error or a detectable error.

In this paper, three valued-polar code is proved that it has an error detecting and error correcting property, and can be used to detect error and correct error.

Definition 4: If a pair of mutual complement signals are transmitted through the channel (see fig.1), the data transmission system is referred to as two-rail transmission system.

Definition 5: In two-rail transmission system, there are three signals: " $\bar{1}$ ", "0" and "1". " $\bar{1}$ " and "1" are defined as valid signals and "0" is defined as a redundant signal. Such digital signal sequence is called three valued-polar code (abbr, TP code).

In order that TP code is applied to the traditional binary digital data transmission system, signal "1" is called code 1 and signal " $\bar{1}$ " is called code 0. In two-rail transmission system delivering TP code, the signals delivered by source are normally a pair of mutual complement signals and the signals input to receiver are also a pair of mutual complement signals (see table 4: $X=\bar{1}, Y=1$ in the row 3 and $X=1, Y=\bar{1}$ in the row 7).

When digital data are delivered along the channel, the transmission error are caused by noise

Table 4

N	X	Y	F	D*	Z*	L*	Comment
1	$\bar{1}$	$\bar{1}$	0		0	1	Error is detected, request to repeat transmission
2	$\bar{1}$	0	$\bar{1}$	0	1	0	Error caused by negative CMI* is corrected
3	$\bar{1}$	1	$\bar{1}$	0	1	0	Valid signal " $\bar{1}$ "
4	0	$\bar{1}$	1	1	1	0	Error caused by negative CMI is corrected
5	0	0	0		0	1	Error is detected, request to repeat transmission
6	0	1	$\bar{1}$	0	1	0	Error caused by positive CMI is corrected
7	1	$\bar{1}$	1	1	1	0	Valid signal "1"
8	1	0	1	1	1	0	Error caused by positive CMI is corrected
9	1	1	0		0	1	Error is detected, request to repeat transmission

*Where CMI - common mode interference

D - output signal of error detecting and error correcting circuit

Z - output signal of detecting circuit

L - request signal for repeating, and L = Z

disturbance or interference. Nine possible cases are shown in table 4.

Definition 6: Comparative operator " Δ " is defined

$$X\Delta Y = \begin{cases} \bar{1} & \text{if } X < Y \\ 1 & \text{if } X > Y \\ 0 & \text{if } X = Y \end{cases} \quad (5)$$

where $X, Y \in \{\bar{1}, 0, 1\}$ are symmetrical three valued logic variable. If the logic variable X, Y are regarded as ternary number, then the relation of these figures is $\bar{1} < 0 < 1$. Therefore the definition 6 is obviously correct. Truth table of comparative operation is given in table 5. Its logic symbol is shown in figure 2.

Table 5

X	Y	$X\Delta Y$
$\bar{1}$	$\bar{1}$	0
$\bar{1}$	0	$\bar{1}$
$\bar{1}$	1	$\bar{1}$
0	$\bar{1}$	1
0	0	0
0	1	$\bar{1}$
1	$\bar{1}$	1
1	0	1
1	1	0

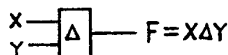


Figure 2

Definition 7: A circuit for ternary logic comparative operation is referred to as a correction gate.

Theorem: In data transmission system for delivering

three valued-polar code, the correction gate has error detecting and error correcting properties.

Proof: The function table of comparative gate consists of the column 2,3,4 in table 4. the row 3, 7 in table 4 show the normal status. In the row 1, 5,9, the outputs in the correction gate are "0", and it indicates that the delivered digital signals suffered interference, thus the valid signals (i.e. $X=\bar{1}, Y=1$ or $X=1, Y=\bar{1}$) change a redundant signal. It is proved that correction gate can detect three kinds of errors in the row 1,5 and 9 of the table 4. In the row 2, and 6, though the delivered signals suffered interference, the correction gate could correctly decode 0 code (i.e. the signal " $\bar{1}$ " of ternary logic). Similarly, the correction gate could translate these distorted signals as $X Y=0 \bar{1}$ and $1 0$ (see the row 4,8) into the corrective valid signal, i.e. code 1. Q.E.D.

III Design of Error Detecting and Error correcting by ternary Logic Corrective Circuit

If the data transmission system is totally ternary logic system, then only a correction gate can perform error detecting and error correcting function. By applying the concept presented in this paper the reliability of the traditional binary data transmission systems will improve and the error probability of them will reduce.

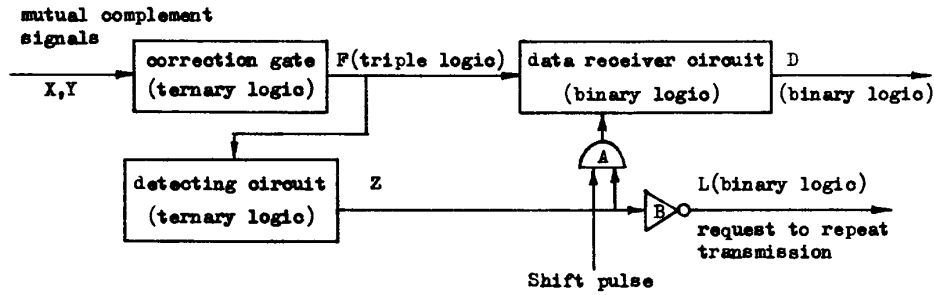


Figure 3

The error detecting and error correcting circuit of the ternary logic is shown in figure 3. Some major components in figure 3 are specified as follows. The correction gate performs error detecting and error correcting function as indicated above. This circuit can transfer the possible nine digital signals into two valid signals (i.e. $F=\bar{1}$ or 1, see table 4), and into a redundant signal (i.e. $F=0$, see table 4). The data receiver circuit is essentially a shift register operating in the mode of serial input and parallel output. Its shift pulse is controlled by the error detecting circuit. When the correction gate input signal is ternary logic "1" (or " $\bar{1}$ "), the error detecting circuit output is binary logic 1. In that condition, gate A is open and the shift register receives this ternary logic "1" (or " $\bar{1}$ ") by shift pulse. When correction gate input is a ternary logic "0", the detecting circuit output is binary 0, then the gate A is closed, and the redundant signal "0" is rejected by it. However, the error detecting circuit output 0 is inverted by gate B, and output L of the gate B is 1. This signal 1 is delivered oppositely to source and make a request to retransmit the previously detected error signal once again.

The circuit of the correction gate is designed as follows. According to the table 4 a symmetric three valued logic map (i.e. ST map, see figure 4) [4] is drawn, then the rule of simplification ST map is used to simplify it, and thus the simplest logic representation can be written as follows:

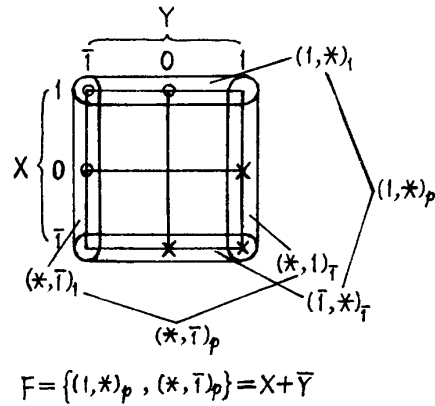


Figure 4

$$F = X + \bar{Y} \quad (5)$$

According to the definition 1,3, it is easily derived that the correction gate consists of ternary logic inverter and a ternary logic OR gate as figure 5. Using two MC14007 and several resistors can form a correction gate figure 6.

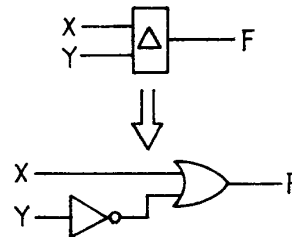


Figure 5

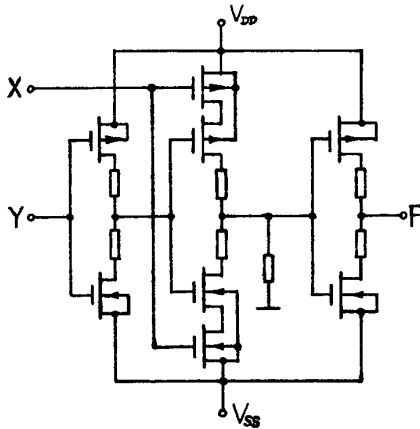


Figure 6

The error detecting circuit of the ternary logic is designed according to the principle as described above. Its logic representation Z is (from table 6)

$$Z = \begin{cases} 1 & \text{if } FE \{\bar{1}, 1\} \\ 0 & \text{if } FE \{0\} \end{cases} \quad (6)$$

The circuit as shown in figure 7 consists of one MC14007, two diodes and five resistors.

In figure 3, if each part of this circuit is supplied by the same voltage power, the input X, Y of the collection gate are binary valued, and the output F of it (i.e. the input of the data receiver and the error detecting circuit) is three valued. The output D or Z of the data receiver or

Table 6

F	Z
$\bar{1}$	1
0	0
1	1

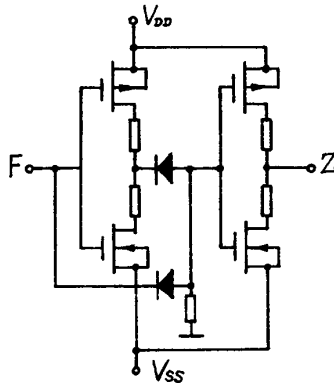


Figure 7

the error detecting circuit are all binary valued. Therefore, the error detecting and error correcting circuit in figure 3 can be compiled in an integrated circuit. This integrated circuit is called error detecting and error correcting gate (EDC gate).

Property 1: EDC gate is a compatible monolithic integrated circuit, so in the traditional binary digital transmission system (but the transmission signal must be a pair of mutual complement signals), the EDC can be used as error detecting and error correcting.

Property 2: EDC can eliminate the interference not only from random error but also from burst error.

The traditional circuit performs the error detecting and error correcting function by various code using encoding technique. The capability of this circuit depends upon the encoding and decoding methods. The properties of the random error and the burst error are different, hence the code to eliminate random error is generally useless to the burst error, and vice versa. The EDC gate performs the error detecting and error correcting function by detecting and correcting every bit, so the capability of error detecting and error correcting is independent on the cause for producing errors.

Property 3: In the data transmission system with EDC gate and delivering TP code, the transmission efficiency is highest (no redundant bits), the capability of error detecting and error correcting is more powerful, and the costs is cheaper (because of the simple circuit configuration of this data transmission system).

IV Conclusion

A microcomputer data acquisition system designed by the author, by utilizing the theory presented in this paper is working perfectly. In this system, TP code is used in channel, and EDC circuit is adopted in channel unit. Its operational condition has proved that this data transmission system has very powerful capability against interference (especially powerful common

interference) in severe circumstances, and the EDC circuit worths a practical value in data transmission system.

In summary, the conclusion will be obtained as follows:

1. The comparative operation and the correction gate of ternary logic presented in this paper have a good capability of error detecting and error correcting.

2. TP code presented according to ternary logic theory has a good property of easily detecting and correcting errors.

3. The EDC circuit has several good property: powerful capability of error detecting and error correcting, simple circuit configuration and very cheap cost.

References

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