A Novel Ternary Switching Element Using CMOS Recharge Semi Floating-Gate Devices

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Abstract

In this paper we present a novel voltage mode non-inverting CMOS Semi Floating-Gate(SFG) Ternary Switching Element. The design is applicable for reconstructing or refreshing ternary logic signals. The switching points are tuned using capacitive division. A preliminary simulation results from Cadence Spectre with AMS 0.35µm process parameters c35b4 is included.

1 Introduction

Multiple-valued logic has in the last few decades been proposed as a possible alternative to binary logic. Whereas binary logic is limited to only two states, "true" and "false", multiple-valued logic (MVL) replaces these with finitely or infinitely numbers of values.

The history of Multi-valued Logic as a separate object began in the early 1920 by a polish philosopher Lukasiewicz [1]. His intention was to introduce a third additional truth-value for "possible". The outcome of this investigation is known as the Lukasiewicz systems. Parallel to the approach of Lukasiewicz, the American mathematician Emil Post [2], introduced the idea of an additional truth degrees, and used this approach to solve the problems of the represent ability of functions, also known as the Post Algebra.

Ternary logic

Ternary logic has three logic states, "0","1" and "2", and the optimum radix of a fractional number is found to be the natural logarithm (e). Ternary logic uses number representation with radix=3, compared to binary logic witch uses radix=2, hence the most economical integer radix which is the closest to the natural logarithm e, is the number 3 [3]. This special property of base 3, inspired the early computer designers to build a ternary computer.

The first approach to build a MV-computer with ternary architecture was in the early 50th. in the USA. The earliest published discussion appears in the 1950 book *High-Speed Computing Devices*, a survey of computer technologies compiler on the behalf of the U.S Navy, by the staff of Engineering Research Associates [4]. But the first working ternary computer was built in Russia at the Moscow State University in 1958. The computer was design by Nikolai P. Brusentow and his colleagues and they named it *Setun*, for a river that flows near the university campus [5]. From 1958 to 1965 some 50 machines where built.

Floating Gate (FG) Transistors

The multiple-input FG transistors can be used to simplify the design of multiple-valued logic [6]. The initial charge on the floating-gates may vary significantly and therefore impose a very severe inaccuracy unless we apply some form of initialization. Some work on floating-gate reset strategies have been presented [7], [8].

Recharge Semi-Floating Gate (RSFG) Transistors

By recharging of the semi-floating-gate (SFG) we do not only avoid the problems linked to programming or initializing of the floating gates, but we convert the non-volatile floating gates to semi-floating-gates. The control of the actual floating gate charges in terms of predictable long term charge restoration becomes easier. The SFG is not influenced by a random FG charge distortion due to a periodic or frequent charge restoration or reset. The recharge of the SFGs is accomplished by a local recharge transistor or a pass gate temporarily connecting the output to the floating gate of a gate [9].

2 The Recharge Semi Floating-Gate (RSFG) Ternary Switching Element

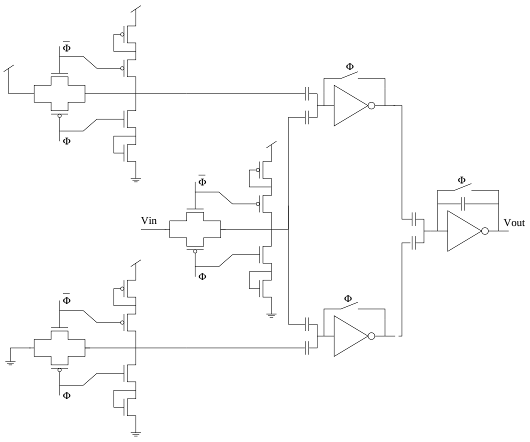

Figure 1. *Schematic diagram for ternary element. The design comprise three Semi Floating-Gate(SFG) AutoZero blocks, two digital SFG inverters and one analog SFG inverter at the output.*

The circuit in figure 1 shows a novel voltage mode ternary switching element. The design uses three AutoZero circuits, two Semi-Floating Gate(SFG) threshold elements also called a MVL SFG Down Literal Circuit [10], and a MVL SFG inverter [10]. This application is suitable to refresh or reconstruct ternary voltage mode signals.

Figure 2 shows the output signal of the circuit versus the input signal. The dotted line is the input signal. As we notice the output signal is converging to three logic levels, 0.2 Volt, 1 Volt and 1.8 Volt. It is also a valid MVL recharge signal. As we notice, in the recharge periods, the output is set to $V_{dd}/2$.

The SFG AutoZero Circuit (AZC)

A Recharge AutoZero circuit sets the input signal to $V_{dd}/2$ in the recharge periods and in the precharge periods the input signal is connected to the output thru the pass gate transistors, this to make sure the inputs to the next circuit will be a valid MVL recharge signal.

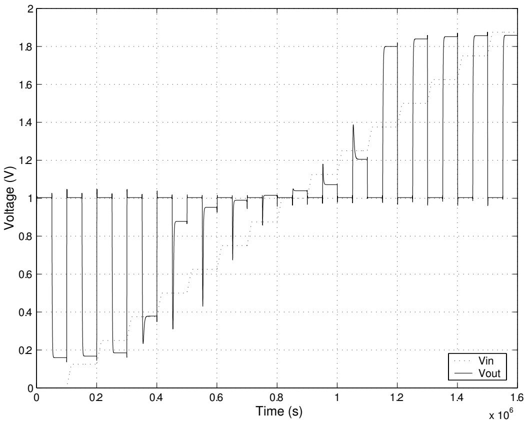

Figure 2. *Simulation over 16 clock periods showing output versus input voltage.*

The SFG Down Literal Circuit (DLC)

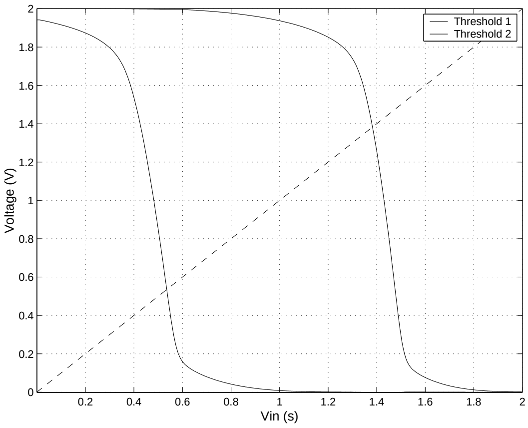

Figure 3. *Shows the thresholds for internal switching elements used for building the ternary element. The thresholds or switching points are determined by the capacitive division factors associated with each of the two switching elements.*

The threshold or the switching point is set by the MVL Recharge SFG DLC circuit [10] as shown in figure 3. A DLC can be seen as a digital inverter with two inputs. The dotted line in the figure is the input signal. The lower threshold or switching point is set by the output of the AutoZero Circuit(AZC) connected to the V_{ss} (gnd), and the upper switching point is set by the AZC connected to V_{dd} . The figure shows the internal switching nodes on the output of the DLC circuit. The switch point is determined by the capacitive division factor. k_i[1], V_{in} has weight $2C$ and $V_{Threshold}$ from the AutoZero Circuit, has weight C (C=$7.5fF$). By changing this factor we can fine tune the three logic levels.

The MVL SFG Inverter

The circuit at the output in figure 1, is a MVL recharge SFG Inverter [10] with two inputs. It will convert the output signal to a valid MVL recharge signal. The transfer characteristic of a MVL inverter is given by:

$$V_{out} = V_{dd} - V_{in} \tag{1}$$

Where V_{in} and V_{out} are the voltages on the input and output terminals, V_{dd} is the supply voltage.

The gain of MVL SFG inverter is determined by the capacitive division factor k_i. The feedback capacitor C_f should be $\sum C_{in}$, hence $2C$ to make sure EQ 1 is true, however C_f has to be slightly smaller than $2C$ due to the output conductance and the parasitic capacitance, C_{gd}.

The SFG Ternary Switching Element

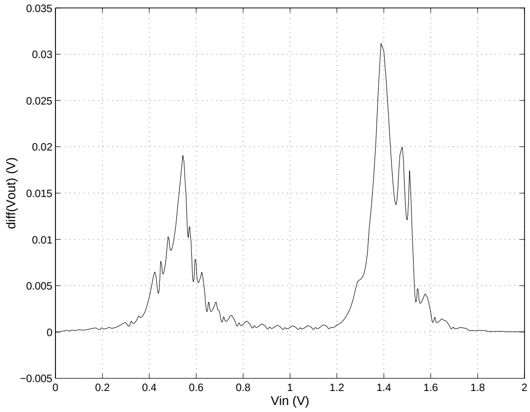

Figure 4. *A sweep of the derivative of the output signal V_{out}. Illustrates three stable regions around the three voltage levels 0.2V, 1V and 1.8V.*

If we analyse the circuit in figure 1, we find three stable regions given by dV_{out}/dV_{in}, this is shown in figure 4. These three regions are logic level '0' ($0 - 0.35V$), '1' ($0.8 - 1.2V$) and '2' ($1.65 - 2.0V$). This gives us, if the input is between $0 - 0.35V$ it will converge to logic level '0', if the input is $0.8 - 1.2V$ the output will be set to logic level '1' and if the input is in the region $1.65 - 2.0V$ the output will be set to logic level '2'. This is also shown in the figure 5 we can see how the output converge to the three logic levels.

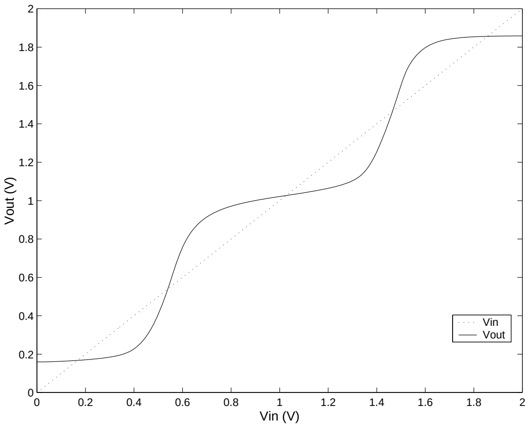

Figure 5. *A sweep of the output signal V_{out} versus the input signal V_{in}. This illustrates how valid input voltage are moved towards the output voltages 0.2, 1, 1.8V.*

A graphical illustrations of the noise margins are calculated in figur 6. The calculations of the noise margins of the simulated values given by the Cadence Spectre simulation, are obtained by using Matlab. This calculation confirms the noise margins of the ternary circuit. We can see three logic levels '0', '1' and '2' respectively $0.2V$, $1V$ and $1.8V$.

The switching region or noise is indicated using gray color, this is where the logic levels are undefined. As we can see we got better noise margins for the logic level '1', but this can be tuned by changing the value of the capacitors on the input of the DLC circuit.

Figure 7 shows the zero crossing point of the three logic levels, here is $V_{in} - V_{out}$ calculated using Matlab. The zero crossing point, which gives the three logic levels, is $0.18V$, $1.03V$ and $1.85V$ this is possible to fine tune by changing the capacative division factor k_i in the DLC circuit.

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[1] $k_i = C_i / \sum C_{In}$

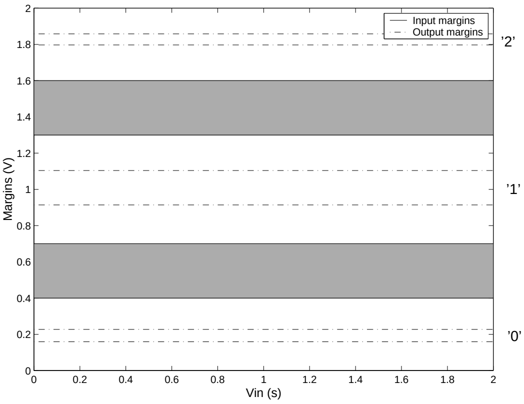

Figure 6. *Matlab calculations demonstrating the noisemargin diagram of the ternary element. The analysis is based on circuit simulations in Cadence Spectre. The three logical output values 0, 1, 2 is found as output voltages 0.2, 1, 1.8V respectively. The noise or switching region is indicated using gray color.*

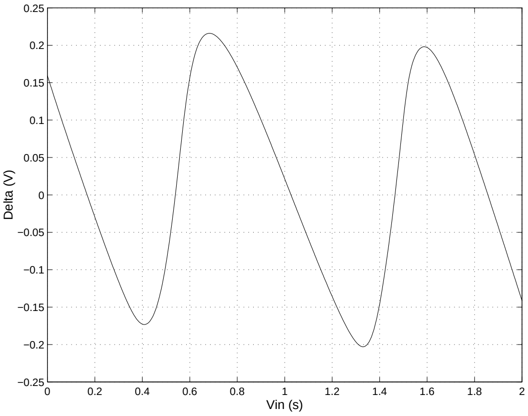

Figure 7. *The delta difference between output and input voltage ($V_{out} - V_{in}$). The results were obtained from simulation on schematic in Cadence Spectre using 10MHz precharge clock.*

3 Conclusion

In this paper we have presented a novel non-inverting voltage mode CMOS Ternary Switching Element. This element have shown good noise margins, and it is easy to fine tune, and it is well suitable to use in refreshing ternary signals in memory applications and also to reconstruct internal ternary logic signals. All simulation results are obtained from Cadence Spectre AMS 0.35 μm CMOS device parameters with 10MHz precharge clock frequency and $2V$ power supply. This application can easely be fabricated using a conventional CMOS process.

References

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