A Proposal for the Implementation of Ternary Digital Circuits

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Abstract - A nonclassical multi-valued logic based on Post algebra is presented. Besides the conventional Post's cyclic negation, this nonclassical logic algebra defines new operators that simplify the truth-table minimization techniques. An electronic implementation of this algebra for a 3-level logic is proposed. Electronics gates of Post negation and the new operators were designed and simulated using current mode circuits. These gates can be easily interconnected to form flip-flops, counters and other conventional digital gates in a true 3-level gate logic. ASICs with mixed analog/digital high-speed processing can benefit from this current processing ternary logic, which can be easily implemented in bipolar technology.

I. INTRODUCTION

After the development of multivalued logics by Post [1] and Lukasiewicz [2] in 1920, and the presentation of the concept of *Post algebra of order n* in 1942 by Rosenbloom [3], several attempts have been made to use this concept in computer science. An excellent review of the first developments of multivalued logics and its applications to electronics, including a few circuit implementations, was presented by Epstein in 1974 [4]. In the last 20 years, however, microelectronics technology has improved greatly and several circuits have been published using both CMOS and bipolar technology, with a great emphasis in I^2L technology [5]. In 1993 it was expected that the technological advances achieved over the last ten years would bring back the discussion on the commercial realization of multivalued circuits [6], and recently, new techniques have been presented [7].

This paper describes a new multivalued algebra that uses the Post's cyclic negation, the *AND* conjunction, and new operators which allow the development of simple algorithms for the synthesis and simplification of the logical functions.

An electronic implementation (using current processing techniques) of a ternary logic is also presented.

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II. DEFINITIONS AND NOTATION

The algebra contains a set of variables (*x,y, z,...*) which can assume *n* logic values from a set defined as $P = \{t_1, t_2, ..., t_n\}$, with $t_i > t_j$, if $i > j$. The unary cyclic rotation (Post's cyclic negation) is defined as:

$$\overline{t_i} = \begin{cases} i+1 \ , \ if \ i \neq n \\ 1 \ , \ if \ i = n \end{cases} \quad (1)$$

We also define a counterclockwise negation as:

$$\underline{t_i} = \begin{cases} i-1 \ , \ if \ i \neq 1 \\ n \ , \ if \ i = 1 \end{cases} \quad (2)$$

The binary conjunction *AND* (·), as in classical logic, is defined as:

$$t_i \bullet t_j = \min \{ t_i , t_j \} \quad (3)$$

It is possible to show that any multivalued function can be expressed in a canonic form based on these two operators (*NEGATION* and *AND*), and, thus, this logic is functionally complete [8].

For an *n*-valued logic, *(n -1)* operators are defined, as shown in Eq. (4). Although all operators OP_k are redundant (they can all be expressed in terms of the *AND* and the *NEGATION)*, they are important in the process of

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minimization/simplification of logical functions.

$$\overline{t_i \, . \, t_j} = \bar{t}_i \, OP_1 \, \bar{t}_j$$

$$\overline{\overline{t_i \, . \, t_j}} = \bar{\bar{t}}_i \, OP_1 \, \bar{\bar{t}}_j = \bar{t}_i \, OP_2 \, \bar{t}_j$$

$$\vdots$$

$$(n-1)\left\{ \begin{array}{c} \overline{\quad} \\ \vdots \\ \overline{\quad} \\ \overline{\quad} \end{array} \right. \qquad (4)$$

$$t_i \, . t_j = \ldots = \bar{t}_i \, OP_{n-1} \, \bar{t}_j$$

To simplify the notation in the ternary logic, we define 3 operators, α, β and γ, where α is the *AND* conjunction and β and γ are defined as follows:

$$\overline{x \; \alpha \; y} = \bar{x} \; \bar{\alpha} \; \bar{y} = \bar{x} \; \beta \; \bar{y}$$

$$\overline{x \; \beta \; y} = \bar{x} \; \bar{\beta} \; \bar{y} = \bar{x} \; \gamma \; \bar{y} \qquad (5)$$

$$\overline{x \; \gamma \; y} = \bar{x} \; \bar{\gamma} \; \bar{y} = \bar{x} \; \alpha \; \bar{y}$$

The truth tables for the β and γ operators with logic values *a*, *b* and *c* (*c*>*b*>*a*) are shown in Table I.

β operator		X		
		a	*b*	*c*
Y	*a*	*a*	*b*	*c*
	b	*b*	*b*	*b*
	c	*c*	*b*	*c*

γ operator		X		
		a	*b*	*c*
Y	*a*	*a*	*a*	*c*
	b	*a*	*b*	*c*
	c	*c*	*c*	*c*

Table I - Truth-tables of β and γ operators.

From the truth-tables one notices that the β operator is the *max{x,y}*, except for the cases where a value *(b)* appears operated with a higher value *(c)*. In this particular case, the value *(b)* dominates and the result of the operation is equal to *(b)*, which, in turn, is the *min{x,y}*.

The same type of inspection in the γ truth-table operator leads to the conclusion that γ is the *min{x,y}*, except for the case where a *(c)* is operated with a lower value. In these cases the *(c)* value dominates and the result is equal to the *max{x,y}*. These interpretations of relative maximum and minimum do not have any special logical meaning, but are very convenient for the design of electrical circuits that implement these operators β and γ.

For these operators, the distributive property is valid in the following cases:

$$x \; \alpha \; (y \; \beta \; z) = (x \; \alpha \; y) \; \beta \; (x \; \alpha \; z)$$

$$x \; \beta \; (y \; \gamma \; z) = (x \; \beta \; y) \; \gamma \; (x \; \beta \; z) \qquad (6)$$

$$x \; \gamma \; (y \; \alpha \; z) = (x \; \gamma \; y) \; \alpha \; (x \; \gamma \; z)$$

III. Synthesis of Functions

A basic algorithm for the synthesis of a two-variable function is presented. This algorithm does not minimize the logical function, but its simplicity is adequate to show how the synthesis can be realized. More sophisticated algorithms are needed if a minimization is required [8].

Let *F1* and *F2* be two ternary input functions (with logic values *a,b and c*) and *So* the desired output. In Table II all combinations of *F1* and *F2* are presented, and each cell of the desired output *So* assumes any of the three logic values, *a, b or c*. Two functions *K1* and *K2* must be written, so that their arguments can only be *(a,b)* and *(b,c)*, respectively. The output function *So* will be *So*=*K1* γ *K2*, if *K1* and *K2* are constructed with the following procedure:

a) *K1* - In all cells where *So*=*a*, one must transform (if necessary) the values of *F1* and *F2* in (*a*), by using negations. A β operation between each two pairs [*F1*,*F2*] is then performed. The function *K1* will be the α product of all these terms.

b) *K2* - In all cells where *So*≠*c*, the values of *F1* and *F2* must be transformed, using negations, in *(c)*. Then, a γ operation between each pair [*F1*,*F2*]is realized. *K2* will be expressed as the β operation between all these terms.

So		F1		
		a	*b*	*c*
F	*a*	*c*	*c*	*c*
	b	*c*	*a*	*c*
	c	*a*	*b*	*a*

Table II - Example of synthesis.

Thus, functions *K1*,*K2* and the output function *So* of Table II are given by:

$$K_1=[\underline{F_1}\,\beta\,\underline{F_2}]\,\alpha\,[F_1\,\beta\,\overline{F_2}]\,\alpha\,[\overline{F_1}\,\beta\,\overline{F_2}]$$
$$K_2=[\overline{F_1}\,\gamma\,\underline{F_2}]\,\beta\,[F_1\,\gamma\,\underline{F_2}]\,\beta\,[F_1\,\gamma\,F_2]\,\beta\,[\underline{F_1}\,\gamma\,\underline{F_2}] \qquad (7)$$
$$S_o = K_1\,\gamma\,K_2$$

IV. Electronic Realization

The interest for current mode circuits has increased in the last 5 years, with several developments made in this area. Current mode circuits can process analog signals at very high speeds and, since they are not complex, they became an attractive solution for ASICs analog circuitry.

The circuits designed for this ternary logic were developed using current mode techniques. These ternary logic circuits are compatible with the standard analog circuits design techniques used today; actually, some of the logical operators are implemented based on standard translinear circuits [9].

As defined previously (see Eq. 3), the α operator is the equivalent of the *AND* operator (minimum). Assuming that we have 3 current levels: *Ia*, *Ib* and *Ic*, with *Ic*>*Ib*>*Ia*,the translinear circuit presented in Fig. 1 realizes the desired function [9]. The output current I_{out} is equal to the minimum current available at the input. This can be easily verified by writing the translinear loop equation and solving for I_{out}. The quadratic equation presents two solutions: $I_{out}=Ix$ or $I_{out}=Iy$, and by simple inspection in the circuit one concludes that the current I_{out} will be the minimum of *{Ix,Iy}*. The string of transistors used to bias the base of Q2-Q3 is necessary to avoid problems when connecting this circuit with others. A simulation of the α operator is shown in Fig. 2.

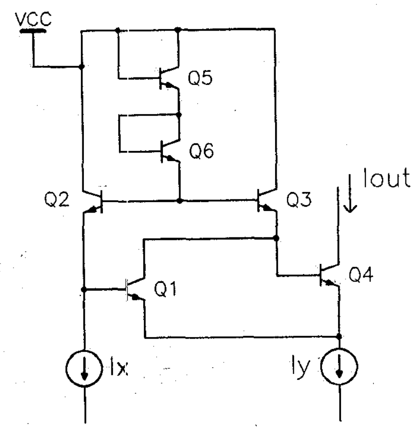

Fig.1 - Translinear circuit used to realize the α operator.

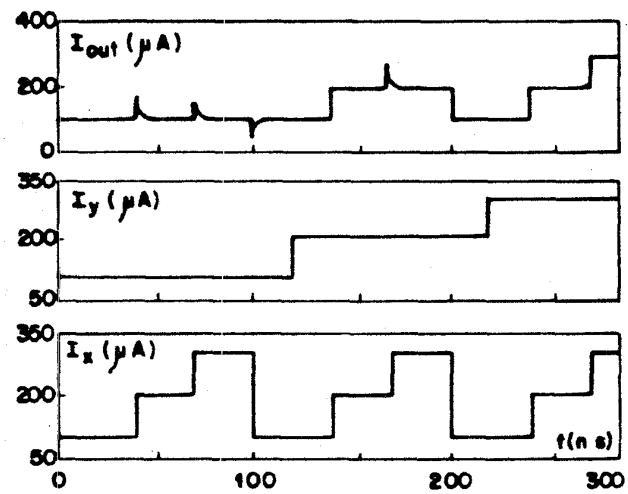

Fig. 2 - Results of PSPICE simulation of the α operator.

The Post negation and the counterclockwise negation circuits were designed using the same current inputs,*Ia*,*Ib* and *Ic*, with $Ib=2\cdot Ia$ and $Ic=3\cdot Ia$. Since all functions can be expressed in terms of the α operator and the Post negation, the counterclockwise inverter is not necessary, because it can be always realized with two Post inverters in series. However, to reduce the number of transistors in the circuits, a counter-clockwise inverter was also designed. The Post inverter is shown in Fig. 3.

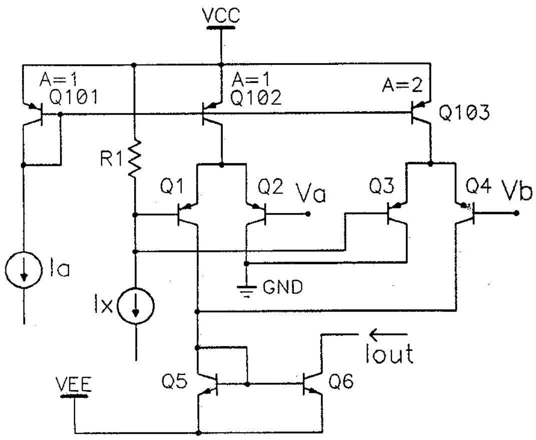

Fig. 3 - Circuit of the ternary cyclic Post negation.

The comparators with PNP transistors are not allowed to saturate, so they can switch very fast (even with standard lateral *PNP*'s). The threshold voltages *Va* and *Vb* are calculated to make the comparators change their output state when I is $(Ia+Ib)/2$ and $(Ib+Ic)/2$, respectively.

The principle of operation of the Post inverter is quite simple: when the input current $Ix=Ia$, the left side transistors of both comparators (Q1 and Q3) are not conducting and the current *Ia* from current sources Q102 and Q103 is deviated to Q2 and Q4. The collector current of Q2 is directed to ground and the collector current of Q4, which is $Ic4=Ic103=2\cdot Ia$, is fed into the input of the current mirror Q5-Q6. Since this current mirror has a unity transfer ratio, the output current is $Ic6=2\cdot Ia=Ib$.

When the input current *is* $Ix=Ib$, the voltage drop across *R1* makes the differential pair Q1-Q2 switches, so that $Ic1=Ia$ and $Ic2=0$. No changes occur in the comparator Q3-Q4,and the input of the current mirror is now equal to $Ic4+Ic1$, or $Ic6=3\cdot Ia=Ic$.

Finally, when the input current is $Ix=Ic$, the voltage in *R1* force the left sides of both comparators to conduct ($Ic1=Ia$ and $Ic3=2\cdot Ia$), and, since *Ic3* is discarded to ground, the current fed into the current mirror is $Ic5=Ic1=Ia$.

The circuit of the counterclockwise inverter is presented in Fig. 4. It has only two transistors more than the circuit of Fig.3, making it much more attractive than the alternative of using two Post inverters in series. The principle of operation of the counterclockwise Post inverter is similar to the classical Post inverter: when the input current is $Ix=Ia$, the left side of both comparators (Q1 and Q3) are not conducting and the current *Ia* from current sources Q102 and Q103 is deviated to Q2 and Q4, so that $Ic1 = Ic4 = Ia$.

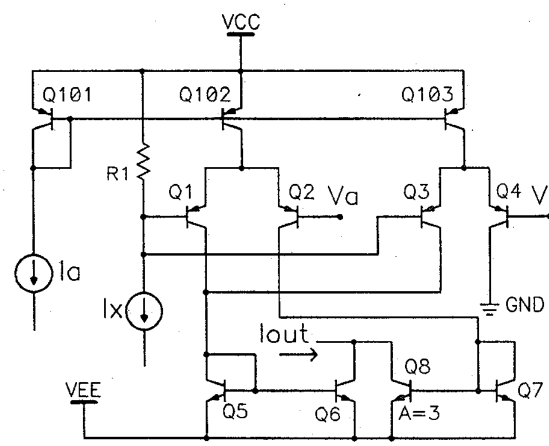

Fig. 4 - Counterclockwise inverter circuit.

The collector current of Q4 is steered to ground while the collector current of Q2 (*Ic2*) is transferred to Q7, the input transistor of the current mirror Q7-Q8. The area ratio of Q8/Q7 is made equal to 3, and the output of the current mirror is $Ic8=3\cdot Ia$. With Q1 and Q3 in the cutoff region, there is no input in current mirror (Q5-Q6) and the collector current of Q6 is zero. Therefore, the output current is $I =3\cdot Ia=Ic$.

When the input current is $Ix=Ib$, the voltage developed across resistor *R1* is sufficient to make the comparator (Q1-Q2) switch, making $Ic1=Ia$ and $Ic2=0$. No changes occur in the right-handed comparator. Now, the current mirror Q5-Q6 has an input current $Ic1=Ia$, while the input in current mirror Q7-Q8 is zero. The output current is $I =Ic8=Ia$. Finally, when $Ix=Ic$, both Q1 and Q3 are ON and their collector currents are fed into the current mirror Q5-Q6. Hence, $I =2.Ia=Ib$. A PSPICE simulation of both inverters is shown in Fig. 5.

A circuit realization of the β operator is shown in Fig.6. The design of the β operator was realized based on the interpretations of relative minimum or relative maximum presented previously. The output current of this circuit is either *Imin* or *Imax*, depending on which transistors are conducting (Q2 or Q4) in the comparators. The threshold voltage *Vc* is set to a value which makes both comparators change their states (Q1-Q2 and Q3-Q4) when the voltage across *R1* is equal to $R1\cdot(4.5\cdot Ia)$. When $Ix+Iy$ is greater than $(4.5\cdot Ia)$, the current *Imax* is selected in the output. When the current $Ix+Iy$ is less than $(4.5\cdot Ia)$, transistor Q2 is ON and, since Q4 is OFF, the output current is *Imin*. Thus, this circuit executes the desired β operation.

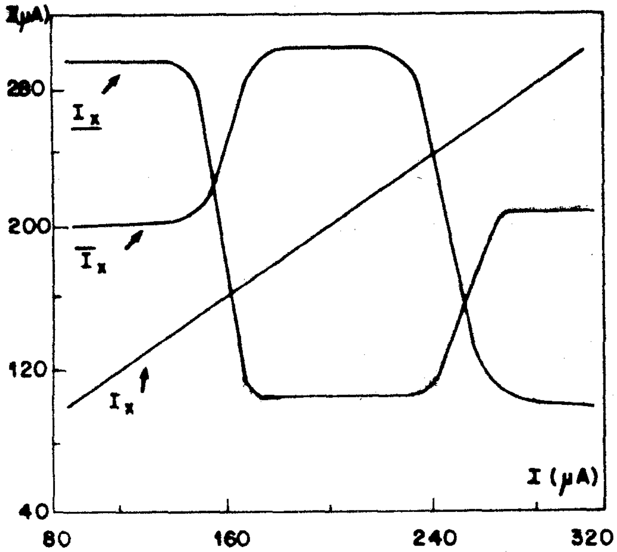

Fig. 5 - Result of PSPICE simulation of clockwise and counterclockwise inverter circuits.

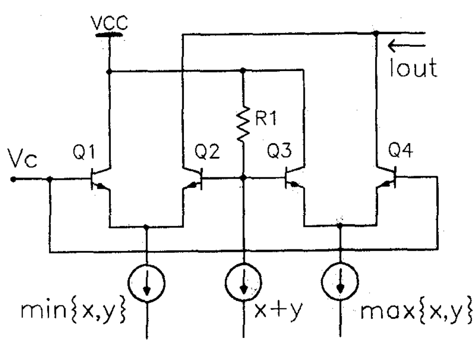

Fig. 6 - Circuit implementation of β operator.

A similar approach is used to design the γ operator. The only difference is that the positions of currents *Imin*, *Imax* must be interchanged and the threshold voltage *Vc* of the differential pairs must be set to make them switch when $Ix+Iy=3.5\cdot Ia$.

The circuit shown in Fig. 7, a conventional translinear circuit [9], produces the *Imax* current used in the β and γ circuits.

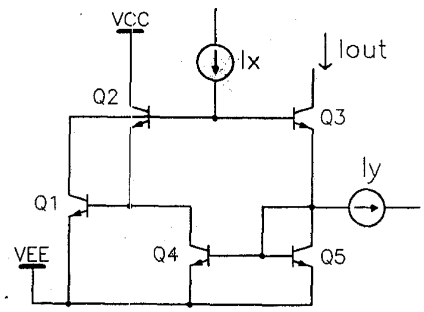

Fig. 7 - Translinear circuit which realizes the maximum selection.

From the circuits of Fig. 6 and 7, it is evident that several current mirrors would be necessary to change the polarities of the currents, and also adjust the collector voltage level of the transistors to avoid saturation. However, since both β and γ operators can be realized with the α operator and the negation (clockwise or counterclockwise), we believe that their fabrication is only of academic interest, because the number of transistors in their circuits is greater than in the α/negation realization.

V. Conclusion

A Post ternary logic with new operators is proposed. The operators β and γ allow the synthesization of logical ternary functions with simple algorithms. All operators were designed using current mode circuits, and they can be easily fabricated using bipolar technology.

Due to their current mode operation, these circuits exhibit excellent performance at very high frequencies. Circuits simulated using transistors models from a 7.5 μm standard (diffused isolation) bipolar technology (ft_{NPN} = 360 MHz and ft =2 MHz) were able to operate up to 20MHz.

These ternary current mode circuits fabricated with modern bipolar technologies, which have PNP and NPN transistors with *ft* higher than 1 GHz and 20 GHz respectively, would be very attractive for mixed signal analog/digital ASICS circuits intended to operate at high speed. A significant economy of silicon area can also be achieved with the use of ternary circuits, since the number of gates of a ternary circuit is much less than its binary counterpart.

To take full advantage of this current mode technique in mixed signal circuits, further developments in the area of ternary A/D and D/A conversion must be realized to interface the ternary circuits with the real world.

Although no concept has yet prevailed when circuit realization is concerned, it seems that I^2L has been the most used technology in multivalued circuits. However, the problems with operating speed and noise immunity typical in I^2L gates, however, limit its application. The proposed current mode technique can be an interesting solution for very high speed mixed signal ASICs.

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